



HAL
open science

Using of Bond-Wire Resistance as Ageing Indicator of Semiconductor Power Modules

Ali Ibrahim, Zoubir Khatir, Jean-Pierre Ousten, Richard Lallemand, Stefan V. Mollov, Nicolas Degrenne, Damien Ingrosso

► **To cite this version:**

Ali Ibrahim, Zoubir Khatir, Jean-Pierre Ousten, Richard Lallemand, Stefan V. Mollov, et al.. Using of Bond-Wire Resistance as Ageing Indicator of Semiconductor Power Modules. *Microelectronics Reliability*, 2020, *Microelectronics Reliability*, 114, 10.1016/j.microrel.2020.113757 . hal-03153283

HAL Id: hal-03153283

<https://hal.science/hal-03153283>

Submitted on 26 Feb 2021

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Using of Bond-Wire Resistance as Ageing Indicator of Semiconductor Power Modules

A. Ibrahim, Z. Khatir, J.P. Ousten, R. Lallemand, N. Degrenne, S. Mollov, D. Ingrassio

Abstract – This paper investigates the use of wire—bonds contact resistance as indicator to diagnose the health state of power electronics modules. This technique is especially dedicated to monitoring the degradation of the topside interconnection (metallization-wire bonds) when the module is wired with a Kelvin point. One advantage of this indicator is that it can be followed online, without being disturbed by current or voltage, to diagnose the state of health and, possibly, the prognosis of the remaining lifetime of the power module by associating it with a lifetime model. For this purpose, based on power-cycling tests in different conditions, a comparison between this indicator and the one commonly used, i.e. the collector-emitter voltage V_{ce} , shows that the first one is much more sensitive to the degradations, easier to use online and finally should be more suitable for lifetime prognosis.

1. Introduction

Power semiconductor modules are the key elements in the chain of power conversion. Nowadays, they are widely used in various applications but these components remain also the weak element of power conversion systems in terms of reliability. In fact, power modules constitute an assembly of various materials (Fig. 1). Generally, the power chips are carried on a ceramic substrate which must ensure good electrical insulation and good thermal conduction. The substrate could be welded on a base plate to be cooled. The assembly technologies are various. This includes materials and process for insulation or passivation, interconnections, and die attach. Due to power and thermal cycling, the power modules are subjected to thermomechanical stresses which affect their lifetime and reliability [1]. The topside interconnections, consisting of the metallization and the wire bonds, are subjected in operation to high functional stresses. This is the result of an important difference between the coefficients of thermal expansion (CTE) of the materials in contact: metallization and wire bonds (aluminum) and dies (silicon). The metallization layer (around 5 μm) deposited on the chips becomes very distorted with temperature, leading to large inelastic strains [2]. It has been reported that two main types of degradation can take place in the topside of power chips under the effect of thermomechanical cycles: metallization reconstruction (Fig. 2) and degradation of bonding contacts [2], [3], [4]. The last one may itself be either heel-cracks or cracks propagation followed by lift-off [5] (Fig. 3). Various works have been conducted to propose scenarios of degradation mechanisms using thermal and power cycling tests [6], [7]. Although it is quite clear that the wire-bond lift-off contributes mainly to the module failure [8], this link is not obvious with the metallization degradation [8].

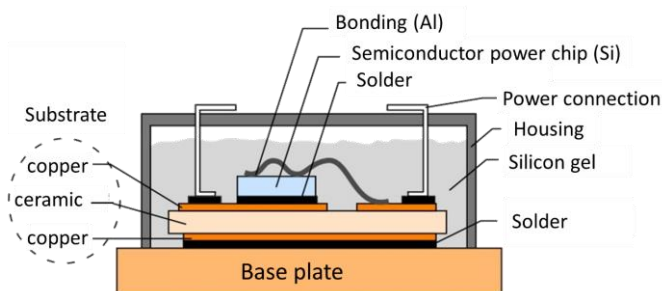


Fig. 1: General structure of power module.

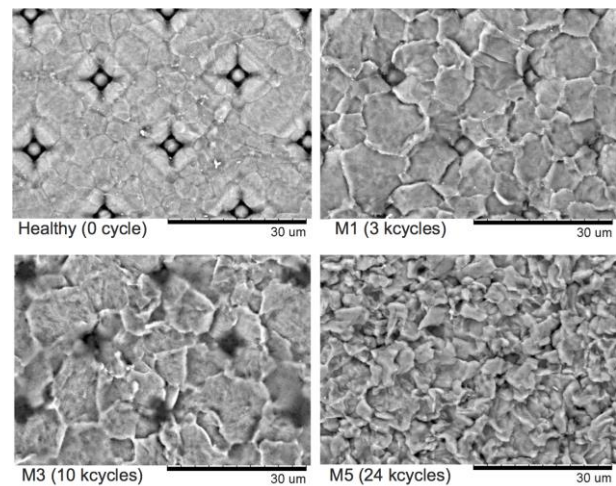


Fig. 2: Topside metallization: before and after aging.

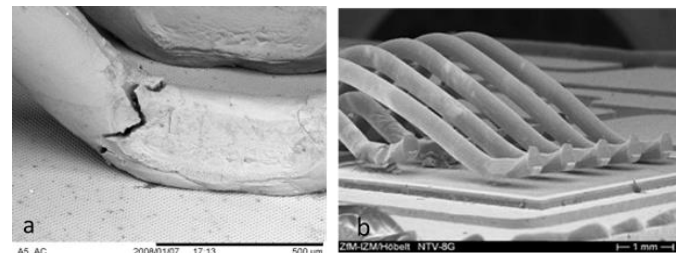


Fig. 3: Heel crack (a) and Lift off (b) of bond wires

Classically, for the top-side interconnection, the collector-emitter voltage drop (V_{CE}) is used to monitor the status of degradations. Nevertheless, it is difficult to perform this measurement online, in addition it is a global measurement and does not allow to locate directly the failure in the power module. This paper proposes an alternative diagnostic tool based on the monitoring of the resistance of bond-wires to follow the degradation of the topside interconnections. Its main advantage is that it could be used for online diagnosis, it is easy to implement and is directly related to the failure of topside interconnections. This technique requires the use of the Kelvin connection to the source, so the resistance of bond-wires is measured between Kelvin connection and the mid leg for high side and between Kelvin connection (if it exists) of the lower side and the negative bus of the power modules. Such condition monitoring has been made in case of silicon carbide Mosfets in discrete case package [9]. The purpose was to be able to separate

a possible degradation from the semiconductor chip itself. Here, the concept is applied for the first time to IGBT power modules for online condition monitoring.

2. Power cycling tests methodology and results

A. Test circuit and protocol

Accelerated aging tests have been performed on standard six-pack modules IGBT power modules (1200V-150A). Only high side IGBT's have a Kelvin connection. The power cycles are performed on 6 modules at a time for which only the central leg is tested. This constitutes 2 DUTs respectively high side and low side switches per power module. The power modules are mounted in a water-cooler heat-sink device with a thermal grease interface. The circuit schematic of the test bench is shown in Fig. 4. The aging consists on repetitive cycles of self-heating and cooling phases. The power devices undergo thermal stresses due to temperature swings ΔT_j between a maximum (T_{jmax}) and a minimum junction temperature (T_{jmin}) depending on the setting parameters.

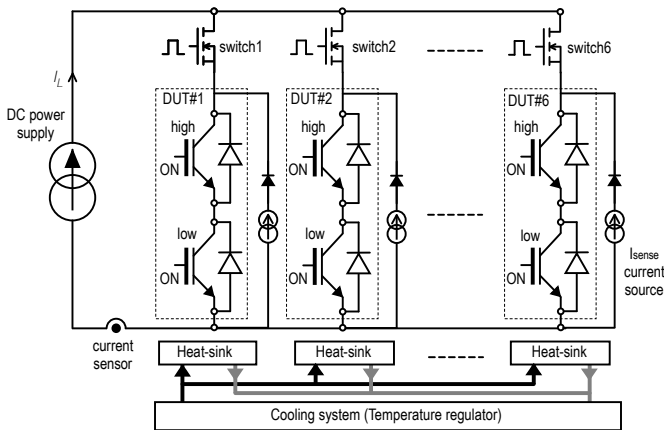


Fig. 4: Schematic power cycling test circuit.

All electrical and thermal measurements (V_{CE} , V_{GE} , I_L , V_{bond} , I_{sense} , T_{case} and $T_{heat-sink}$) are monitored and recorded. The switching sequence is controlled by auxiliary power MOSFETs. A permanent low current ($I_{SENSE}=50mA$) is flowing through the devices under test (DUTs) in order to get the junction temperature (T_j) by the thermo-sensitive electrical parameter (TSEP), i.e the collector-emitter voltage ($V_{CE} @ V_{GE}=15V$). The case temperature, below each IGBT chip of the central leg, and inlet water temperature are measured by close thermocouples for evaluating junction-to-case (R_{THJC}) and junction-to-water (R_{THJW}) thermal resistances. The DC current load (I_L) is set in order to reach the targeted temperature swings (110K, 90K and 70K). The power cycling test conditions are summarized in Table I : temperature swing (ΔT_j), minimum junction temperature (T_{jmin}), load DC current (I_L), heating time (t_{ON}). In the following, the number of cycle to failure N_f is normalized for reasons of confidentiality.

TABLE I: POWER CYCLING TEST CONDITIONS

Test case#	ΔT_j (°C)	T_{jmin} (°C)	I_L (A)	t_{ON} (s)
1	110	35	150	3
2	90	35	135	3
3	70	35	120	3

The ageing indicators are collector-emitter voltage (V_{CE}), resistance of contact (R_{bond}), and junction-to-water thermal resistance (R_{THJW}). The resistance of contact is obtained by dividing the potential difference between the Kelvin connection and the mid-leg connection over the load current; this resistance includes the resistance of the metallization, the resistance of the contact between the metallization and the wire bonds (includes electrical constriction resistance [10]) and the resistance of wire bonds.

$$R_{bond} = \frac{V_{bond}}{I_{load}} = R_{metallization} + R_{contact} + R_{bonding}$$

We assume that the change of resistance of wire-bonds is not significant and the variation of R_{bond} is related only to the state of the metallization and the contact between metallization and wire bonds.

Ageing indicators are always measured in the same electrical and thermal conditions in static characterization phases. For this purpose, the aging is regularly interrupted to perform them. During characterizations, power current is set to 58A. Each IGBT is subjected to this current for 10 minutes, the time necessary to reach thermal steady state. The thermal resistance, the voltages V_{CE} and V_{bond} are measured just before switch off of the current.

Measured voltage V_{CE} may possibly include a thermal contribution due to any increase in thermal resistance from possible delamination of the die attach. So, this latter contribution needs to be removed from the measured V_{CE} in order to detect only the contribution due to the top-die interconnection degradations. Thus, a correction on the measured V_{CE} is done to get only the degradations related to top-metal and bonding wires contacts.

Furthermore, all these parameters are monitored "on the fly". However, as these latter measurements can be performed under slightly different conditions, they can introduce some errors. Nevertheless, the resistance R_{bond} remains less dependent on the measurement conditions than the V_{CE} because it does not depend on the chip characteristics. So, its measurement "on the fly" gives more confident and relevant results.

The test bench is set to interrupt aging test if the V_{CE} or R_{bond} progressions reaches the thresholds of 5% or 180% respectively.

B. Test results

Fig. 5 illustrates the evolution of the relative variation of V_{CE} of high side IGBT's during power cycling for the six tested modules at $\Delta T_j=110K$. It can be seen for all components that the relative voltage increase is quite linear till 1%, due to the metallization degradation and to the crack propagation in the wire-bond interconnection with the metallization, then there are multiple jumps until 5% which is the failure criteria. However, there is no significant evolution in the V_{CE} of low side IGBT's, it's still around 0.5%. All tested devices have failed by bond-wire lift-off due to crack propagation in the high side IGBT chip. Moreover, microscopic analyzes have shown that the degradations on the high side are located essentially in the red ellipse, shown in Fig. 9. No significant variation in thermal resistance was detected, indicating that no delamination or degradation has occurred in the structure. This has been verified and confirmed by scanning acoustic microscopy (SAM) analysis as shown in Fig. 6 (By comparing the state of the central part (aged part) and the other two parts on both sides).

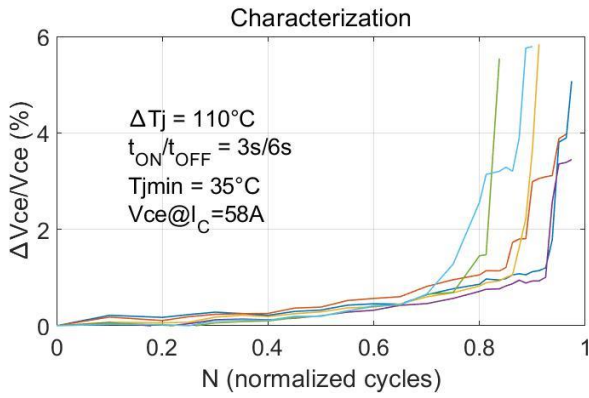


Fig. 5. Monitoring of VCE during static characterizations.

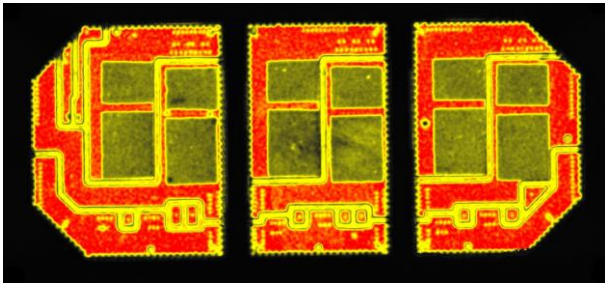


Fig. 6. Scanning acoustic microscopy of module after aging.

The degradation of wire-bond interconnection with the metallization is investigated by optical microscope analysis. This result is consistent with the measurements of bonding resistance during static characterization phases (Fig. 7) and "on the fly" measurements (Fig. 8). By comparison of Fig. 5 and Fig. 7, they have the same tendency and we can establish a correlation. For example, a threshold of 1% and 5% in $\Delta V_{\text{CE}}/V_{\text{CE}}$ matches with 25% and 180% in $\Delta R_{\text{bond}}/R_{\text{bond}}$ respectively. The Fig. 8 shows that the "on the fly" measurements (for $\Delta T_j = 110\text{K}$ and $\Delta T_j = 70\text{K}$) are as accurate as static characterization ones but with a continuous sampling because the monitoring is easily and accurately performed continuously during aging. So, based on this results, this parameter could be advantageously used as aging indicator for the top interconnection.

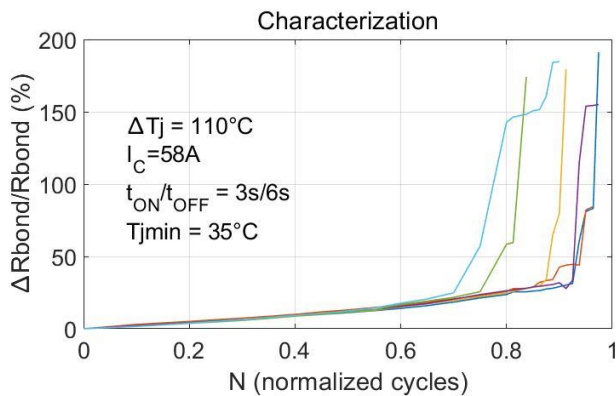


Fig. 7. Monitoring of wire-bonds resistance during static characterizations.

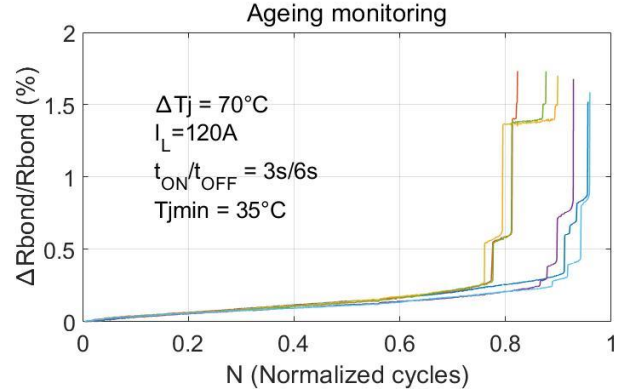
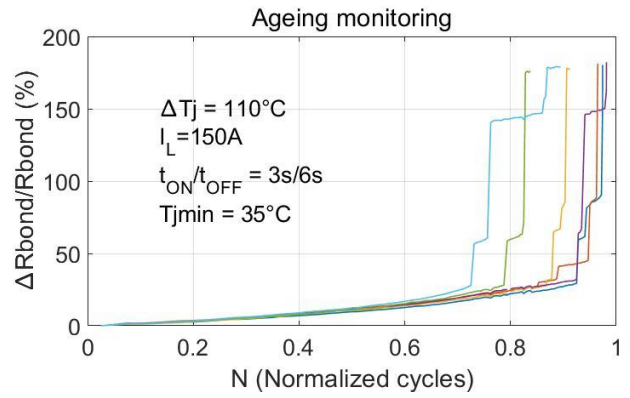


Fig. 8. Monitoring of wire-bonds resistance "on the fly".

3. Specific investigations on the bond-wires resistance

Some measurements have been performed on a healthy half bridge to understand the impact of bond-wires lift-off. The study focuses on the six bond-wire contacts as represented by the red ellipse in Fig. 9. These contacts are causing the module failure apart from the degradation of the metallization. A current of 1A ($\pm 2.3\text{mA}$) is applied using a Source Meter Unit on the DC bus of the half bridge where the two IGBTs (high and low sides) are in the on state ($V_{\text{GS}} = 15\text{V}$). The current is chosen relatively low to avoid self-heating of bondings and dies. The voltage is then measured between the kelvin point of the high side IGBT and the midpoint, avoiding the effect of bonding of mid-point. The resistance of the top interconnection corresponds to the voltage and current ratio. All measurements are made at 25°C .

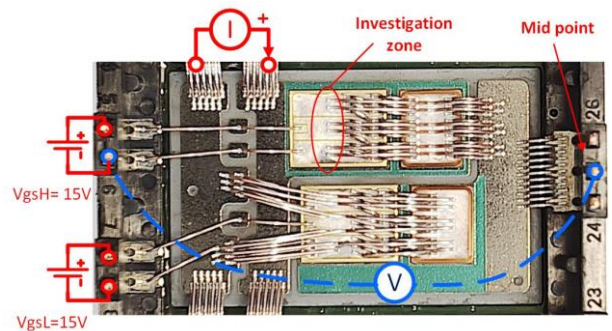


Fig. 9. Measurement of the resistance of the top interconnection.

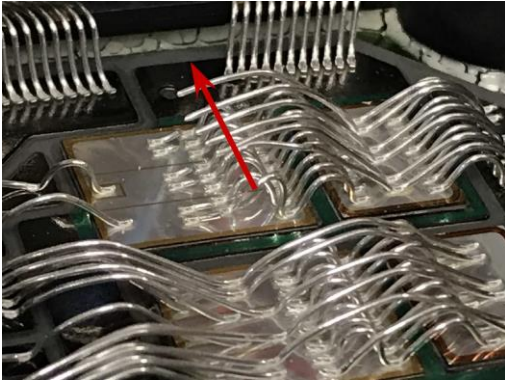


Fig. 10. Manually open contact of wire bonds

The bond-wires were cut out successively one by one from one edge to the other as seen in Fig. 10. Given the location of the high and low chips, it is intuitive to deduce that there will be a mutual heating effect which induces an inhomogeneity in the temperature distribution because the dies are warmer in the direct vicinity. As the damage also depends on the temperature, the degradation of the contacts will be more pronounced on the edge near the low side chip and consequently the lift-off of wire-bonds should begin from this edge. This hypothesis has been confirmed by microscopic observation. The equivalent resistance, given in Table II, has been noted each time a contact was opened. These measures are strongly correlated to the aging tests. Indeed, there is an increase in $\Delta R/R$ of 26% for the disconnection of one contact and 176% for the loss of 5 bond wires. In fact, the resistance is very sensitive to the position of bond wires on the metallization with regard to the Kelvin point. The metallization consists of three parallel pads (see Fig. 10). The lift-off of the two wire bonds from the common pad with the Kelvin point forces the current to pass through the metallization that represents a higher resistance and consequently a strong increase in the overall electrical resistance of the contact. This explains some variabilities in the progress of $\Delta R/R$ for the six DUT's as shown clearly on Fig. 8. But whatever the order of detachment of wire-bonds, we can always determine the moment when the wire-bonds start to lift-off, and also the increase of R_{bond} to 175% always corresponds to an increase in the V_{CE} to 5% and to the end of life of the module.

TABLE II : VARIATION OF THE RESISTANCE OF THE TOP INTERCONNECTION WITH BOND-WIRE LIFT-OFF

Number of wire bonds cut-off	Current (A)	$V_{CE}(mV) \pm 0.15mV$	Resistance (m Ω)	% $\Delta R/R$
0	1	1,64	1,64	0
1	1	2,09	2,09	26
2	1	3,72	3,72	120
3	1	3,9	3,9	131
4	1	4,49	4,49	165
5	1	4,64	4,64	173
6	1	5,14	5,14	202

4. Numerical simulation

In this part, a 2-D model was built using Simulink in order to reproduce what is done by experimental study and to quantify the effect of metallization and contact degradations. Fig. 11 shows a part of the model that represents one pad of the metallization. Where:

- Bond-wires are represented by R_{bond} and R_{bondC} , it depends to the length of bond-wire.
- R_{cont} represents the resistance of contact bond-metallization, it was deduced by experimental

- measurement.
- R_{met} is the resistance of the metallization and is determined by 4-wires measurement at the extremity of the pad and confirmed by a theoretical approach.
- R_{on} represents the On-State resistance of IGBT
- V_{bond} is the measure of potential difference between the Kelvin connection and the output of the circuit.
- $V_{ceKelvin}$ is the collector emitter voltage measured between collector and Kelvin connection.

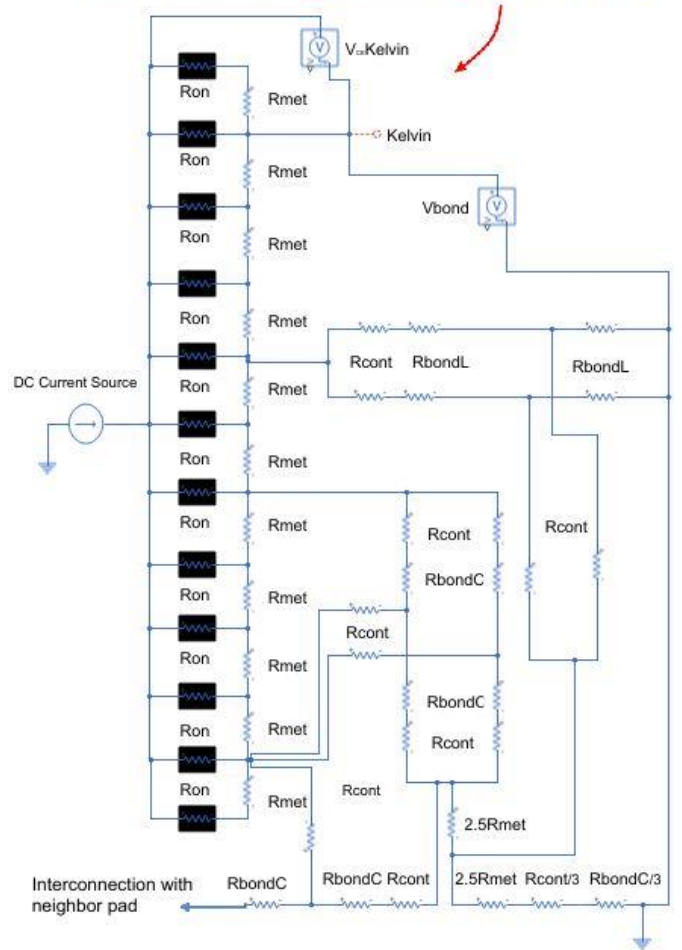
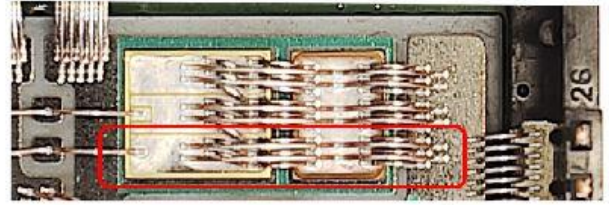


Fig. 11. Electrical model of metallization and top interconnection.

Table III summarizes the different parameters used in this model. To estimate all of them, an optical profilometer is used to determine the dimension of the metallization and the position of contacts on the metallization area. Based on that, each pad is represented by a network of 10 elementary cells ($R_{met}/2 - R_{on} - R_{met}/2$) and then it has been grafted a connection wires which are represented by a contact resistance and a bonding resistance. Admittedly this model is simplified but it makes it possible to validate some experimental measurements and to link the variation of the V_{CE} to the degradation of the metallization and the contacts. All results are given in a steady state under constant temperature.

TABLE III : PARAMETERS USED FOR SIMULATION

R_{bond}	10 m Ω
R_{bondC}	5 m Ω
R_{cont}	2 m Ω
R_{met}	4.6 m Ω
R_{on}	36 m Ω
I_{load}	60A

First, we simulate the bond-wire lift-off by opening the contacts one by one. As reported in Table IV, we find the same trend in the progression of the interconnection resistance including metallization, contacts and wires. As expected, we notice that the progression is not linear especially with the loss of the prime two contacts. The evolution of the voltage $V_{CEKelvin}$ taken with the kelvin connection also confirms our experimental observation. Indeed $V_{CEKelvin}$ decreases with aging regardless of degradation or not of metallization. This is explained by the fact that the current is redistributed over the other pads of the metallization when contacts degraded. We would just caution the use of kelvin connection for measuring V_{CE} , whatever as an aging indicator or as a thermosensitive parameter for the indirect measurement of the junction temperature.

TABLE IV : SIMULATION OF CONTACT DEGRADATIONS

N° of open contacts	% $\Delta V_{CEKelvin}$	% ΔV_{CE}	% $\Delta R/R$
0	0,0%	0,0%	0,0%
1	-2,0%	0,8%	21,4%
2	-9,4%	3,7%	103,1%
3	-9,2%	4,8%	110,6%
4	-8,6%	8,4%	136,7%
5	-8,0%	9,6%	142,2%
6	-5,8%	13,9%	162,3%

In [8], investigation in the degradation of the metallization with aging have been done, it has been noticed that the damages in the metallization appear immediately at the beginning of the aging. In addition, it has been observed an increase of around 25% in the resistance of the metallization equivalent to a V_{CE} increase of 1.15%. It should be mentioned that the study presented in [8] was conducted on another type of module but both modules in these studies have an aluminum metallization. By simulation, the degradation of the metallization can be represented here by changing its resistance progressively to 30% without any degradation in bond-wire contacts. Curiously, V_{CE} increases also to 1.1% as it is resumed in Table V. The cause of the increase in metallization resistance can be either due to a change in the aluminum resistivity because of chemical reactions, or a modification of the geometry due to metal reconstruction. Anyway, this leads to a redistribution of the current in the die and on the metallization and then justify the negative evolution of $\Delta V_{CEKelvin}$. Once again, the use of $V_{CEKelvin}$ is compromising.

TABLE V : SIMULATION OF DEGRADED METALLIZATION

% ΔR_{met}	% $\Delta V_{CEKelvin}$	% ΔV_{CE}	% $\Delta R/R$
0,0%	0,0%	0,0%	0,0%
5,0%	-0,1%	0,2%	2,1%
10,0%	-0,1%	0,4%	4,2%
15,0%	-0,2%	0,6%	6,2%
20,0%	-0,2%	0,8%	8,2%
25,0%	-0,3%	1,0%	10,2%
30,0%	-0,3%	1,1%	12,2%

The resistance of the interconnection is sensitive both to the degradation of the metallization and to the degradation of the

contact. This parameter can be used to diagnose the state of the interconnection and to assess the module's health online.

5. Conclusions

An alternative diagnostic tool based on the monitoring of the resistance of bond-wires to follow the degradation of the topside interconnections of Insulated Gate Bipolar Transistors (IGBT) power modules has been presented in this paper. The main advantage is that it could be used for online diagnosis, it is easy to implement and is directly related to the failure of topside interconnections. The experimental and simulation results show the good accuracy of the proposed technic and its potential to be used as aging indicator or as failure precursors for online lifetime prediction. However, using this indicator is conditioned by the presence of the Kelvin connection to the source. Also, this indicator is sensitive to the position of the Kelvin wire bond on the metallization. It is necessary to validate this tool with other modules and other topographies in order to establish a finer correlation with the collector-emitter voltage drop (V_{CE}).

References

- [1] V. Smet, F. Forest, J.J Huselstein, F. Richardeau, Z. Khatir, S. Lefebvre, M. Berkani, "Ageing and Failure Modes of IGBT Modules in High-Temperature Power Cycling", IEEE Trans. on Industrial Electronics, vol. 58, n°10, pp. 4931-4941, 2011.
- [2] M. Ciappa, "Selected failure mechanisms of modern power modules", Microelectronics Reliability. 42, p.653-667 (2002)
- [3] Th. Detzel, M. Glavanovics, K. Weber, "Analysis of wire bond and metallization degradation mechanisms in DMOS power transistors stressed under thermal overload conditions", Microelectronics Reliability. 44, p.1485-1490 (2004)
- [4] S. Russo et al., "Fast thermal fatigue on top metal layer of power devices", Microelectr. Reliab. 42, p.1617-1622 (2002)
- [5] S. Ramminger, N. Seliger, G. Wachutka. Reliability Model for Al Wire Bonds subjected to Heel Crack Failures. Microelectronics Reliability. 40, 1521 (2000).
- [6] P.A. Agyakwa, L. Yang, E. Arjmand, P. Evans, M.R. Corfield and C.M. Johnson. Damage Evolution in Al Wire Bonds Subjected to a Junction Temperature Fluctuation on 30K. J. Electron. Mater. (2016)
- [7] D. Martineau, C. Levade, M. Legros, P. Dupuy, T. Mazeaud. Universal Mechanisms of Al metallization ageing in power MOSFET devices. Microelectronics Reliability. 54, 2432 (2014).
- [8] N. Dornic, A. Ibrahim, Z. Khatir, J. Ewanchuk, S. Mollov, "Analysis of the degradations mechanisms occurring in the topside interconnections of IGBTs Power Devices", Microelectronics. Reliability, Vol.88-90, pp.462-469, 2018
- [9] N. Baker, H. Luo, F. Iannuzzo, "Simultaneous On-State Voltage and Bond-Wire Resistance Monitoring of Silicon Carbide MOSFETs", Energies, 10 (3), 2017.
- [10] R. Holm, *Electric Contacts*. Berlin, Heidelberg: Springer Berlin Heidelberg, 1967.