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Low voltage switching cell for high density and modular 3D power module with integrated air-cooling

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Abstract

This paper presents the TAPIR (compact and modular Power modules with IntegRated cooling) power module technology based on dual side air-cooling, the heat sinks acting as electrodes of power devices. Used with a large number of power semiconductor devices, this technology improves the cooling performances while maintaining low stray inductances in switching cells. It is therefore suited to high-speed devices and allows increasing the density of power converters. A low-voltage switching cell is designed and electrically and thermally tested. The weight of the semiconductor and thermal management parts of a three-phase inverter made with TAPIR technology is estimated and compared with more classical packaging approaches.

1. Introduction

The challenges of tomorrow's power electronics are among others the improvement of semiconductor packaging [1-2]. Particularly, new power modules are designed to reduce electrical and electromagnetic disturbances in order to be used with high switching speed devices [3]. The optimization of the thermal management system is also a major issue to reduce the weight of converters and meets the needs of electrical mobility. Indeed, the weight of the cooling system is generally non-negligible. For example, Delhommais et al. [4] propose a global optimization of a SiC switching cell and show that about 25% of the weight is due to the heat sink and the fan. For a Si switching cell, they show that 38% of the weight is due to the cooling system because losses are higher.

This paper presents a double-sided cooling technique, called TAPIR; adapted to high switching speed semiconductors and that would allow reducing drastically the weight of power converters. Contrarily to most researches on double side cooling [5], the heat extraction is made by air cooling and the heatsinks are used as electrodes like it is done in press-pack power converters [6]. As it will be seen later, this implementation technique allows for a better distribution of heat losses inside the cooling system and therefore increases the effectiveness of heat sinks that are thus lighter than in classical cooling systems.

TAPIR technology will be presented in the next section. Then an implementation of a switching cell will be proposed using discrete low voltage silicon components. The switching cell will be characterized from electromagnetic and thermal points of view. Before concluding, the weight of the semiconductor and thermal management parts of a three phase inverter will be estimated and compared with more classical packaging approaches

2. TAPIR technology

The basic of the proposed technology consists of inserting a semiconductor chip between two aluminum heatsinks (see **Figure 1**). The buffer part of the gate drive circuit can also be contained between these two heatsinks to be as close as possible to the chip for reducing disturbances on the gate circuit. Ideally, the chip can be connected (soldered or silver sintered) directly to a heatsink on one face to reduce the number of thermal interfaces. Note that plating of the aluminum heatsinks is necessary to perform the soldering process. There is not any ceramic material in this assembly, thus ensuring a good electrical and thermal conduction.

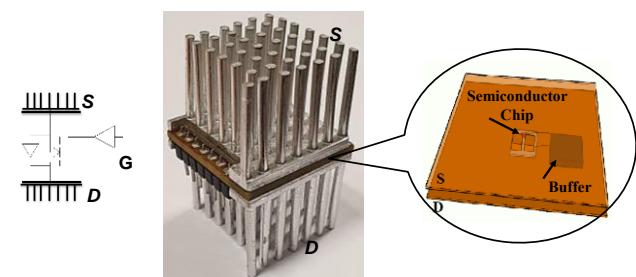


Figure 1 TAPIR elementary brick

The elementary brick of **Figure 1** can be connected with others in series or in parallel through heatsinks to construct different types of converters. As an example, **Figure 2** presents a possible implementation of an multiphase converter with four arms. The heat sinks are plotted in grey: they are plate fin heat sinks but they could be made using different technologies (foams, pin fins (**Figure 1**)...) to optimize the cooling efficiency. In orange, there are metallic plates to connect the heatsinks to each other. The green parts are isolating materials that can be made in plastic or polymer materials. The blue part is also an isolating material in which it is interesting to integrate a

capacitor to reduce the stray inductance of the switching cells. Note that an enclosure surrounding the system (not represented in **Figure 2**) is necessary to isolate the heatsinks from the outside and/or manage conducted and radiated electromagnetic fields. As it can be seen in **Figure 2**, one major advantage of this technology is to distribute the heat sources (semiconductor chips) in the whole volume of the cooling system. Furthermore, cooling on both sides and directly on the power component improves the evacuation of the heat flux. This would allow increasing the power density compared to classical systems.

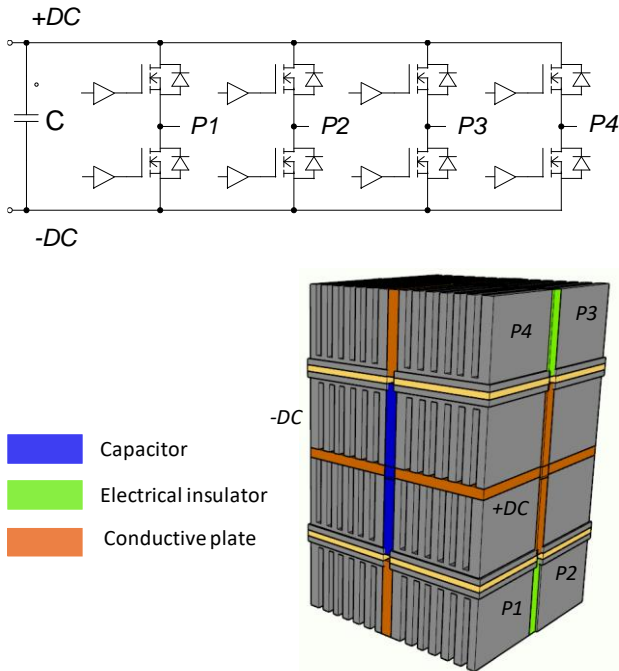


Figure 2 Possible implementation of a multiphase converter

The following section will be dedicated to the presentation of a first implementation of a single switching cell.

3. Low voltage switching cell

SiC and Si MOSFET semiconductor chips available on the market have generally a source metallization that is not adapted to the proposed technology (aluminum plating). Thus, to make a first implementation of the proposed technology, packaged components adapted to double side cooling were used. They are 60V-100A silicon MOSFETs TPW1R306PL components from Toshiba (**Figure 3**).

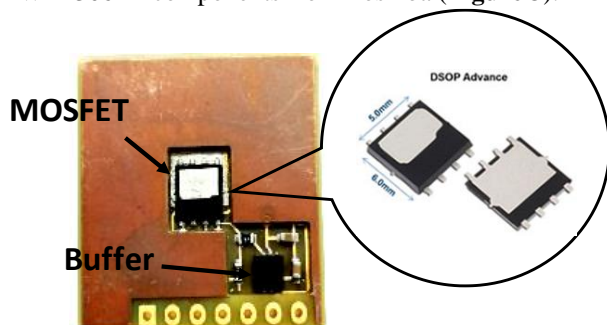


Figure 3 Top view of the PCB including electronic devices

A printed circuit board (PCB) was made to connect the power MOSFET with the buffer of the gate driver circuit (**Figure 3**). The Drain electrode of the MOSFET is soldered to the PCB and the Source is directly accessible on the top of the PCB through one cavity. The Source electrode can then be directly assembled on a tin plated heatsink. The connection of the Drain electrode to the other heatsink is made via a copper inlay inside the PCB. **Figure 4** shows the specific architecture of the PCB. It is a four layers PCB with a cavity between layers 1 and 3. The components (MOSFET packaged, buffer circuit) are soldered in the cavity and on layer 3. The details of this layer can be seen in **Figure 5**. Under the MOSFET, there is a copper inlay between layers 3 and 4. It is used to make the drain potential accessible from the bottom layer of the PCB with low electrical and thermal resistances.

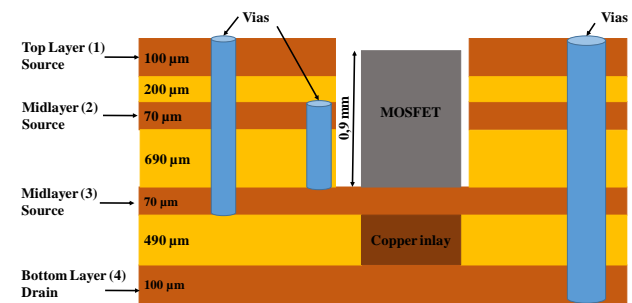


Figure 4 Architecture of the PCB

The deepness of the cavity (0.9mm) and thus the thickness of related PCB layers is linked to the thickness of the packaged MOSFET and its solder, this device being the thickest component of the circuit. The upper surface of the MOSFET and the height of layer 1 of the PCB should ideally be the same or as close as possible in order to make the soldering process easier and to have a good electrical and thermal contact with the heatsink. Layer 1 is at the Source potential like the heatsink. Layers 2 and 3 are also at the Source potential through vias as it can be seen in blue at the left hand side of **Figure 4**. This architecture allows reducing the gap between Source and Drain potentials in order to reduce the stray inductance. The stray inductance could be further reduced by decreasing the FR4 thickness between layer 3 and 4. The PCB manufacturer (CIBEL) has achieved the thickness of 490μm to facilitate the PCB manufacturing process. The connector in **Figure 5** is used to power and control the buffer. The first three pins from the left are connected to the MOSFET electrodes (Drain, Source and Gate) for implementing Kelvin measurements as close as possible to the component.

Layer 4 of the PCB is thick (205μm) for a better heat spreading and thus minimizing the thermal resistance of the assembly.

The PCB with the soldered component is sandwiched between two aluminum heatsinks previously coated with 5μm Ni and 5μm Sn. A lead-free solder (Sac 305) is used to solder the components inside the hole and also for assembling heatsinks and PCBs, so that the assembly

between elementary bricks is carried out with lead solder (lower soldering temperature). One elementary brick after the soldering process is presented in the center of **Figure 1**. Two elementary bricks are then assembled to fabricate a switching cell (**Figure 6**). This figure shows that three aluminum plates were also assembled to the heatsinks for electrical connections of the switching cell with a power supply and a load.

The capacitor C included in this assembly is achieved by integrating numerous SMD capacitor (0803) into a PCB. This capacitor is made with 63 capacitors of $10\mu\text{F}$ each and a capacitance value of $570\mu\text{F}$ is measured using a multimeter. This capacitor is inside the structure and thus allows reducing the stray inductance.

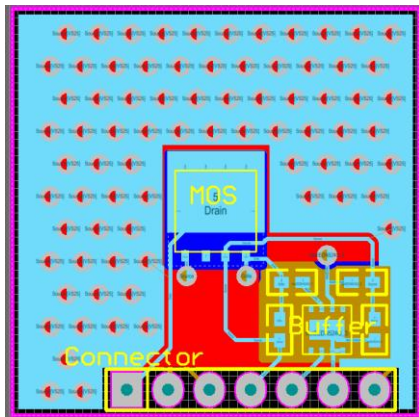


Figure 5 PCB layer 3 architecture

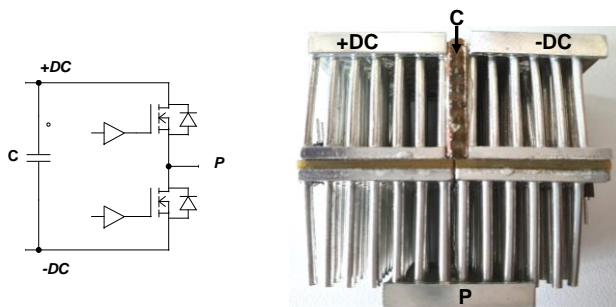


Figure 6 Implementation of TAPIR switching cell

4. Characterization

4.1. Electrical measurements

The on-state resistance between two heat sinks was measured by a Kelvin measurement to check the quality of the electrical connections. A global resistance of $0.92\text{ m}\Omega$ was obtained with $V_{\text{GS}}=15\text{V}$, while $R_{\text{DSon}}=0.95\text{ m}\Omega$ for $V_{\text{GS}}=10\text{V}$ in the datasheet.

The double pulse method is then used to test the switching cell and to estimate the value of the stray inductance. The test bench is presented in **Figure 8**. Different tests under different current levels were carried out. The stray inductance value was obtained measuring the oscillation frequency of the drain-source voltage V_{DS} after turn-off and using the value of the output capacitance C_{oss} of the device (the additional capacitance due to the package is

largely lower in this case). The stray inductance was estimated to be close to 2 nH which confirms the good behavior of the switching cell for the implementation of high switching speed devices. **Figure 9** shows the rate of the V_{DS} voltage across the controlled MOSFET (the one on the left in Figure 6) during turn-off for a bus voltage of 25V and 50 A current in the load.

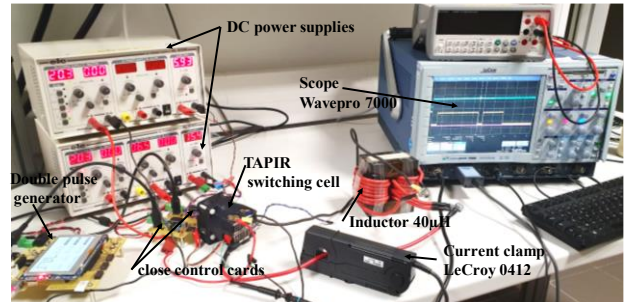


Figure 8 Electromagnetic measurement test bench

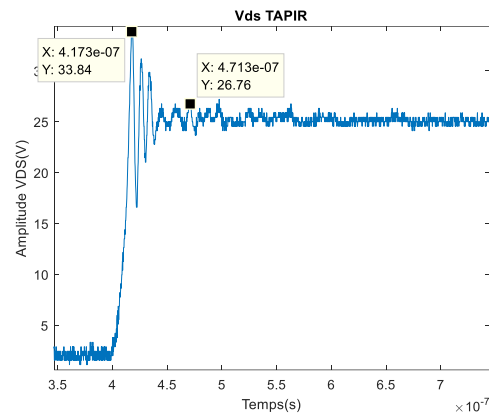


Figure 9 V_{DS} during turn-off for TAPIR switching cells ($V_{\text{DS}}=25\text{V}$ and $I_{\text{D}}=50\text{ A}$)

4.2. Thermal characterization

The purpose of this section is to analyze the thermal performance of the TAPIR switching cell. The thermal resistance between the junction and the ambient air is measured. Packaged semiconductors are cooled by forced convection as presented in **Figure 10**. The reference of heat sinks and the fan are respectively ICKS $25*25*18.5$ from Fischer Elektronik and AFB0612DH from Delta Electronics.

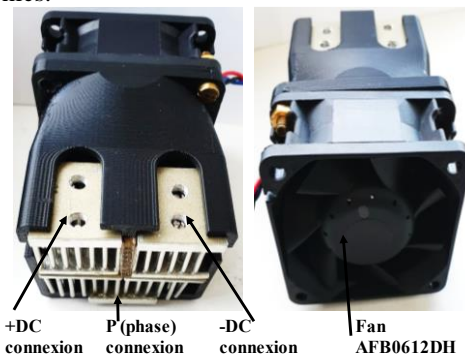


Figure 10 Global view of the cooled switching cell

In the literature, several methods exist to measure the junction temperature of power semiconductor devices [7]. Temperature measurement by thermo-sensitive electrical parameters (TSEPs) is today the main way to carry out fast measurements on packaged devices [7]. In the case of power MOSFETs, the forward voltage under low bias current of the body diode can be used as temperature indicator. The voltage dependence is close to $-2\text{mV}/^\circ\text{C}$ for silicon devices [8].

During the calibration step, the temperature is fixed by an oven. A measurement of the body diode voltage V_{SD} is performed for several temperatures and a current I_m of 20 mA (Figure 11).

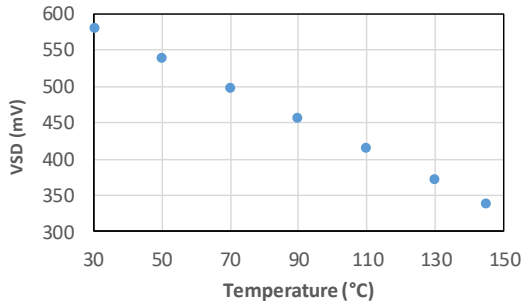


Figure 11 Body diode voltage V_{SD} as function of the device temperature ($I_m=20$ mA and $V_{GS}=-5\text{V}$).

The circuit of Figure 12 is designed to estimate the junction temperatures of the components under constant dissipation thanks to the calibration previously performed [9]. One device is heated by using a high current source I_p . Two thermocouples are placed in the baseplate of the heatsinks to determine when the stationary state is reached. Once the temperature is stabilized, the voltage across the other MOSFET is measured to estimate its junction temperature and to estimate the thermal coupling between both devices. Then the current in the hotter MOSFET is turned off and it is possible to estimate its temperature during dissipation. The ambient temperature is measured with the thermosensitive parameter before the current dissipation step. This temperature is 22°C .

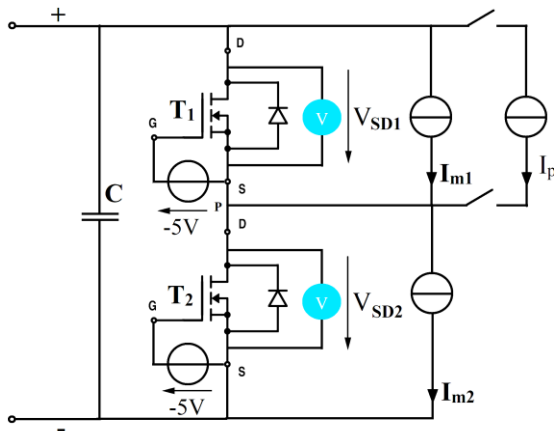


Figure 12 Circuit for measurement of the diode forward voltage under low current

For 100 A drain current, the power dissipation is 73W. In these conditions, the estimated junction temperature of the dissipating MOSFET is 119°C . The temperature of the other MOSFET is 37.5°C . The junction to ambient thermal resistance of the MOSFET is thus close to 1.30 K/W. The coupling thermal resistance is 0.2 K/W.

Note that the datasheet of the packaged MOSFET indicates that the junction to case thermal resistance is close to 0.45 K/W if the heat flux is the same on both sides of the device. Thus the thermal resistance of the proposed solution could be lower than 1 K/W for air cooling if bare dies were used.

5. Benchmark

In this section, a theoretical study will be carried out to estimate the potential gains of the TAPIR technology compared with classical approaches in terms of weight and thermal efficiency - the stray inductance and electromagnetic issues will not be studied. The weight includes only the semiconductor parts and the thermal management system (fan + heatsinks). The case study is a three-phase inverter.

5.1. Commercial solutions

The thermal performance of the conventional converter is obtained using the SEMIKRON's online calculation tool "Semisel". The inverter is composed of three SKM50GB12T4 power modules composed of 2 IGBTs and 2 diodes chips. The DC bus voltage is 600V and the output current is 40A. The switching frequency is 15 kHz. The dissipated powers are 96W in each IGBT and 22W in each diode. By using the online tool in the case of air cooling by forced convection, it is found that the transistor junction temperature is 169°C using the P3-180 (0.120 K/W) heatsink with an ambient temperature of 22°C . From the datasheets, the weight of the power module, the heatsink and the fan are respectively 160g, 3100g and 550g. The global weight is thus about **4.1 kg**.

The same calculation has been made with water cooling. In this case, the reference of the cold plate is WP16_280 and the transistor junction temperature is 83°C . The weight of the system is close to **2 kg**.

5.2. Estimation of TAPIR performance

The estimated performance of the TAPIR solution is determined by simulations with FLoTHERM software by considering the same chips as those in the selected SKM50GB12T4 modules.

Figure 13 shows a cross-section of the simulated geometry for an IGBT. It is then possible to distinguish the different interfaces taken into account. The top is the collector and the bottom is the emitter. The pins of the heat sink are replaced by a global heat transfer coefficient.

This heat transfer coefficient is obtained from the heatsink thermal resistance presented in Figure 14 for an air velocity of 5 m/s. The relationship between the thermal

resistance R_{th} of the heatsink and the heat transfer coefficient h is given by Eq. 1.

$$R_{th} = \frac{e}{\lambda \cdot S} + \frac{1}{h \cdot S} \quad \text{Eq. 1}$$

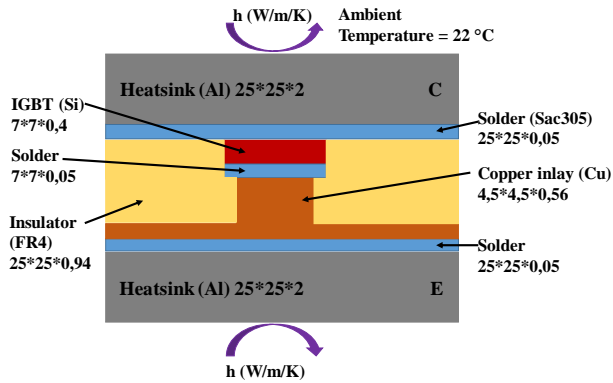


Figure 13 Cross-section simulated for an IGBT

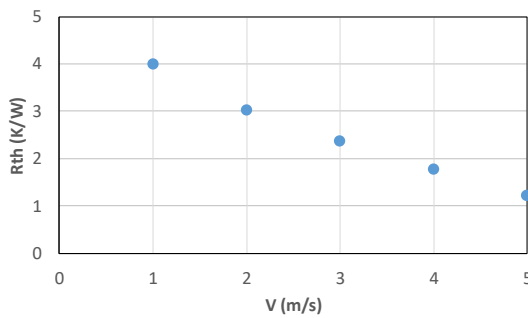


Figure 14 Thermal resistance of the used heatsink as a function of air velocity (ICKS 25*25*18.5)

The TAPIR switching cell is simulated by arranging the semiconductor chips as shown in **Figure 15**. The decoupling capacitor is replaced by FR4 material with a thickness of 2.5mm and a height of 2mm. It is placed between IGBT 1 and Diode 2 and along the assembly (see **Figures 15 and 16**). The losses given by 'Semisel' are used for thermal simulations of the TAPIR phase leg.

Figure 17 shows a 3D schematic of the inverter (semiconductor devices and cooling) considered. One fan is used per arm. By symmetry, the thermal study of the three-phase inverter can be reduced to that of one inverter arm. Note that the power connections from the outside are not represented.

The heat transfer coefficient h applied to the heatsinks is then varied from $500 \text{ W/m}^2/\text{K}$ – 2 m/s air velocity – to $1500 \text{ W/m}^2/\text{K}$ and the average junction temperature of the hottest component is recorded. The simulation shows that the temperature of both IGBT (respectively both diodes) are not the same. This is due to the structure of the assembly and principally to the presence of the decoupling capacitor that reduces the exchange surface (see **Figure 16**). However, the difference is small. It is between 3 and 5°C depending on the applied heat transfer coefficient. For $h=1500 \text{ W}\cdot\text{m}^{-1}\cdot\text{K}^{-1}$, the temperature of IGBTs 1 and 2 are respectively 88°C and 86°C and the temperatures of diodes 1 and 2 are respectively 53°C and 52°C .

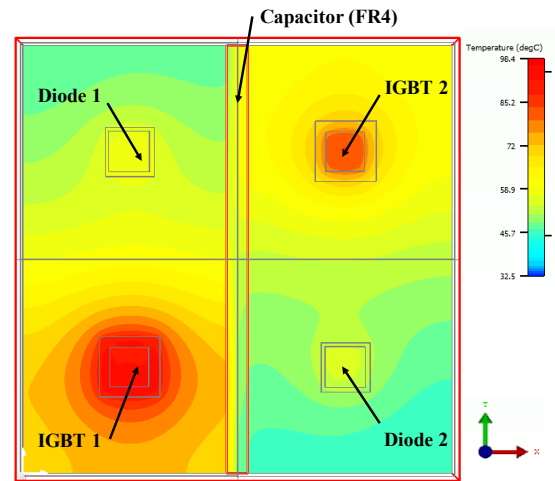


Figure 15 Temperature map in the cross section of the assembly containing the chips ($h=1300 \text{ W/m}^2/\text{K}$)

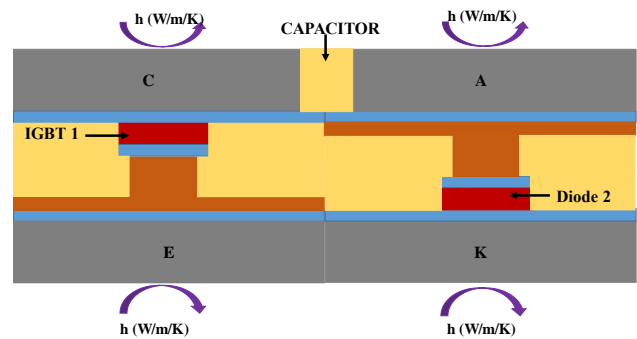


Figure 16 Cross section (along the y-axis) of the simulated switching cell

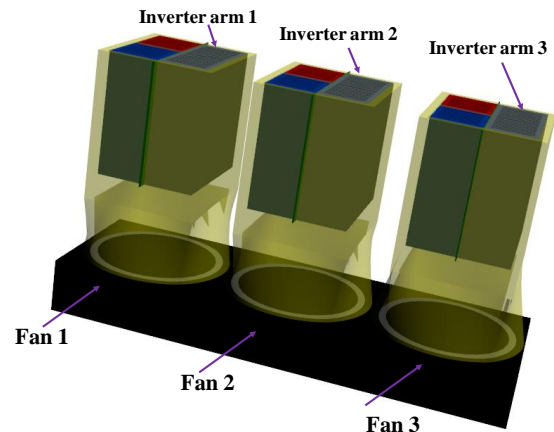


Figure 17 3D diagram of the inverter (semiconductor devices and cooling)

5.3. Comparison

The difference between the junction temperature of the hotter IGBT and the ambient temperature is given in **Figure 18** for the different cases presented above: the commercial solution (air and water-cooling), the TAPIR solution with different heat transfer coefficients. The weight of each solution is also given in this figure. The weight of the TAPIR solution (**0.7 kg**) is estimated by

taking into account the mass of the heat sinks, PCBs containing the components (**Figure 3**), the fan and the plastic box (**Figure 10**). It should be noted that this weight does not include some elements like the busbar.

Concerning the weight of the solution, it can be seen that TAPIR allows for a mass reduction of a **ratio of 5 to 6** compared to the chosen SEMIKRON system with air-cooling. Compared with water cooling (“classical water” in **Figure 18**), the weight reduction is lower (**ratio of 2 to 3**) but it must be mentioned that a complementary heat exchanger and a pump are generally necessary.

Concerning thermal performances, it can be seen that the junction temperature obtained with the TAPIR solution is close to the one obtained with the air-cooled classical solution for lower heat transfer coefficients. For higher heat transfer coefficients, it is very close to the classical water-cooled solution.

However, it must be noted that the Semikron power module is made with an alumina DBC which explains why the thermal performances are limited with water cooling. A simple calculation allows estimating the junction temperature if alumina is replaced by AlN (“classical water DBC AlN” in **Figure 18**). It can thus be seen that water-cooling is the best solution if performant electrical insulators are used but the weight of the cooling system remains higher than the weight of the TAPIR solution.

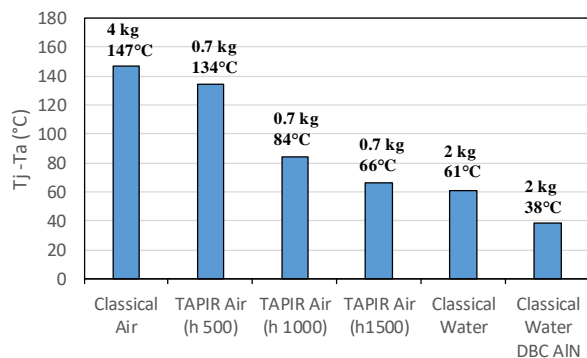


Figure 18 IGBT junction temperature for different cooling technologies.

6. Conclusion

The TAPIR technology was presented and was first implemented in a simple switching cell fabricated with low voltage power MOSFETs. The stray inductance is very low. The measured thermal resistance reflects the cooling performance of this solution. The thermal simulation of a three-phase TAPIR inverter compared to a three-phase inverter made with commercial technologies has shown that TAPIR is more efficient than a conventional air cooling system and reduces drastically the weight. TAPIR's performance is close to that of water-cooling with high (but realistic) heat transfer coefficients. This performance is achieved by reducing the mass of the module and cooling system assembly by a ratio of 3 to 6 depending on the cooling strategy.

The scalability of this technology in terms of power and voltage will be addressed in future works. Regarding the power level, it must be proved that a large number of switching cells could be connected in parallel to provide both a good current sharing between devices and also a good cooling. Regarding the voltage, two different aspects must be studied: prove the possibility of connecting devices in series and design switching cells with high voltage capability.

7. Acknowledgement

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8. Literature

- [1] J. D. van Wyk and F. C. Lee, “On a future for power electronics,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 1, no. 2, pp. 59–72, 2013.
- [2] S. Seal and H. A. Mantooth, “High performance silicon carbide power packaging—past trends, present practices, and future directions”, *Energies*, vol. 10, no. 3, 2017.
- [3] G. Regnat et al., "Optimized power modules for silicon carbide mosfet," in *IEEE Transactions on Industry Applications*, vol. 54, no. 2, pp. 1634-1644, 2018.
- [4] M. Delhommais et al., “Using design by optimization for reducing the weight of a SiC switching cell”, *Energy Conversion Congress and Exposition, ECCE, IEEE* 2016.
- [5] J. Broughton et al., "Review of thermal packaging technologies for automotive power electronics for traction purpose", *Journal of Electronic Packaging*; Vol. 140, n°4, pp. 1-11, 2018.
- [6] O. S. Senturk et al., "Converter structure-based power loss and static thermal modeling of the press-pack IGBT three-level ANPC VSC applied to multi-MW wind turbines", *IEEE Transactions on Industry Applications*, vol. 47, no. 6, pp. 2505-2515, 2011.
- [7] Y. Avenas et al., "Temperature measurement of power semiconductor devices by thermo-sensitive electrical parameters- a review " in *IEEE Transactions on POWER ELECTRONICS*, vol. 27, NO.6, JUNE 2012.
- [8] J.-W. Sofia, “Electrical measurement using semiconductors,” *Electron. Cool*, vol. 3, pp. 22–25, 1997
- [9] B. Thollin, L. Dupont, Z. Khatir, Y. Avenas, J. C. Crebier and P. O. Jeannin, "Partial thermal impedance measurement for die interconnection characterization by a microsecond “pulsed heating curve technique”," *Power Electronics and Applications (EPE), 2013 15th European Conference on, Lille, 2013*, pp. 1-10.