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Wendpanga Fadel Bikinga, Kouceila Alkama, Bachir Mezrag, Jean Michel Guichon, Yvan Avenas. Implementation of TAPIR switching cells with integrated direct air-cooling for SiC power devices. European Conference on Power Electronics and Applications EPE'20, Sep 2020, Lyon, France. 10.23919/EPE20ECCEurope43536.2020.9215620 . hal-03145530

HAL Id: hal-03145530

<https://hal.science/hal-03145530v1>

Submitted on 18 Feb 2021

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Implementation of TAPIR switching cells with integrated direct air-cooling for SiC power devices

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Acknowledgements

The authors would like to thank SATT LINKSIUM for funding the work.

Keywords

«Power module», «3D packaging», «SiC devices», «Thermal management», «Switching cell».

Abstract

This paper presents the design of an SiC switching cell made with the TAPIR technology. Electromagnetic and thermal simulations are carried out in order to analyze the performance of this switching cell. This cell is then compared to commercial power modules and discrete components and exhibits excellent junction to ambient thermal resistance and stray inductance.

Introduction

The energy transition involves a deep change in energy production and consumption patterns and involves an increase in the electrification of systems. According to the U.S. Advanced Research Projects Agency-Energy (ARPA-E) more than 80% of electrical energy in the United States will use static converters by 2030 [1]. Modern power electronics is thus facing a substantial demand on improving efficiency while reducing size and cost of systems for a broad range of areas, including electric vehicles, renewable energies, industrial motors and generators, and distribution grid applications [2]. Size reduction and efficiency of converters have been improved in recent years due to the growth of wide-bandgap semiconductors use [3]. The increase in switching frequency allows reducing the size of passive components and thus obtaining converters with higher power density [4] [5]. However, the packaging of these semiconductors requires special attention due to their high switching speeds [6].

Therefore, the challenges of tomorrow's power electronics designers include improving semiconductor packaging to reduce electrical and electromagnetic disturbances, and optimizing cooling to lighten converters to meet the needs of electric mobility where weight is a significant constraint. Indeed, the weight of the cooling system is generally non-negligible. For example, Delhommis et al. [7] propose a global optimization of a SiC switching cell and show that about 25% of the global weight is due to the heatsink and the fan.

The TAPIR (compact and modular Power modules with Integrated cooling) technology [8] seems to be able to reduce the mass of power modules and cooling systems by a ratio of 3 to 5 by distributing the heat sources (chips) in the volume of the heatsink. Contrarily to most researches on double side cooling [1], the heat extraction is made by air-cooling and the heatsinks are used as electrodes as it is the case with press-pack power converters [9] or Power Chip on Bus (PCoB) modules [10]. TAPIR technology consists in sandwiching vertical semiconductor components between two heat sinks. Then two sandwiches and a decoupling capacitor are assembled to make a low voltage-switching cell as shown in

Fig. 1. Finally, the global power module is made by assembling several switching cells together. An example of a 4-phase converter is given in [8].

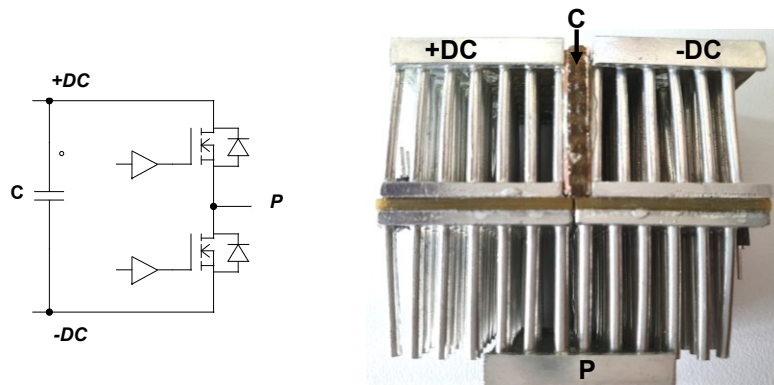


Fig. 1: TAPIR low voltage Switching cell

In [8], two packaged 60V-100A power MOSFETs are implemented in a switching cell that is characterized using the double pulse method. The parasitic inductance of the switching loop is less than 2 nH. Also the thermal behavior is estimated using thermo-sensitive electrical parameters. The measured junction to ambient thermal resistance is close to 1.30 K/W. The coupling thermal resistance is relatively low and limited to 0.2 K/W. However, the junction-to-ambient thermal resistance can be further reduced by using bare chips and improving the heat sink as proposed by Xu et al. [10]. In this reference, the authors propose a sandwich similar to the one of the TAPIR method and including SiC devices with a junction-to-ambient thermal resistance of only 0.5 °C/W.

The aim of the present paper is to propose an implementation of the TAPIR technology on a high voltage SiC switching cell. The goal is to analyze the electromagnetic and thermal performances of the cell and compare it to commercially available power modules and discrete components. The implementation of the SiC switching cell is presented, followed by electromagnetic and thermal simulations. Before concluding, a comparison will be made with commercially available components.

Implementation of an SiC switching cell

SiC MOSFETs CPM2_1200_0080b (1200V-36A, $R_{DSon}=80m\Omega$) from CREE company were used to build a switching cell. A 4-layer printed circuit board (PCB) has been designed to connect the MOSFET to the gate drive circuit but also to ensure a connection of the die to the heatsinks with few thermal interfaces (Fig. 2 and 3).

In Fig. 3, it can be seen that the source and gate pads of the chip are soldered on PCB layer 2. For this purpose, a nickel-gold coating has been made on the gate and source metallizations. Beneath the two source electrodes of the chip, a copper inlay is inserted between layer 2 and layer 4. Layer 1 is cut so that the Drain is accessible from the PCB surface through a hole (Fig. 2 and 3).

This implementation has several advantages in terms of thermal management:

- one heatsink can be directly connected to the drain of the chip,
- the number of thermal interfaces between the source metallization and the other heatsink is relatively low.

The gate drive circuit (buffer) is located on layer 4 of the PCB and vias provide electrical connections between the control signals and the chip. Layer 1 is thin (35 μ m) to minimize the distance between the chip and the top of the PCB in order to have the thinnest soldering thickness and ensure good electrical and thermal conductions. Layer 3 is used to connect the gate to the driver circuit avoiding the guard rings. Vias connecting the source are located on either side of the gate track. This minimizes the inductance of the gate circuit and creates electromagnetic shielding of the gate. Layer 4 thickness is 120 μ m for allowing heat spreading of the heat flux and thus reducing the thermal resistance of the solder between the PCB and the heatsink.

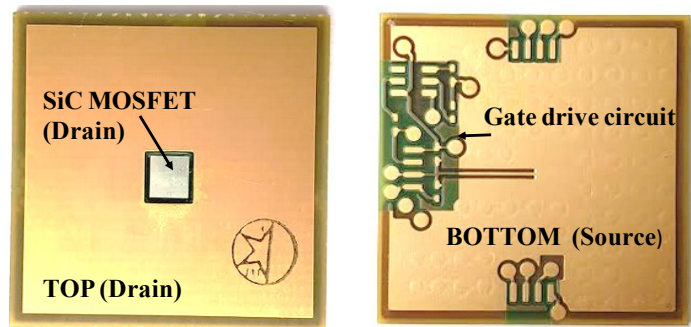


Fig. 2: PCB for SiC MOSFETs

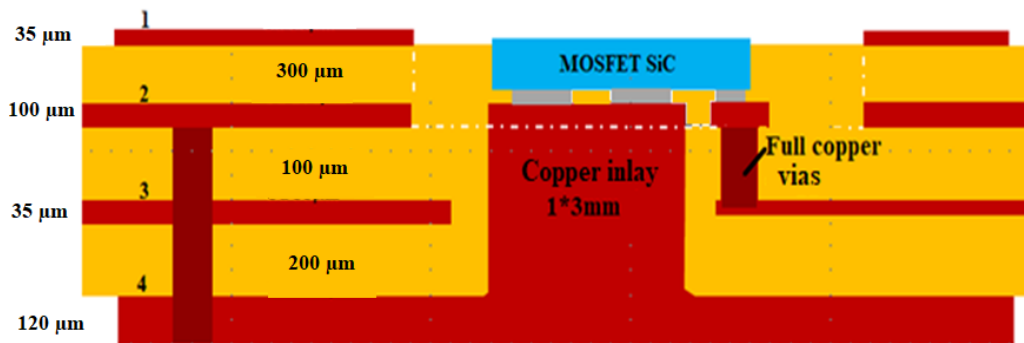


Fig. 3: Architecture of the PCB

To make the switching cell, the heatsinks are cut (Fig. 4) to avoid any electrical contact with the components of the gate control circuit on the PCB board. The thickest component is the gate driver which has a height lower than 2 mm. This choice is made in order not to degrade too much the thermal performances by improving the electromagnetic one. Note that a gate driver chip could be directly integrated inside the PCB to simplify the assembly but the technological process is not done already.

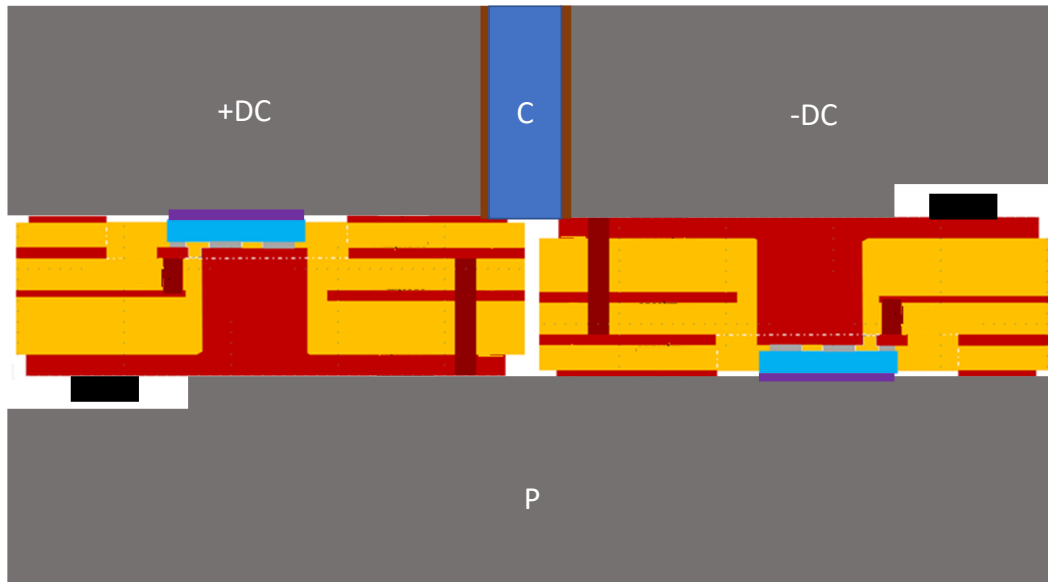


Fig. 4: SiC Switching cell

Once the switching cell is presented, electromagnetic simulations will be proposed to estimate the parasitic inductance of the switching loop, then thermal simulations will be carried out to analyse the thermal performances of this assembly.

Stray inductance of the SiC switching cell

Electromagnetic simulations are carried out with Flux3D software based on the finite element method. Indeed, the PEEC method that is usually used for evaluating power electronics packages is not adapted to the TAPIR geometry that does not include any thin electrical conductors like it is the case in classical power modules. The MIPSE software still under development at G2Elab which uses integral methods [11] is also used here to visualize the distribution of the current density in order to refine the mesh on Flux3D, but also to confirm the result obtained with Flux3D.

In Flux3D, a magneto-harmonic application at a frequency of 100 MHz is used. The simulation is done at this frequency because the equivalent frequency measured in [8] was about 100MHz. The decoupling capacitor is replaced by a current source of 1A injected on the surface over a thickness of 2mm (see Fig. 5). This consideration was made after having noted that during switching time only the lower part of the capacitor injects current in the structure (see Fig. 4). The voltage is measured across the current injection areas and the stray inductance is deduced. The capacitive effects are not included in this simulation.

The simulated geometry is shown in Fig. 5. The chip (3mm*3mm*0.35 mm) is assumed to be directly attached to the heatsinks, as well as the copper inserts (3mm *1mm*0.4mm). Only one internal layer is considered in this simulation because adding the second one does not change much the result. This inner layer is not connected to the copper inlay as can be seen on the PCB architecture in Fig. 3. The micro vias that link the inner layers to the source potential are represented as two bars.

All components of the switching cell are assumed to be made of aluminum of resistivity $2.68E-8 \Omega.m$. This approximation is valid since the size of the chips and inserts is small compared to that of the heatsinks.

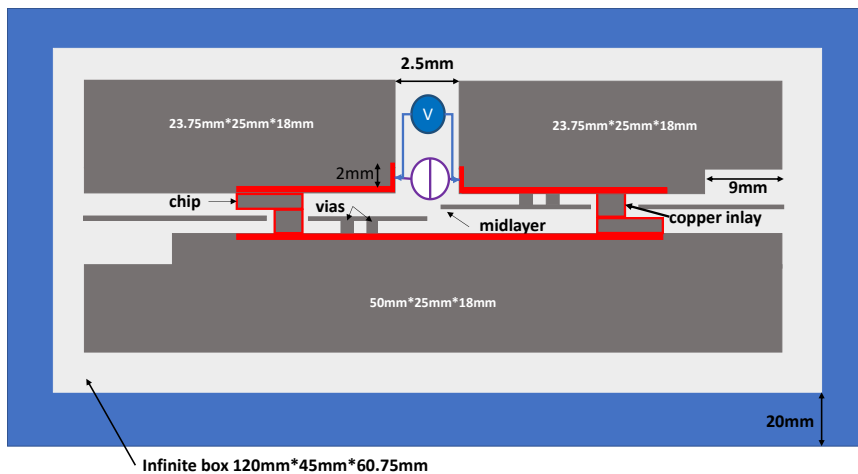


Fig. 5: Simulated switching cell geometry

For applying boundary conditions, an infinite box is used. Its dimension is twice the size of the device to be tested as recommended in the software documentation. The thickness of the infinite box is 20mm. Simulations have been performed to analyze the impact of increasing the size of the infinite box. This has almost no influence on the results.

As in any finite element resolution, the quality of the mesh has an impact on the veracity of the results. For this purpose, it is necessary to know which is the main current path and thus to adapt the mesh by decreasing the elements size in critical areas. Several simulations have been done with Flux3D and MIPSE softwares to determine the current path at the proposed frequency. Fig. 6 shows the distribution of the current density in logarithmic form obtained after simulation on MIPSE. It can be seen that the current flows mainly on the edges (skin effect) of the heatsinks and in the semiconductor chips and copper inlay. The mesh is densified at these places by adding 100 μ m plates shown in red in Fig. 5, so

as to have at least two meshes in the skin thickness which is about $60\mu\text{m}$. The mesh creates more than 500,000 1st order volume elements.

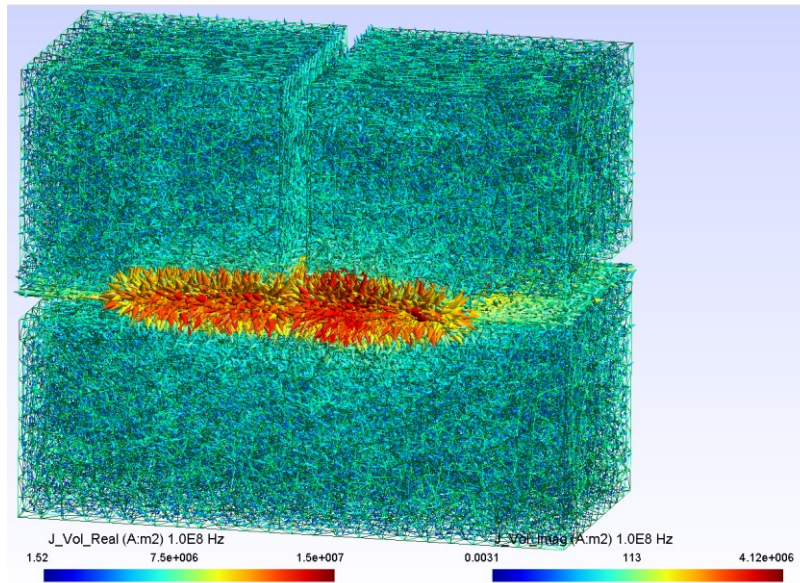


Fig. 6: Current path in the switching cell

The parasitic inductance obtained after simulation with Flux3D is 1.41nH . To carry out the simulation with MIPSE, the appropriate mesh is exported from Flux3D. The application is always magneto-harmonic and the injected current is 1A . The elements here are assumed to be in copper simply because that is the only available conductive material. This time the parasitic inductance obtained is 1.38nH that confirms the value obtained with Flux3D. Note that the simulation time is largely decreased using MIPSE compared with Flux3D, it will allow optimizing the geometry in the future.

The parasitic inductance of the simulated SiC cell is thus less than 1.5 nH while the parasitic inductance measured in [8] is 2nH . This is explained by the fact that in [8] the MOSFETs are packaged and thus the PCB is thicker that increases the stray inductance of the assembly.

The SiC switching cell shows the advantages that were expected from an electromagnetic point of view. The thermal behavior will now be studied.

Thermal behavior of the SiC switching cell

Thermal simulations are performed to estimate the junction to ambient thermal resistance of a MOSFET and the thermal coupling that would exist between the two MOSFETs of the switching cell. They are carried out with the Flotherm software. The simulated architecture is shown in Fig. 7 and Fig. 8. This assembly is fairly representative of the actual switching cell. The solder thickness of $200\mu\text{m}$ between the heatsink and the drain of the chip (fig. 7) is present in practice due to a too large margin taken by the subcontractor (CIBEL) in order to avoid the breakdown of the chip during the PCB fabrication. This thickness will be considerably reduced in the next phases of production. Contact resistances are not considered in these simulations. The thermal conductivity of the different materials used for the simulation are shown in Table I. The heat transfer coefficient varies between 500 and $1500\text{ W.m}^{-2}\cdot\text{K}^{-1}$, these values are estimated from heat sink datasheets [8]. The dissipated power is 50W in MOS1 and 0W in MOS2. The average temperature of both MOSFETs is measured to determine the junction to ambient thermal resistance of MOS1 and the coupling thermal resistance between MOS1 and MOS2. The results are shown in Fig. 9.

Then MOS2 dissipates 50W and the other 0W to check if the heat is extracted in the same way. The thermal resistance value is slightly lower than that of the MOS1 and is 1.38K/W for a heat transfer

coefficient of $1500 \text{ W.m}^{-2} \cdot \text{K}^{-1}$ instead of 1.46 K/W for MOS1. The coupling remains the same 0.074 K/W .

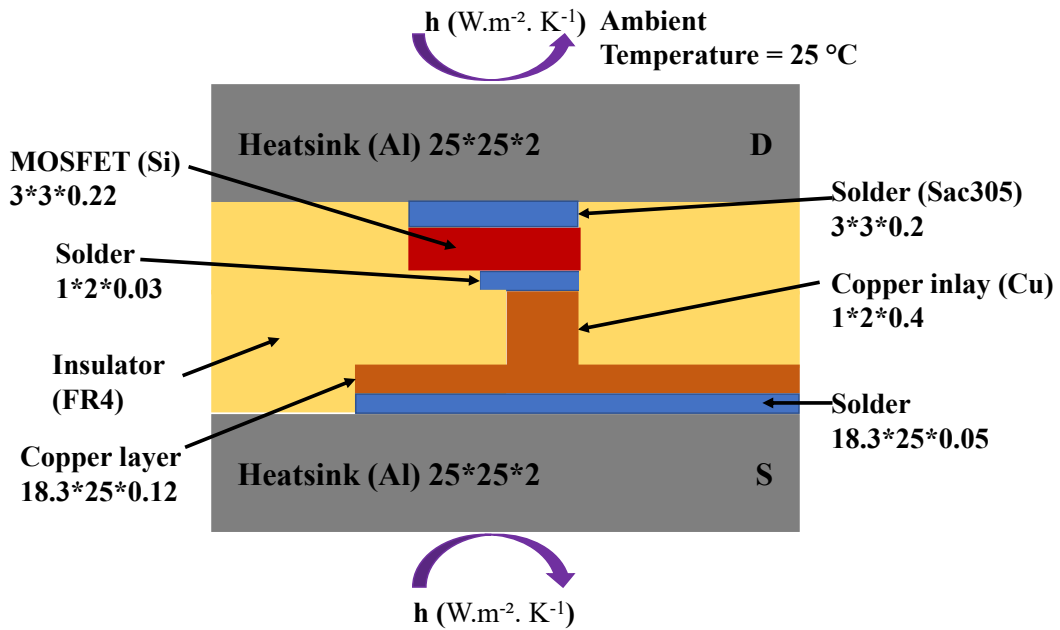


Fig. 7: Cross-section simulated for one MOSFET (dimensions are given in mm)

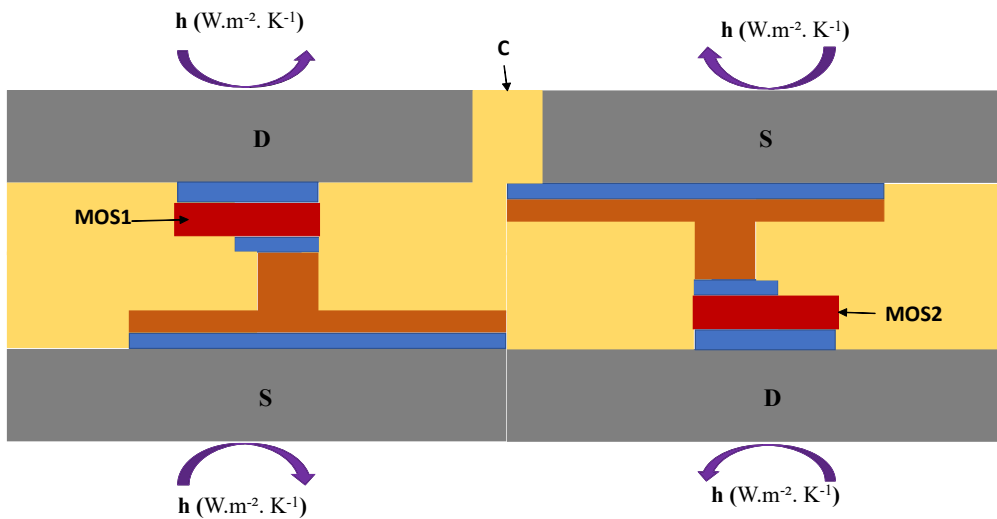


Fig. 8: Cross-section of the simulated switching cell

Table I: Thermal conductivity of materials

| Material | Thermal conductivity $\text{W.m}^{-1} \cdot \text{K}^{-1}$ |
|-----------------|---|
| Aluminum | 201 |
| SiC | 350 |
| Copper | 385 |
| Solder (SAC305) | 58.7 |
| FR4 | 0.5 |

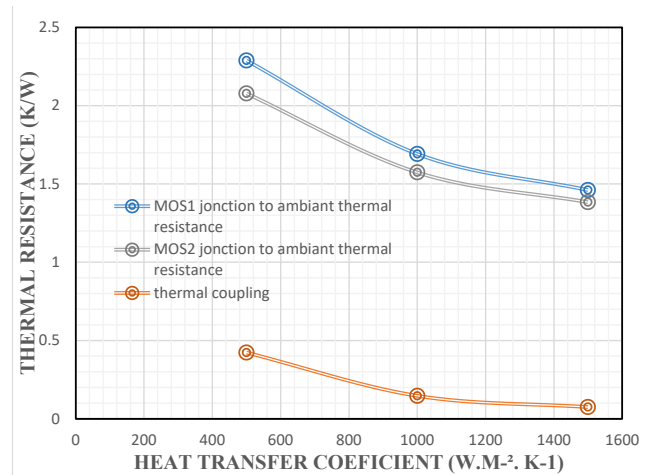


Fig. 9: Junction to ambient thermal resistance and thermal coupling as a function of the heat transfer coefficient

It is then interesting to analyze the temperature map inside the assembly to understand what can be done to improve its thermal behavior. For that purpose, Fig. 10 presents the evolution of the temperature along two paths: the first is perpendicular to the chip surface and crosses its center, the second is also perpendicular to the chip but crosses the center of the copper inlay. First it can be observed that the temperature is not uniform in the chip, the temperature being largely higher at the chip center than at the inlay center. It is something usual but that is accentuated here by the non-uniform dissipation area on the source side of the device. It is also observed that the temperature drop in the inlay is relatively high. It is due to its small cross section compared to the chip surface area. This problem induces a non-symmetrical heat flux diffusion inside the assembly: using Flotherm, it is estimated that about 2/3 of the total dissipated heat flows through the top heat sink (Φ_D in the figure) and thus only 1/3 of the remaining heat goes through the bottom heat sink (Φ_S in the figure). Therefore, a good way to improve the global thermal behavior should be to propose a solution for increasing the average cross section of the copper inlay to obtain a better heat repartition between the two faces of the chip.

Also, it is observed that there are large temperature drops in the heat sink base plates and between these base plates and the ambient temperature. This is the reason why the temperature evolution inside the assembly using a copper base plate was also shown. It can be clearly seen that the better thermal conductivity induces a lower temperature gradient and a better heat spreading (the temperature at the base plate surface is decreased). The last way to improve the thermal behavior would be to use a more performant heat sink to increase the global heat transfer coefficient.

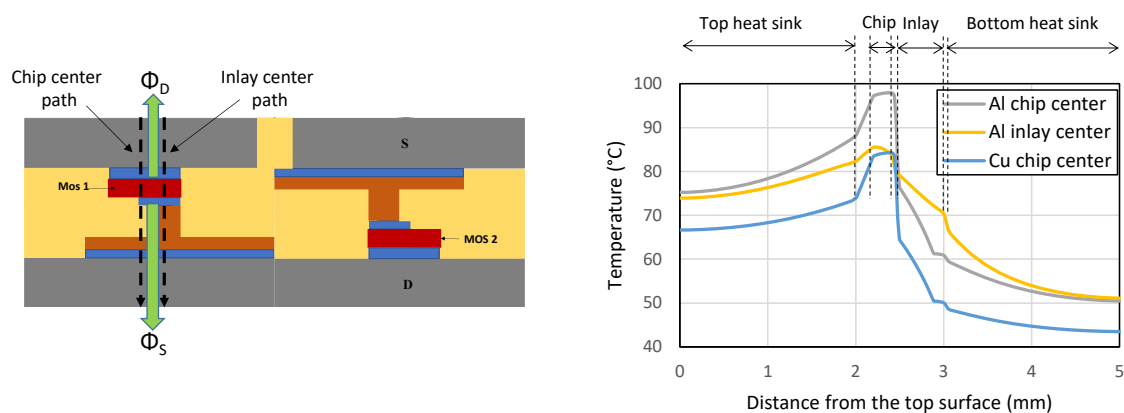


Fig. 10: Temperature evolution inside the assembly (dissipated power in MOS1 50W, $h=1500 \text{ W.m}^{-2} \cdot \text{K}^{-1}$ and ambient temperature 25°C)

The thermal performances obtained are those expected. However, it would be possible to optimize the heatsink in order to have higher heat transfer coefficients and therefore a lower junction-to-ambient thermal resistance. The TAPIR SiC switching cell will then be compared with commercially available discrete SiC power modules and discrete components.

Benchmark of TAPIR SiC switching cell with commercially available power modules and discrete components

For this comparison power modules and discrete components using 1200V-80mΩ MOSFET SiC devices are chosen. It is obvious that the thermal resistance depends on the size of the devices and on the number of paralleled chips but it can even give first ideas on the performance of the proposed package. Data are given in Table II.

Considering the stray inductance parameter, the TAPIR switching cell exhibits very interesting performances (1.5 nH) compared with classical power modules [12] and circuits using discrete devices with global stray inductances that are higher than 10 nH. Today commercial power modules are improved, by including decoupling capacitors for example [13], but such a low stray inductance is not reported. Note that if N devices are put in parallel in the TAPIR technology, the stray inductance is divided by N which is hardly obtained when implementing 2D packages.

Considering thermal aspects, it can be seen that the junction to ambient thermal resistance of the TAPIR switching cell is close to the junction to sink thermal resistance of power modules. That proves its very good thermal behavior. The use of better ceramic materials in power modules could reduce their thermal resistances but it has also to be noted that the thermal resistance of the TAPIR switching cell could be largely reduced by implementing better heat sinks. It was proved by Xu et al. [10] that obtained a junction to ambient thermal resistance of 0.5 K.W⁻¹ with a geometry close to the TAPIR one. Finally, it is important to mention that the coupling thermal resistance of the TAPIR technology is very low especially when the heat transfer coefficient is high because the cooling is made at chip level. In the case of power modules, a thermal coupling exists through the power module substrate but also through the heat sink that induces more important values. For example, in [15], the thermal coupling resistance between devices was until 25 % of the junction to ambient thermal resistance using water cooling.

Table II: Electromagnetic and thermal performances benchmark

| Components | Package | Stray inductance | Thermal resistance |
|---|--------------|--|---|
| TAPIR SiC Switching cell | | $L_s = 1.5 \text{ nH}$ | $R_{th(j-a)} = 1.4 \text{ K/W @ } h=1500 \text{ W.m}^{-2}. \text{ K}$ $R_{th(j-a)} = 2.3 \text{ K/W @ } h=500 \text{ W.m}^{-2}. \text{ K}$ |
| SK25MH120SCTp, SEMIKRON [12] | Power module | $L_s = 18 \text{ nH}$ | $R_{th(j-s)} = 1.52 \text{ K/W}$ |
| 10-PZ126PA080ME-M909F18Y Vincotech [13] | Power module | Not provided but includes a decoupling capacitor | $R_{th(j-s)} = 1.79 \text{ K/W}$ |
| C2M0080120D, CREE ([14]) | TO247 | Depends on the PCB layout (> 10 nH) | $R_{th(j-c)} = 0.65 \text{ K/W}$ |

Conclusion

An SiC switching cell was designed and the structure of the related PCB was presented. The results obtained from the electromagnetic simulations show the quality of the switching loop and therefore makes this technology suitable for wideband gap components. The TAPIR SiC switching cell has also

been evaluated from a thermal point of view. It has been seen that this technology is more efficient than those currently on the market. The TAPIR solution has a junction to ambient thermal resistance close to the junction to sink thermal resistance of some modules. The next step will therefore be to electrically and thermally characterize the SiC switching cell. The breakdown voltage, the common mode perturbations and the assembly of several switching cells to make a more complex topology will also be specific points to be addressed in the future.

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