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# Extraction of Access Parasitics of Packaged GaN Power Transistors Using S-Parameters

L. Pace, N. Defrance, A. Videt, N. Idir, J.-C. De Jaeger and V. Avramovic

**Abstract**—In order to better predict the high frequency switching operation of transistors in power converters, the access elements of these devices like resistances and inductances must be accurately evaluated. This paper reports on the characterization of a gallium nitride (GaN) packaged power transistor using S-parameters in order to extract the parasitics stemming from ohmic contacts and packaging. As the transistor is encapsulated, a calibration technique is set using specific test fixtures designed on FR4 printed circuit board (PCB) in order to get the S-parameter in the transistor plane from the measured ones. The proposed method is based a modified “Cold FET” technique and off-state measurements. It is applied to a commercially-available enhancement mode GaN HEMT (High Electron Mobility Transistor). The extracted parasitic elements are compared to reference values given by the devices manufacturers. The impact of junction temperature on drain and source resistances is also evaluated. Finally, an electrothermal model of these parasitics is proposed.

**Index Terms**—Access resistances, access inductances, S-parameters, GaN, power transistors, temperature

## I. INTRODUCTION

Gallium nitride (GaN) power transistors constitute an enabling technology for efficient power conversion at switching frequencies higher than the megahertz range. However, their very low switching times (a few nanoseconds) make them very sensitive to any circuit parasitic elements, such as resistances or inductances. Thus, in order to accurately simulate the transistor behavior in power converters and estimate the power losses, it is of great interest to accurately determine the values of these access parasitics.

According to [1], simulation based on finite-element analysis (FEA) is a way to estimate the parasitics of packaged transistors. However this method requires internal topologies and other technological data that only devices manufacturers own. S-parameters, measured by a vectorial network analyzer (VNA), have shown their potential to extract transistors access elements as well as intrinsic small-signal equivalent circuit [2]-[9].

While access resistances play an important role in degrading high-frequency operation of GaN HEMTs [10], they potentially

add charging and discharging delays during switchings in high-frequency power converters. Furthermore, source and drain parasitic resistances are a major part of on-state resistance. Therefore these values must be known with a good accuracy in order to estimate power losses and also must be well separated from channel resistance in order to get a good modeling of the drain current sources. Several works, mainly performed on unpackaged transistors, are based on S-parameters to extract the access resistance values and their temperature dependency [3]-[6].

Fast switching performance of GaN power transistors is critically determined by the values of parasitic inductances. Negative effects of these elements like voltage overvoltages and oscillations occur during switching transitions [1]. Recent works use S-parameter measurements to extract the access inductances of silicon carbide (SiC) power modules or TO packages [7], [8]. Authors show the potential of S-parameters to extract a few nanohenry values. However, the source and drain inductances of new GaN power transistors packaging have values under the nanohenry range and still remain challenging to measure.

This work reports a methodology to extract access resistances and inductances of packaged GaN power transistors. The use of S-parameter measurements in “Cold FET” [11] and off-state conditions is proposed. First, the commercially available GaN switch used in this work as well as the characterization fixture are presented in Section II. Then, the calibration process of the test fixture is detailed as well. Section III and IV present the results of the access resistances extraction. The temperature dependency is obtained by on-state measurements, also called “Hot FET” conditions. Finally, section V describes results of the parasitic inductances extraction. Obtained values are compared with reference values provided by devices manufacturers.

## II. CALIBRATION PROCEDURE FOR S-PARAMETERS CHARACTERIZATION

In this work, the study is based on the characterization of a commercially available GaN HEMT transistor. It is a normally-off device dedicated to high frequency power conversion applications. The switch is the GS66502B from GaN Systems.

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This transistor is a 650V-7.5A Enhancement-Mode GaN HEMT [12] with GaNPX® packaging [13]. The lumped-element equivalent circuit of its extrinsic part is given in Fig. 1, where  $R_G, L_G, R_D, L_D, R_S$  and  $L_S$  are the access resistances and inductances.

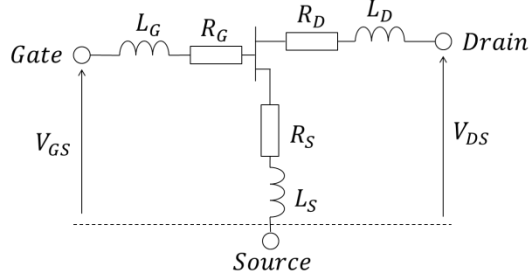


Fig. 1. Lumped-element equivalent circuit of the transistor with parasitics

As the device is packaged and not suitable for direct coaxial measurements using a VNA, the development of specific characterization fixtures is required. Testing printed circuit boards were designed in 1.6 mm FR4 epoxy as shown in Fig. 2(a). It is constituted of 50Ω-coplanar grounded transmission lines to bring into contact the Device Under Test (DUT) to coaxial SMA connectors and avoid high frequency reflections during measurements. The transmission line connected to the source is also connected to ground plane. This source connection allows a symmetric calibration at each transistors terminals and avoids calibration errors caused by ground plane parasitics. Fig. 2(b) shows the equivalent circuit of the system presented in Fig. 2(a) with different impedances and admittances added by the characterization setup.

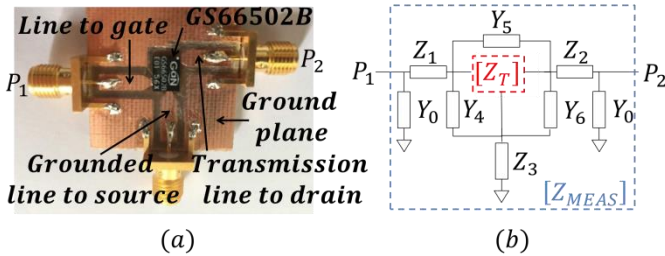


Fig. 2. (a) characterization fixture for the transistor GS66502B (b) equivalent circuit of the characterization fixture

$[Z_{MEAS}]$  is the impedance matrix measured by the VNA and  $[Z_T]$  is the impedance matrix of the transistor. In order to get the matrix  $[Z_T]$  from  $[Z_{MEAS}]$ , a measurement calibration is required. Several calibration techniques have already been proposed [14], [15]. They are mostly adapted to on-wafer measurement and require an accurate knowledge of the calibration standards. A new calibration method based on measurement setup equivalent circuit is proposed in this work. The objective of the following calibration method is to obtain the matrix  $[Z_T]$  from  $[Z_{MEAS}]$  using the calibration standards presented in Fig. 3.

In the equivalent circuit,  $Y_0$  represents the coupling between transmission line and ground plane. It is determined by performing a 1-port S-parameter measurements on the “OPEN-1P” calibration standard presented in Fig. 3 as shown by the equivalent circuit in Fig. 4. Thus,  $Y_0$  is given by (1):

$$Y_0 = \frac{1 - S_{11_{OPEN-1P}}}{(1 + S_{11_{OPEN-1P}})Z_0}, \quad \text{with } Z_0 = 50\Omega \quad (1)$$

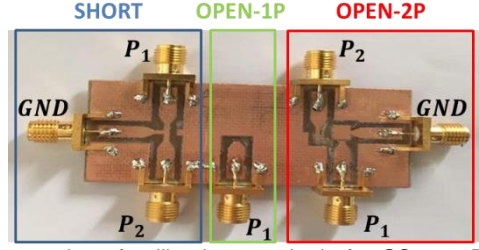


Fig. 3. Presentation of calibration standards for GS66502B transistor characterization

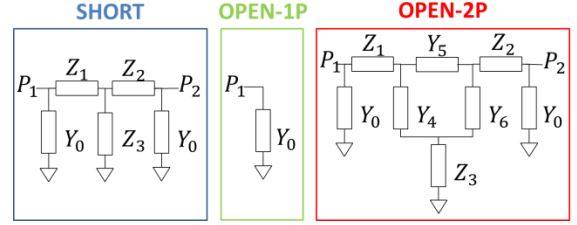


Fig. 4. Equivalent circuits of the characterization standards

The impedances  $Z_1, Z_2, Z_3$  are the transmission lines impedances and are determined from a 2-port S-parameter measurements on the “SHORT” standard presented in Fig. 3 as shown by its equivalent circuit in Fig. 4.  $Z_1, Z_2, Z_3$  are obtained using the procedure given by (2) to (6):

$$[S_{SHORT}] \rightarrow [Y_{SHORT}] \quad (2)$$

$$\begin{bmatrix} Y_{11_{SHORT}} - Y_0 & Y_{12_{SHORT}} \\ Y_{21_{SHORT}} & Y_{22_{SHORT}} - Y_0 \end{bmatrix} \rightarrow [Z_{SHORT}] \quad (3)$$

$$Z_1 = Z_{11_{SHORT}} - Z_{12_{SHORT}} \quad (4)$$

$$Z_2 = Z_{22_{SHORT}} - Z_{12_{SHORT}} \quad (5)$$

$$Z_3 = Z_{12_{SHORT}} \quad (6)$$

Where  $\rightarrow$  represents a matrix conversion.

Admittances  $Y_4, Y_5, Y_6$  represent the capacitive couplings between lines and are obtained from a 2-port S-parameter measurements on the “OPEN-2P” calibration standard presented in Fig. 3. According to its equivalent circuit given in Fig. 4.  $Y_4, Y_5, Y_6$  are obtained from the procedure given by (7) to (12):

$$[S_{OPEN-2P}] \rightarrow [Y_{OPEN-2P}] \quad (7)$$

$$\begin{bmatrix} Y_{11_{OPEN-2P}} - Y_0 & Y_{12_{OPEN-2P}} \\ Y_{21_{OPEN-2P}} & Y_{22_{OPEN-2P}} - Y_0 \end{bmatrix} \rightarrow [Z_{OPEN-2P}] \quad (8)$$

$$\begin{bmatrix} Z_{11_{OPEN-2P}} - Z_1 - Z_3 & Z_{12_{OPEN-2P}} - Z_3 \\ Z_{21_{OPEN-2P}} - Z_3 & Z_{22_{OPEN-2P}} - Z_2 - Z_3 \end{bmatrix} \rightarrow [Y_{OPEN-2P*}] \quad (9)$$

$$Y_4 = Y_{11_{OPEN-2P*}} + Y_{12_{OPEN-2P*}} \quad (10)$$

$$Y_5 = -Y_{12_{OPEN-2P^*}} \quad (11)$$

$$Y_6 = Y_{22_{OPEN-2P^*}} + Y_{12_{OPEN-2P^*}} \quad (12)$$

Finally, the mathematical procedure given by (13) to (16) enables to get the impedance matrix of the transistor  $[Z_T]$  from the measured S-parameter matrix  $[S_{MEAS}]$ .

$$[S_{MEAS}] \rightarrow [Y_{MEAS}] \quad (13)$$

$$\begin{bmatrix} Y_{11_{MEAS}} - Y_0 & Y_{12_{MEAS}} \\ Y_{21_{MEAS}} & Y_{22_{MEAS}} - Y_0 \end{bmatrix} \rightarrow [Z_{MEAS}] \quad (14)$$

$$\begin{bmatrix} Z_{11_{MEAS}} - Z_1 - Z_3 & Z_{12_{MEAS}} - Z_3 \\ Z_{21_{MEAS}} - Z_3 & Z_{22_{MEAS}} - Z_2 - Z_3 \end{bmatrix} \rightarrow [Y_{MEAS^*}] \quad (15)$$

$$\begin{bmatrix} Y_{11_{MEAS^*}} - Y_4 - Y_5 & Y_{12_{MEAS^*}} - Y_5 \\ Y_{21_{MEAS^*}} - Y_5 & Y_{22_{MEAS^*}} - Y_6 - Y_5 \end{bmatrix} \rightarrow [Z_T] \quad (16)$$

Once the  $[Z_T]$  matrix is known, knowing the equivalent scheme of the transistor for a specific gate and drain biases condition, parameters of the transistor equivalent circuit can be determined. The complete procedure to extract all parasitic elements of the device will be detailed in the section III to V.

### III. EXTRACTION OF THE ACCESS RESISTANCES

The method proposed in this work to extract access resistances of packaged GaN transistors is based on the ‘‘Cold FET’’ technique [11]. In this method, the drain of the transistor is shorted with the source, which is connected to ground reference ( $V_{DS} = 0V$ ). The gate is biased at a voltage higher than the threshold voltage, involving that the channel is open (conducting). The part of the channel located under the gate has its own resistance named  $R_{ch}$ . A schematic representation of the transistor in Cold FET conditions and its equivalent circuit are given in Fig. 6.

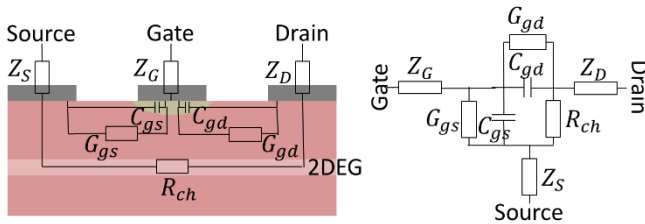


Fig.6. Schematic representation of a GaN transistor in Cold FET conditions and its equivalent circuit

In Fig. 6,  $Z_G, Z_D, Z_S$  are the access elements located at the gate, drain and source respectively as given by (17) to (19).  $C_{gs}$  and  $C_{gd}$  represent the gate capacitances.  $G_{gs}$  and  $G_{gd}$  are the gate diodes conductance. Additionally,

$$Z_G = R_G + j.L_G.\omega \quad (17)$$

$$Z_D = R_D + j.L_D.\omega \quad (18)$$

$$Z_S = R_S + j.L_S.\omega \quad (19)$$

Up to 100 MHz at least, the channel resistance  $R_{ch}$  is considered to be low compared to the gate capacitances and conductance corresponding impedances. This hypothesis will be reinforced by experimental results. Therefore, the equivalent circuit presented in Fig. 6. can be simplified to the T-structure shown in Fig. 7.

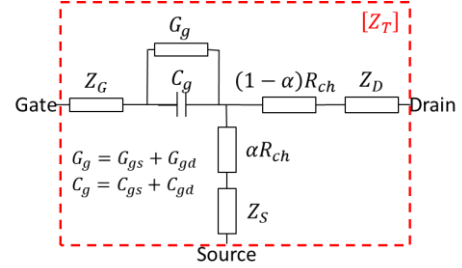


Fig.7. Simplified equivalent circuit in Cold FET up to 100 MHz

According to Fig. 7,  $\alpha$  represents the fraction of  $R_{ch}$  located between gate and source and the real part of the impedance ( $Z_{11T} - Z_{12T}$ ) is given by equation (20). At high frequency, it is then possible to deduce the value of the gate resistance  $R_G$ .

$$Re(Z_{11T} - Z_{12T}) = R_G + \frac{G_g}{G_g^2 + C_g^2 \omega^2} \quad (20)$$

The evolution of  $Re(Z_{11T} - Z_{12T})$  versus frequency between 1 and 100 MHz is shown in Fig. 8 at  $V_{GS} = 6V$ . The calibration of the VNA is performed from 300 kHz to 1 GHz. Then, the calibration method presented in section II is done in order to get the transistor impedance matrix  $[Z_T]$ .

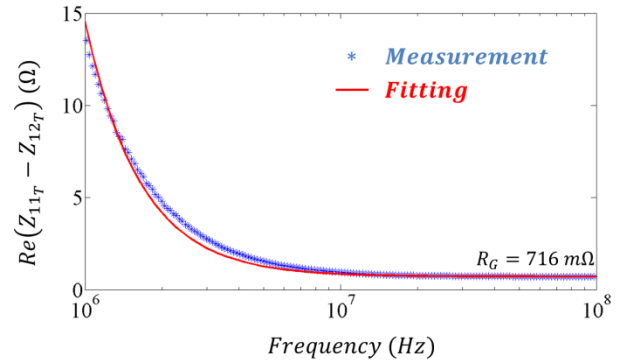


Fig.8.  $Re(Z_{11T} - Z_{12T})$  vs. frequency at  $V_{GS} = 6V$  and fitting results

By fitting the experimental data presented in Fig. 8 with equation (20), the extracted value of  $R_G$  is 716 m $\Omega$  compared with 1.5  $\Omega$  given in the manufacturer’s model. Fitting parameters are summarized in Table 1. It can be noted that this method not only gives the gate resistance value but also the gate diodes conductance and capacitance for a given  $V_{GS}$ .

TABLE I  
FITTING PARAMETERS OF FIG. 8.

$R_G$ (m $\Omega$ )	$G_g$ ( $\mu\Omega^{-1}$ )	$C_g$ (pF)
716	22.8	204

According to Fig. 7, the real part of impedances  $Z_{12T}$  and  $Z_{22T}$  are given by (21) and (22) [16] :

$$\text{Re}(Z_{12T}) = R_S + \alpha \cdot R_{ch} \quad (21)$$

$$\text{Re}(Z_{22T}) = R_D + R_S + R_{ch} \quad (22)$$

A relation linking  $\text{Re}(Z_{22T})$  to the gate voltage  $V_{GS}$  is given by authors in [17]. In our study, it is proposed to generalize this relation to  $\text{Re}(Z_{12T})$ . Therefore relations given by (23) and (24) are considered in this work.

$$\text{Re}(Z_{12T}) = R_S + \frac{1}{K_1(V_{GS}-V_t)} \quad (23)$$

$$\text{Re}(Z_{22T}) = R_D + R_S + \frac{1}{K_2(V_{GS}-V_t)} \quad (24)$$

Where  $V_t$  is the threshold voltage and  $K_1$ ,  $K_2$  are constant coefficient depending on full channel conductance, threshold and built-in voltages [17].

S-parameter measurements were performed on the transistor for different  $V_{GS}$  from 2V to 6V. Fig. 9 and Fig. 10 show the real parts of impedances  $Z_{12T}$  and  $Z_{22T}$  for different  $V_{GS}$ , from 1 MHz to 100 MHz. In order to avoid errors due to high frequency effects, average impedance values in the flat region of the curves (between 1 MHz and 10 MHz) are determined and plotted as functions of  $V_{GS}$  in Fig. 11 and equations (23) and (24) are used to fit the experimental results. The fitting parameters are given in Table II. The values of 158 m $\Omega$  and 14.1 m $\Omega$  are found for  $R_D$  and  $R_S$  respectively compared to 180 m $\Omega$  and 10 m $\Omega$  given in manufacturer's model at 25°C.

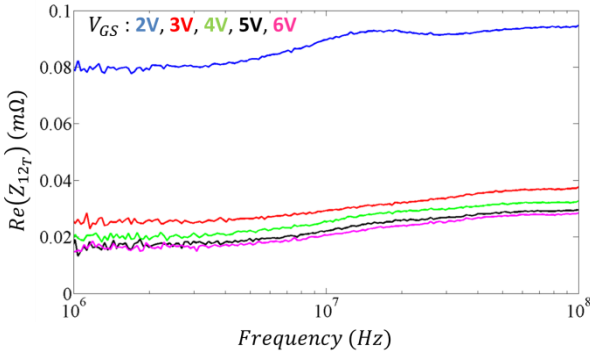


Fig.9.  $\text{Re}(Z_{12T})$  vs. frequency at different  $V_{GS}$

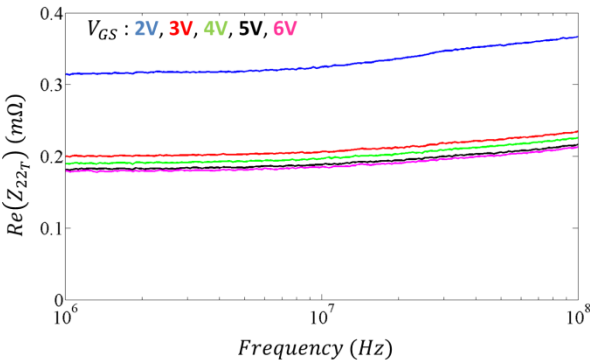


Fig.10.  $\text{Re}(Z_{22T})$  vs. frequency at different  $V_{GS}$

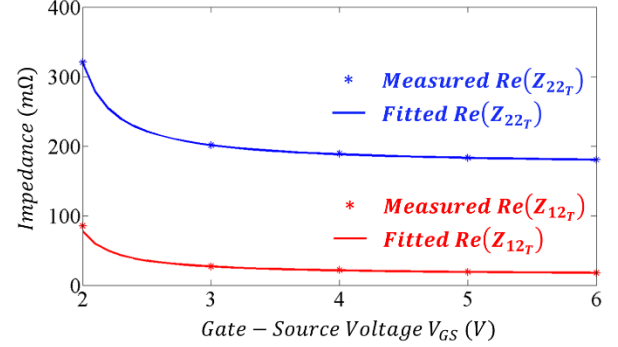


Fig.11.  $\text{Re}(Z_{12T})$  and  $\text{Re}(Z_{22T})$  vs.  $V_{GS}$  and fitting results

TABLE II  
FITTING PARAMETERS OF FIG. 11.

$R_S$ (m $\Omega$ )	$R_D + R_S$ (m $\Omega$ )	$V_t$ (V)	$K_1$ (A.V <sup>-2</sup> )	$K_2$ (A.V <sup>-2</sup> )
14.1	158	1.75	63	27

It can be noted that the parameter  $\alpha$  can be determined as expressed by (25).

$$\alpha = \frac{K_2}{K_1} = 0.43 \quad (25)$$

So far, the access resistances  $R_G$ ,  $R_D$  and  $R_S$  of the transistor were experimentally determined using S-parameter measurements in Cold FET conditions.

#### IV. TEMPERATURE DEPENDENCY OF ACCESS RESISTANCES

The access resistances of transistors are sensitive to junction temperature. In operating conditions, the temperature of the device's junction is much more than the ambient temperature. Thus in order to get the correct resistances values during simulation, their temperature dependency must be determined. However an experimental method to extract access resistances of packaged GaN power transistors at different junction temperature has not been proposed yet.

In this work, the measurement technique presented in section III is proposed to be applied in operating conditions. The electrical equivalent circuit of the transistor presented in Fig. 7 is still considered. The objective is to let a fixed drain current flow through the device by applying a low voltage between drain and source. Then, S-parameters and the transistor temperature are measured. For each drain current, measurements are performed for different  $V_{GS}$  between 3V and 6V (temperature must be constant during these measurements). The junction temperature is evaluated by a thermal imaging camera. These measurements are reinforced by measurements using a thermal sensor located at the source of the device. Table III gives the estimated junction temperatures according to DC drain current.

In order to measure S-parameters at high DC current, specific Bias Tees have been made and enable up to 10A DC current and a measurement bandwidth from 4 MHz up to 700 MHz. The measurement setup is shown in Fig. 12. Bias Tees are calibrated at the output of the VNA.

TABLE III  
 ESTIMATED JUNCTION TEMPERATURE VS. DRAIN CURRENT

Drain Current (A)	Junction Temperature (°C)
0.5	27
1	37
1.5	62
2	104

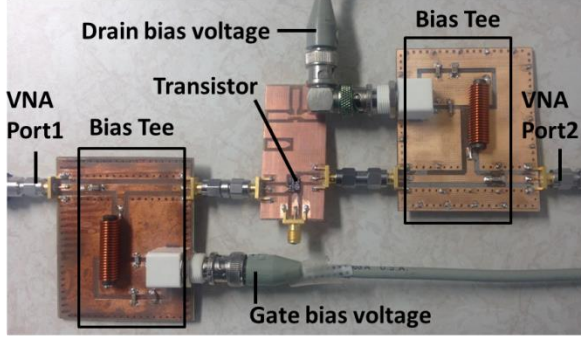


Fig.12. Experimental test bench for S-parameter measurement in operating conditions with proposed Bias Tees

$Re(Z_{12T})$  and  $Re(Z_{22T})$  are obtained at different  $V_{GS}$  at each drain current value as detailed in the previous section. The fitting process shown in Fig. 11 is performed for each current value in order to extract  $R_D$  and  $R_S$  at the four studied junction temperatures. Table IV summarizes the fitting parameters including resistance values at each junction temperature. The value of  $\alpha$  obtained in section III is given as a physical constraint for fittings.

 TABLE IV  
 $R_S$  AND  $R_D$  VS.  $T_j$ 

$T_j$ (°C)	$R_S$ (mΩ)	$R_D$ (mΩ)	$V_t$ (V)	$K_1$ (A·V <sup>-2</sup> )	$K_2$ (A·V <sup>-2</sup> )
27	14.3	163	1.74	63	27
37	15.1	170	1.59	40	19
62	16.6	239	1.37	29	12
104	23.41	317	1.25	21	8.4

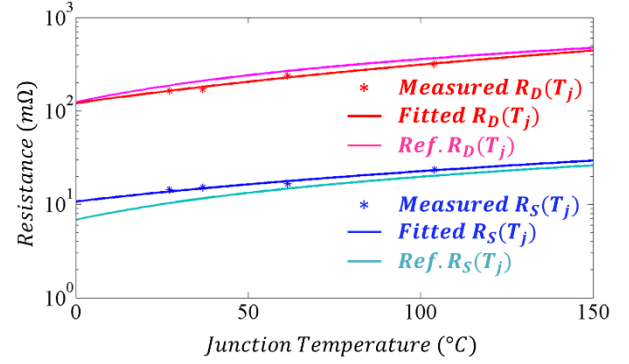
The evolutions of  $R_S$  and  $R_D$  versus junction temperature are shown in Fig. 13 as well as fitting curves from equations (26) and (27) and reference values given by manufacturer's model. The fitting parameters are given in table V.

$$R_S(T_j) = R_{S0} \cdot (1 + \beta_S \cdot T_j + \gamma_S \cdot T_j^2) \quad (26)$$

$$R_D(T_j) = R_{D0} \cdot (1 + \beta_D \cdot T_j + \gamma_D \cdot T_j^2) \quad (27)$$

 TABLE V  
 FITTING PARAMETERS OF FIG. 13

$R_{S0}$ (mΩ)	$R_{D0}$ (mΩ)	$\beta_S$ (°C <sup>-1</sup> )	$\beta_D$ (°C <sup>-1</sup> )	$\gamma_S$ (°C <sup>-2</sup> )	$\gamma_D$ (°C <sup>-2</sup> )

 10.7    121    1.0 10<sup>-2</sup>    1.2 10<sup>-2</sup>    1.1 10<sup>-5</sup>    3.8 10<sup>-5</sup>

 Fig.13. Resistances  $R_S$  and  $R_D$  vs. junction temperature and fitting

In this section, the temperature dependency of packaged GaN power transistor access resistances was determined in operating conditions using S-parameters and thermal measurement.

## V. EXTRACTION OF ACCESS INDUCTANCES

Parasitic inductances due to transistor packaging cause overvoltages and oscillations during switchings. Thus, in order to accurately simulate high frequency converter performances, the access inductances of packaged GaN power switches must be considered.

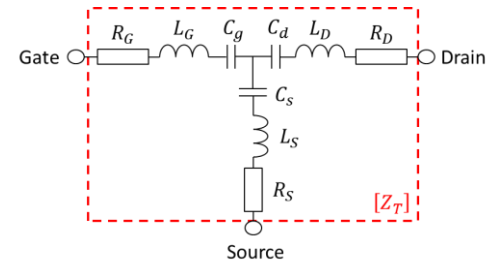


Fig.14. Transistor equivalent circuit in off-state conditions

A well-known technique to extract the parasitic inductances is to perform a 1-port impedance measurement with impedance analyzer [7]. These last few years, some works show the advantages of 2-port S-parameter measurements in off-state conditions [7], [8]. These works were applied to SiC MOSFET inductances extraction. In our study, it is proposed to adapt this technique to packaged GaN power transistors.

Due to the high technological advancement in GaN power devices packaging, the access inductances are reduced to less than 1 nH. Thus, a calibration of the measurement setup is necessary to get the required accuracy. The calibration method described in section II is applied. S-parameter measurements are performed from 1 MHz to 1 GHz at  $V_{GS} = 0V$  and  $V_{DS} = 0V$ . The equivalent circuit of the transistor in off-state conditions is presented in Fig. 14, where capacitances  $C_g$ ,  $C_d$  and  $C_s$  are combinations of capacitances  $C_{gs}$ ,  $C_{gd}$  and  $C_{ds}$  [7]. In order to extract the low inductances with the best accuracy, the impedances given by (28) to (30) are considered.

$$Z_{11T} + Z_{22T} - 2 \cdot Z_{12T} = R_G + R_D + j \cdot (L_G + L_D)\omega + \frac{1}{j \cdot C_{EQ1} \cdot \omega} \quad (28)$$

$$Z_{11T} = R_G + R_S + j \cdot (L_G + L_S)\omega + \frac{1}{j \cdot C_{EQ2} \cdot \omega} \quad (29)$$

$$Z_{22T} = R_D + R_S + j \cdot (L_D + L_S)\omega + \frac{1}{j \cdot C_{EQ3} \cdot \omega} \quad (30)$$

The capacitances  $C_{EQ1}$ ,  $C_{EQ2}$  and  $C_{EQ3}$  are combinations of capacitances  $C_g$ ,  $C_d$  and  $C_s$ . From the resonance frequency of each impedance, given by (31) to (33), the three access inductances can be extracted. Fig. 15 shows the three impedances evolutions and parameters extraction. Table VI gives the extracted parasitic inductances for the considered GaN transistor.

$$f_{R1} = \frac{1}{2\pi \sqrt{(L_G + L_D) \cdot C_{EQ1}}} \quad (31)$$

$$f_{R2} = \frac{1}{2\pi \sqrt{(L_G + L_S) \cdot C_{EQ2}}} \quad (32)$$

$$f_{R3} = \frac{1}{2\pi \sqrt{(L_D + L_S) \cdot C_{EQ3}}} \quad (33)$$

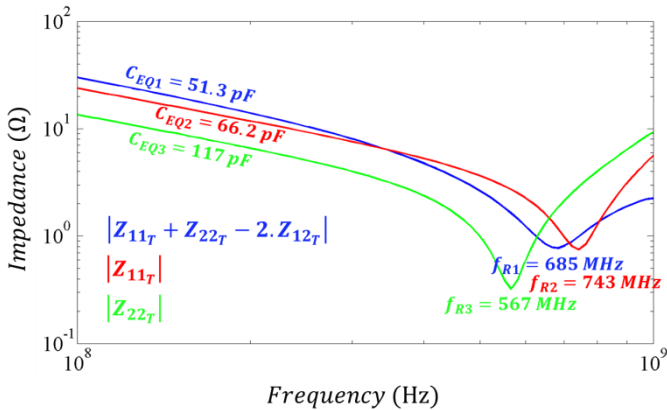


Fig.15. Extraction of parasitic inductances at resonance frequencies

TABLE VI

PARASITIC INDUCTANCES OF GS66502B TRANSISTOR

$L_G + L_D$ (pH)	$L_G + L_S$ (pH)	$L_D + L_S$ (pH)	$L_G$ (pH)	$L_D$ (pH)	$L_S$ (pH)
1050	693	675	534	516	159

The values of 534 pH, 516 pH and 159 pH are extracted for  $L_G$ ,  $L_D$  and  $L_S$  respectively compared to 1 nH, 400 pH and 40 pH given as a reference in the manufacturer's model.

## VI. CONCLUSION

In this paper, a complete methodology is proposed to determine the access parasitics of packaged GaN power transistors for the first time. The method is applied to a commercially available power switch. Access resistances are

obtained using S-parameter measurements in Cold FET conditions and a good agreement is found in term of range with reference values that are only indicators comforting experimental results. The same method is applied in on-state conditions to get the temperature dependency of parasitic resistances and an electrothermal model is proposed. Finally, a methodology is given to extract the access inductances, under the nanohenri range, by adapting existing methods for SiC to GaN devices.

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