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# Indium oxide nanoparticles for Resistive RAM integration using a compatible industrial technology

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## Abstract

- In this work we report on the integration of indium oxide (In<sub>2</sub>O<sub>3</sub>) nanoparticles (NPs) for Resistive Random Access Memory (RRAM) applications. This low-temperature integration process is fully compatible CMOS Back-End integration given a careful selection of materials deposited by MOCVD and ALD. A detailed description of the process is provided together with AFM analysis performed on the indium oxide nanoparticles and TEM cross-sections on the whole stack. It is shown that the introduction of In<sub>2</sub>O<sub>3</sub> NPs provides bipolar switching behavior together with promising electrical performances in terms of large OFF/ON resistance ratio (10<sup>6</sup>) and retention time at room temperature.

Keywords: forming-free RRAM; NVM; nanoparticles; indium oxide.

## 1. Introduction

Current memory technologies (Flash, DRAM) are reaching their downscaling limits and their development has become increasingly complex and costly [1] Flash memory is still considered today as a baseline technology for non-volatile memories in comparison with emerging technologies [2]–[4]. Indeed, finding an alternative technology to Flash non-volatile memories lead to very important research activities on emerging memory technologies such as Magnetic RAM (MRAM), Phase Change RAM (PCRAM) or Resistive Random Access Memory (RRAM) [5]. This later is indeed a potential candidate for the next generations of non-volatile memory. RRAM are often fabricated using CMOS compatible materials and exhibit appealing performances with respect to flash memories in terms of speed, endurance and power consumption [6]–[10]. These two-terminal device

are based on thin layer Metal-Insulator-Metal (MIM) structures and can be switched between two stable resistive states allowing the storage of two binary states. The switching mechanisms of RRAM rely on the growth of conductive filament(s) (CF) within a dielectric layer [7]–[9]. The improvement of RRAM performances in terms of variability and reliability was previously studied through the introduction of nanoparticles within the insulating layer [11]–[15]. Nickel nanoparticle (NPs) - based RRAM have been studied by Tsai et al. [9]. Such RRAM with embedded NPs in Al<sub>2</sub>O<sub>3</sub> dielectric layer exhibited a significant reduction of electrical variability as compared to reference RRAM without NPs. The variability and reliability improvement were attributed to localization of conducting filaments in the vicinity of the NPs.

In this work, indium oxide nanoparticles (In<sub>2</sub>O<sub>3</sub> NPs) were embedded in the Al<sub>2</sub>O<sub>3</sub> and SiO<sub>2</sub> dielectric of RRAM

structures.  $\text{In}_2\text{O}_3$  is an interesting material since it is expected to act as a efficient electron trap with a very large band offset with respect to  $\text{Al}_2\text{O}_3$  and  $\text{SiO}_2$  ( $> 5$  eV), allowing thus to induce electric field modulation within the dielectric layer.  $\text{In}_2\text{O}_3$  NPs are also appealing from a technological point of view since it is possible to use low temperature growth as already demonstrated in [17] and [18]. The proposed approach is therefore fully compatible with Back-End-Off-Line process integration for future non-volatile memory technology nodes. The main objective of our work is to study the nanoparticle size distribution and surface density, to evaluate the effect of a uniform and high density  $\text{In}_2\text{O}_3$  - NPs layer on the electrical properties of RRAM samples.

The fabricated RRAM prototype devices are based on a Metal/ $\text{Al}_2\text{O}_3$ / $\text{In}_2\text{O}_3$ -NPs/ $\text{SiO}_2$ / $\text{Si-n+}$  stack which exhibits a bipolar switching behavior. Efforts have been made to achieve a very good control of the fabrication process in particular for the nanoparticles deposition.  $\text{In}_2\text{O}_3$  NPs fabricated with different process conditions were fabricated and their morphology was studied by means of AFM (Atomic Force Microscopy) measurements. Electrical measurements were then conducted on RRAM devices by means of DC and pulsed measurements. In addition, conduction mechanisms were investigated through IV measurements achieved at various temperatures. Finally, data retention and cycling measurements are presented. The obtained results are finally discussed in connection with the material parameters.

## 2. Experimental

### 2.1. Device fabrication process

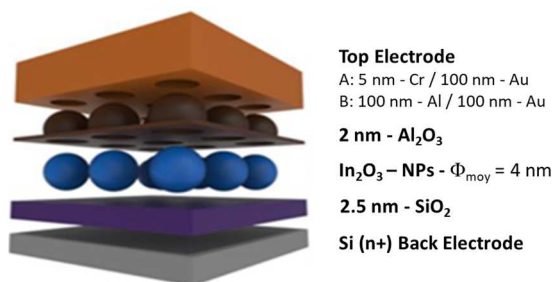


Figure 1: Schematic of the stack of the test device

The material stack used for device fabrication is schematized in Figure 1. It consists in a Au/Metal/ $\text{Al}_2\text{O}_3$ /NPs:  $\text{In}_2\text{O}_3$ / $\text{SiO}_2$ / $\text{Si n+}$  sandwich deposited on highly doped ( $>3.10^{19} \text{ cm}^{-3}$ ) n+ 12 inches (001) silicon wafers serving as bottom electrode. The fabrication procedure starts with the thermal oxidation of the Si substrate to achieve a high quality 2.5 nm-thick  $\text{SiO}_2$  tunnel oxide. nanoparticles were then grown on the  $\text{SiO}_2$  layer by Metal

Organic Chemical Vapor Deposition (MOCVD, Applied Materials tool). The deposition temperature was kept below  $450^\circ\text{C}$  to ensure full compatibility with Back-End-Off-Line process of standard CMOS technology. It is possible to control the size and the density of the nanoparticles with an excellent homogeneity over the 300 mm diameter of the wafer. As shown on the AFM images of Figure 2, a density up to  $2 \times 10^{10} \text{ cm}^{-2}$  can be obtained with an homogeneous average height of 4 nm. The width of the particles seems larger due to the tip convolution effect occurring during the imaging of the NPs [16]. After this first step, the wafers were diced into smaller samples for the rest of the process. The top  $\text{Al}_2\text{O}_3$  oxide layer was deposited by means of a Fiji 200 ALD tool from Ultratech. The deposition process relied on 25 cycles of trimethylaluminum and  $\text{H}_2\text{O}$  in thermal mode at  $200^\circ\text{C}$  to reach a 2 nm-thick aluminum oxide layer. Finally, the top contact electrode was deposited with an Edwards Auto 306 Evaporator through a shadow mask. The electrode material consisted of either chromium for devices of batch A or aluminum for devices of batch B.

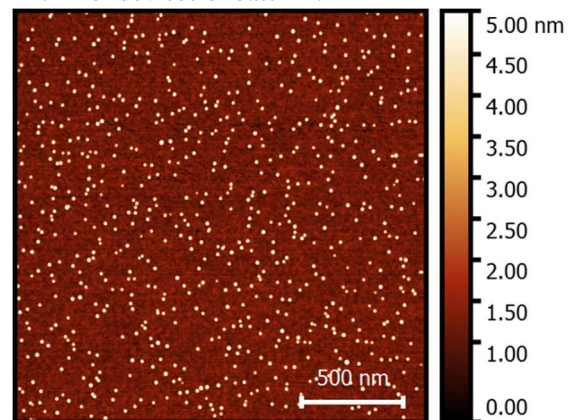


Figure 2: AFM picture on the top of  $\text{SiO}_2$  surface after the growth of  $\text{In}_2\text{O}_3$  NPs.

As the stack is organized vertically, the shape and the area of the memory cell is determined by the top electrode. The electrodes are circular shaped with diameters of 30, 50 or  $100 \mu\text{m}$ . The Top Electrode (TE) for Batch A samples consist of a 5 nm-thick Chromium seed layer followed by the deposition of a 200 nm-thick gold layer. TE for Batch B samples consist of 100 nm-thick aluminum followed by the deposition of a 100 nm-thick gold layer. Aluminum for Batch B allows to get samples with a symmetric energy band diagram of the stack with comparable work functions for top and bottom electrodes ( $\Phi_{\text{Al}} = 4.09$  eV,  $\Phi_{\text{n+ Si}} = 4.05$  eV). Aluminum also led to stable Al /  $\text{Al}_2\text{O}_3$  interfaces as compared with Cr /  $\text{Al}_2\text{O}_3$  system. Top electrodes were capped with gold to prevent their oxidation in air and ensure a good electrical contact with the test probes. The samples were finally annealed at  $400^\circ\text{C}$  for 10 minutes under  $\text{N}_2$  atmosphere using a RTA oven from Jipelec. Batch A samples have been used for a better understanding of

conduction and switching mechanisms. Batch B samples have been mainly used for pulse mode studies thanks to the stable Al / Al<sub>2</sub>O<sub>3</sub> interfaces. For each batch, reference samples without NP was processed with exactly the same material stack. These reference structures are used to better evaluate the role of the NPs in the memory effect of our RRAM devices.

To characterize the devices, the native oxide is removed from the backside of the silicon substrate. The sample is then glued on a conductive holder using silver paste to obtain a good ohmic contact on the n<sup>+</sup> Si bottom electrode. The bottom electrode remained grounded for all electrical measurements.

## 2.2. Indium oxide nanoparticles

Since our previous work [17,18,19], the MOCVD process has been optimized to achieve a better control in terms of size and density of the

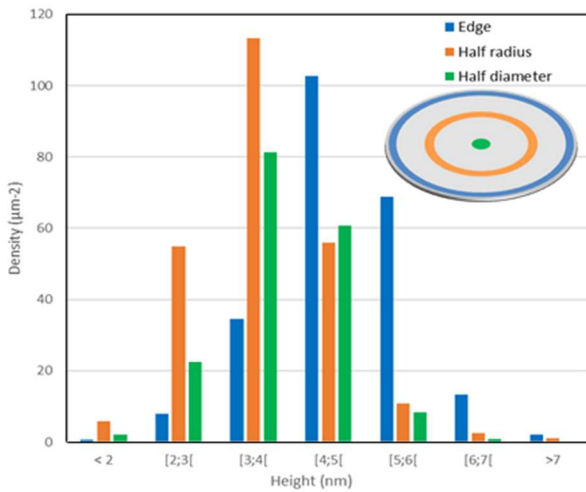


Figure 3: Height distribution of nanoparticles deposited by MOCVD and measured by AFM on the edge, the half radius and the half diameter of a 300 mm wafers as shown on the insert.

deposited indium oxide NPs. In previous works [17, 18, 19], the obtained surface density of NPs was  $3 \times 10^8 \text{ cm}^{-2}$  while the average diameter was distributed from 9 to 14 nm. As shown Figure 3, we were able in the present work to deposit a uniform and high density NPs layer over a 300 mm wafer with a low size dispersion. The height of the nanoparticles has been measured with an Atomic Force Microscope (Icon, Bruker) on the edge, center and half of the radius of the wafer. The height of more than 90% of the deposited NPs ranges between 2 and 6 nm with an average value of 4 nm. Besides an improved control of the deposition in terms of density and size distribution of the NPs, experiments have been conducted in order to characterize the structural parameters of the nanoparticles. Figure 4 shows a typical TEM (Transmission Electron Microscope) cross-sectional

view of a nanoparticle (Jeol 2100 equipment). The corresponding sample is grown on thermal SiO<sub>2</sub> and capped with 2 nm of Al<sub>2</sub>O<sub>3</sub> deposited by ALD and then annealed at 400°C during 10 minutes. The top carbon layer onto the Al<sub>2</sub>O<sub>3</sub> layer acts as a protecting layer for TEM observations. It was already demonstrated that the NPs can be in the crystalline phase even with a diameter of few nanometers as shown Figure 4 [17]. Both amorphous and crystalline nanoparticles were observed in our samples. It has been observed in real time that the electron beam may contribute to the crystallization of the nanoparticles during the observation. The lattice fringe periodicity of the (222) plan of the nanoparticles could be attributed to the most intense diffraction direction of the crystalline In<sub>2</sub>O<sub>3</sub> (222) cubic structure [23], [24]. We can also notice that the aluminum oxide deposited by ALD is conformal as expected.

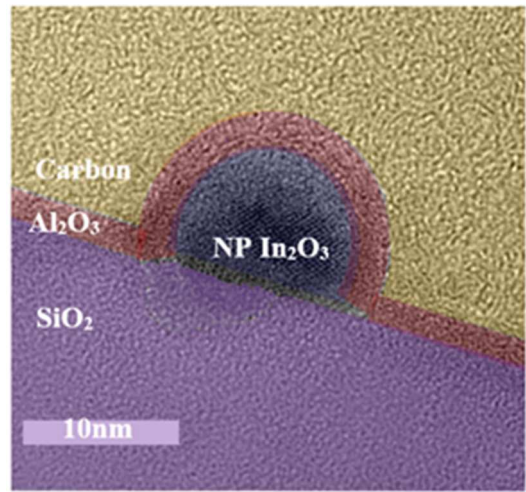


Figure 4: TEM view with artificial colour of In<sub>2</sub>O<sub>3</sub> nanocrystals showing crystalline structure synthesized on 100nm thick thermal SiO<sub>2</sub> and capped with a 2 nm thick Al<sub>2</sub>O<sub>3</sub> then annealed at 400 °C

## 2.3. Electrical measurements setup and protocol

The electrical characterizations in DC or pulse modes were done with a probe station at room temperature. Current-voltage measurements were obtained using a Keithley 4200 semi-conductor parameter analyzer (Keithley 4200-A SCS).

I-V measurements of the RRAM samples were recorded in quasi-static (DC) mode. A 0 to 4 V dual voltage sweep is applied on the top electrode with a grounded bottom electrode and a fixed current compliance I<sub>c</sub> in order to observe resistive switching. In order to minimize power dissipation during resistance switching and prevent early breakdown of the devices, the compliance current was gradually increased after each non-switching sweep.

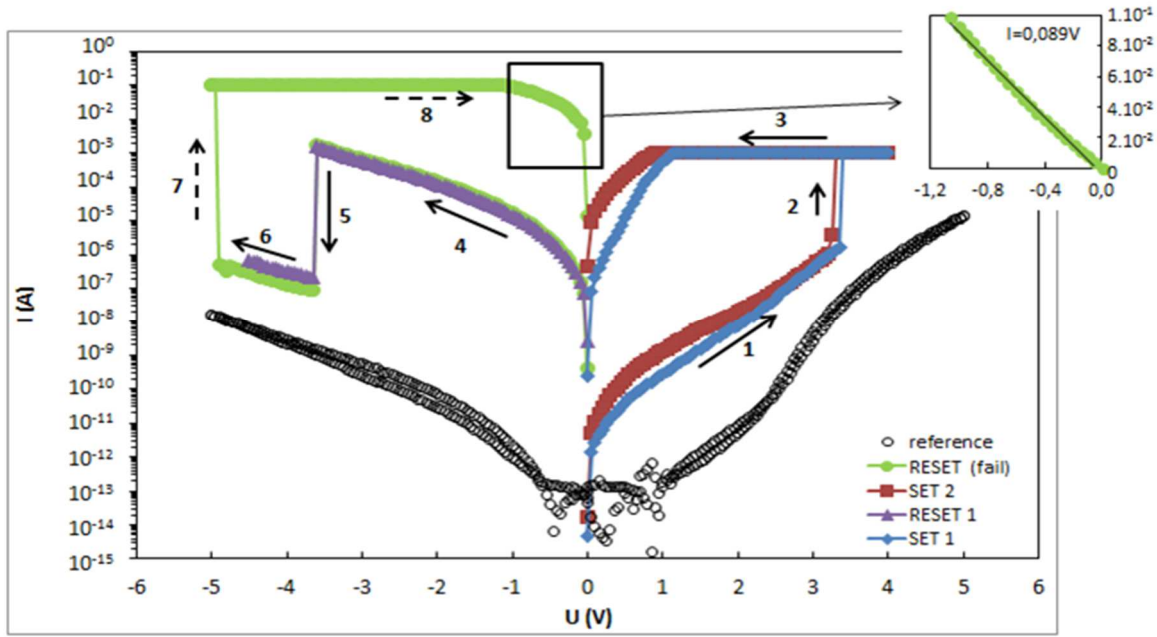


Figure 5: Typical semi-logarithmic  $I(V)$  characteristic of a device with  $100\mu\text{m}$  diameter from batch A. The measurements in color (blue, purple, red and green) correspond to sample with NPs and the black circles correspond to reference samples without NPs. Part of the green curve is plotted in linear scale to show its Ohmic behavior.

### 3. Results and Discussion

#### 3.1. Bipolar resistive switching

Figure 5 illustrates a typical  $I-V$  curves of a  $100\mu\text{m}$ -RRAM device and its corresponding reference sample from batch A.

It is confirmed that RRAM devices exhibited a bipolar resistance switching while no switching event was observed on reference samples even using a stop-voltage of 5 V. This result highlights that the presence of the NPs plays a major role in the switching behavior.

As can be seen in Figure 5, (1) the device initially in a High Resistive State (HRS) suddenly switches to a Low Resistive State (LRS) at a SET voltage of 3.5 V (2). During the backward sweep (3), the Low Resistance State (LRS) is maintained using a compliance current of 1 mA. A negative voltage sweep is then applied without compliance current in order to RESET the device from LRS to HRS (4). Reset is achieved at  $V_{\text{RESET}} = -3.3$  V (5) where an abrupt drop of the current is observed. It is noticeable that these devices do not need any forming process to work as resistive switches as the first and subsequent SET occur at a similar voltages. Our best devices reached more than 20 cycles using this measurement protocol before being definitely stuck in LRS. 64 cycles have been measured at  $100^\circ\text{C}$  in a previous study

[19] for devices with a lower NPs density ( $3 \times 10^8 \text{ cm}^{-2}$ ) and larger size distribution (9 nm to 14 nm). NP density is expected to play an important role in cycling performances. As shown in Figure 5, we can reach the breakdown of devices if the applied voltage is too high or sometimes after a certain number of write/erase cycles (6). We also noticed a strong increase of the measured current (7) during the negative backward sweep often corresponding to a hard-breakdown of the device (8). After the breakdown phenomenon, the devices exhibited a linear  $I-V$  and remained stuck in this ohmic behavior with a electrical resistance of  $11 \Omega$ .

#### 3.2. Pulse mode measurements

Device performances was also investigated through voltage pulse measurements. The objective of the pulse measurements was to switch the resistance of the memory using short voltage pulses. The used protocol is schematized in Figure 6 a). 4 voltage pulses have been used to perform a full measurement cycle: READ/SET/READ/RESET. Since our measurement setup is not suited to measure the current during pulse duration lower than few hundreds of milliseconds, we have only recorded the data (READ) after each programming pulse at  $V_{\text{READ}} = 1$  V. The SET operation was performed at  $V_{\text{SET}} = 5\text{V}$  while RESET was done at  $V_{\text{RESET}} = -3$  V. If no resistance change is observed between

two consecutive READ steps the absolute value of the programming voltage was incrementally increased by 100 mV.

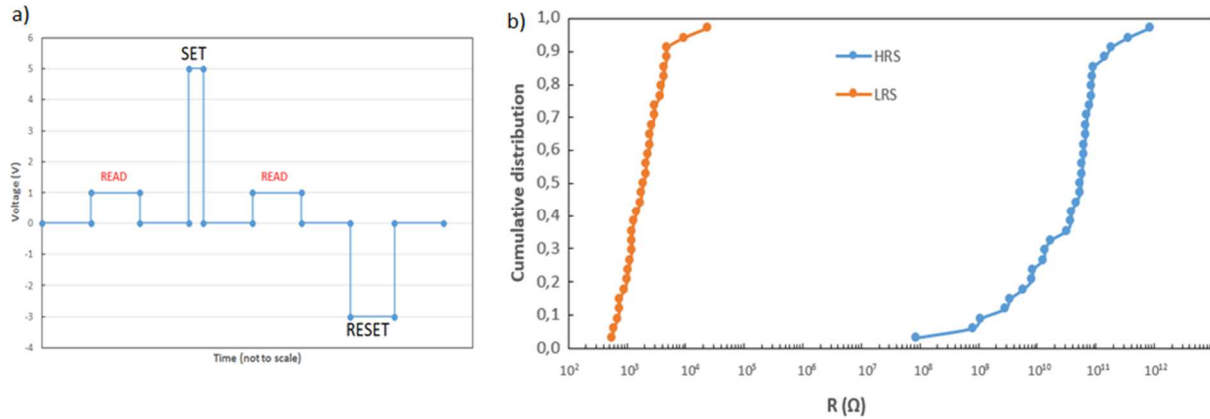


Figure 6: a) Schematic pulse mode process. A controlled voltage is applied during a certain timelapse (here in arbitrary unit). The read operation is achieved at 1 V, the initial SET at 5V and the initial RESET at -3 V. The time axis is only indicative as SET and RESET time durations are adjusted but not the reading time; b) Cumulative distribution of the resistance for both states HRS and LRS for a device with 30  $\mu\text{m}$  diameter from batch B.

Figure 6 b) shows the response of our best device from batch B with 34 consecutive switches. The LRS and HRS cumulative distributions on this sample are shown. The LRS does not vary significantly during the measurements with 32 out of 34 values between 600  $\Omega$  and 5 k $\Omega$ . Higher variability is observed on HRS over 3 to 4 decades. These results are obtained with pulse durations of 300 ms that are shorter than the required time using static I(V) curves but still quite longer than conventional memory operation. Finally, these

measurements in pulse mode allow to clearly distinguish the HRS and LRS states and to extract a  $R_{\text{OFF}}/R_{\text{ON}}$  ratio from 10<sup>3</sup> up to 10<sup>6</sup>. It is interesting to note that reducing SET and RESET programming times may strongly improve the endurance together with the reliability of the devices. It is possible to switch our memory with a pulse duration of 500 ns for the SET and a pulse duration of 500  $\mu\text{s}$  for the RESET.

### 3.3. Data retention

Data retention measurements were performed on devices from batch B to observe the evolution of both resistance states. The devices were first cycled in order to check that they were able to sustain at least two switching cycles. After a SET operation, the devices were left in LRS state and regularly measured at a read voltage of 1V to evaluate their resistance at increasing time delays.

All the devices show a really stable HRS state. This stability is illustrated by the orange line on Figure 7. The HRS value before the retention measurement is close to the pristine state resistance. In addition, we observed that the LRS state (*i.e.* 1.4 k $\Omega$ ) was very stable. We did not observe any change in the LRS before more than 4.5 days ( $4 \cdot 10^5$  s). After  $4 \cdot 10^5$  s the resistance of the LRS decreases a little to reach a minimum value of 600  $\Omega$  after  $8 \cdot 10^5$  s (>9 days).

The magnitude of the resistance then remained unchanged after  $6.5 \times 10^6$  s (75 days). This result confirms a good retention time at room temperature which is expected to be much longer than 75 days.

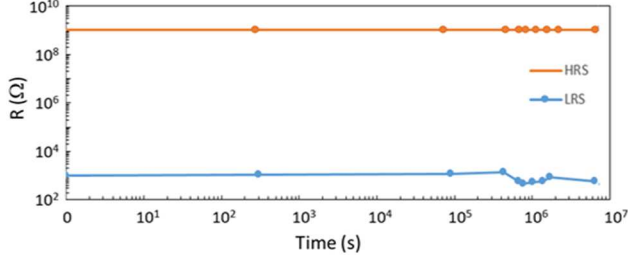


Figure 7: Exemple of retention measurements of a 30µm diameter device from batch B at room temperature ( $V_{read} = 1$  V). The blue line shows a measurement during almost 1800 hours in LRS and the orange one shows the HRS state just before the

### 3.4. Study of conduction and switch mechanisms

To better understand the switching mechanism in our devices we first performed I-V measurements on samples with different electrode areas. Figure 8 shows the I-V curves of two devices from batch A under a sweep voltage from 0 to 4 V then from 4 V to -4 V with a fixed compliance  $I_c = 10^{-4}$  A. The electrode diameter varied from 50 µm (green square curve) to 100 µm (blue triangle curve). These measurements have shown that the current in HRS state is linked to the electrode area while the LRS current did not exhibited significant changes as it may attributed to filamentary conduction. A second set of measurements has been performed at various compliance currents. Figure 9 shows the I-V curves for 3 devices from batch A with a diameter of 100 µm using voltage sweeps from 0 to 4V and then from 4 V to -4 V. Two current compliances are presented ( $I_{c1} = 10$  mA and  $I_{c2} = 10$  µA). In this case, we can notice a direct dependence of the current in LRS state with the compliance level. This phenomenon is typically observed on RRAM devices with a filamentary switching behavior [23], [24].

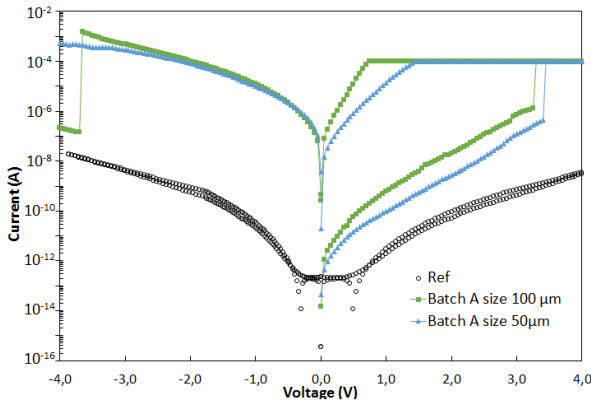


Figure 8: I-V curves for 2 devices from batch A with different diameter: 50 µm (blue triangle) and 100 µm (green square).

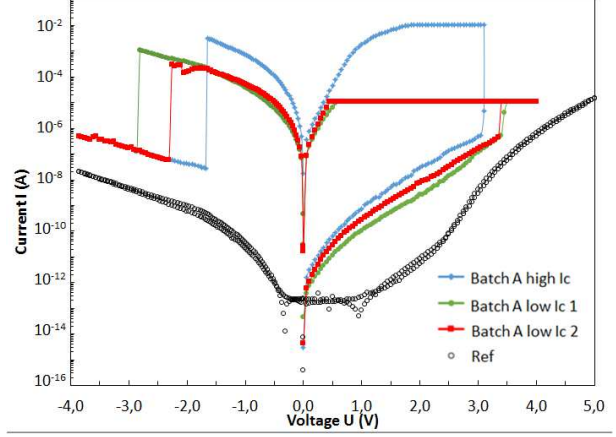


Figure 9: I-V curves for 3 devices from batch A with the same diameter (100 µm). Current compliance is increased from 10 µA (low  $I_c$ ) to 10 mA (high  $I_c$ ).

Finally, the conduction mechanisms in LRS and HRS states have been carefully studied using temperature dependent I-V measurements using a cryogenic probe station. I-V curves were recorded using a voltage sweep from 0 to 4 V with temperature varying from 150 K to 300 K with 50 K temperature steps. Experimental data have been analyzed and compared with theoretical analytical models before parameter extraction. The temperature dependent I-V curves are presented on figure 10 for samples in HRS state. 3 devices from batch B have been analyzed at each temperature (12 plots) to focus on HRS state. The weak temperature dependence observed from 150 K to 300 K is consistent with a tunneling mechanism. One possible conduction mechanism is a Trap Assisted Tunneling (TAT) current.

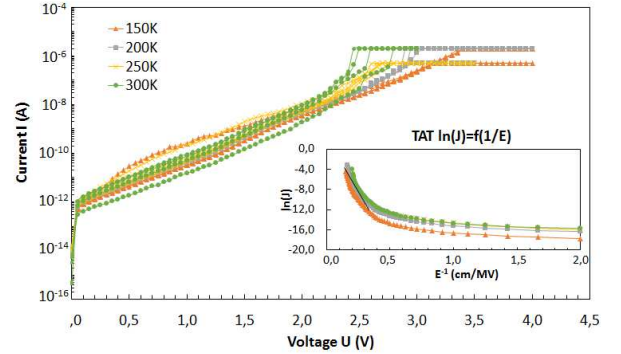


Figure 10: I-V curves as function of temperature (150 K to 300 K with 50 K step) in HRS state of 3 devices from batch B. The insert shows the TAT model plots:  $\ln(J)$  vs  $(E^{-1})$ .

The inset of Figure 10 shows a nice agreement with a TAT model with a data plot of  $\ln(J)$  vs  $(E^{-1})$ . The slope of the curve in the TAT model curve allow a trap level extraction between 0.62 eV to 1.04 eV. This assumption is consistent with a volume conduction mechanism.

I-V curves at various temperatures in the LRS state are plotted in figure 11. The current was measured from 0 to -3 V before the RESET step for 2 devices from batch B. All samples were previously switched with the same compliance at 500  $\mu$ A to ensure the same LRS state. A weak temperature dependence was also observed from 150 K to 300 K.

Among several investigated conduction models, our data exhibited their best agreement with a Poole-Frenkel conduction mechanism. In order to extract Poole-Frenkel parameters, we have fixed the oxide thickness at 2.5 nm and extracted a relative dielectric constant from the Poole-Frenkel plot between 3.5 to 4.1. The extracted dielectric constant is close to the typical 3.9 dielectric constant of SiO<sub>2</sub>. A conductive filament formed in the Al<sub>2</sub>O<sub>3</sub> layer is a plausible explanation for the conduction in LRS state.

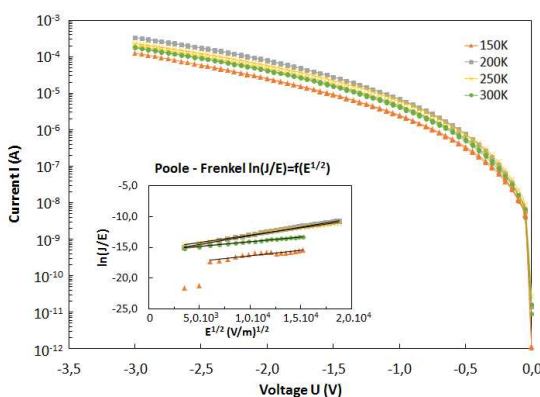


Figure 11: I-V curves as function of temperature (150 K to 300 K with 50 K step) in LRS state of 2 devices from batch B. The insert shows Poole - Frenkel plots:  $(\ln(J/E))$  vs  $(E^{1/2})$ .

## Conclusions

In this paper a fully compatible CMOS Back-End-Of-Line fabrication process is presented for potential applications to RRAM based on In<sub>2</sub>O<sub>3</sub> nanoparticles.

An improved control of the size, shape, nature and density of the nanostructures is demonstrated. We increased the density by a factor of 100 from  $3 \times 10^8$  cm<sup>-2</sup> to  $2 \times 10^{10}$  cm<sup>-2</sup> together with a good control on the size of the nanocrystals. The homogeneity is well controlled all over the surface of 300 mm wafers with a low size dispersion.

The electrical characterization of the devices showed a bipolar switching behavior with a very high R<sub>OFF</sub>/R<sub>ON</sub> ratio up to 10<sup>6</sup> in pulse mode. The switching phenomenon was attributed to the NPs as it was not observed in reference samples without NP. The switching mechanism is attributed to a filamentary growth through the aluminum oxide. Cycling measurements have shown up to 34 switching cycles on 30  $\mu$ m devices. The use of aluminum as top electrode allows a good stability with Al<sub>2</sub>O<sub>3</sub> layer and stable electrical characteristics. Both ON and OFF states are very stable at

room temperature with retention time of few thousands of hours without noticeable LRS or HRS degradation.

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**Highlights** of the manuscript “ Indium oxide nanoparticles for Resistive RAM integration using a compatible industrial technology”

- Uniform layer deposition by MOCVD on 12” wafers of high density sub-10 nm indium oxide nanoparticles
- Compatible CMOS BEOL process for vertical resistive memories integration.
- Proof-of-concept of forming-free ox-RRAM device.
- Bipolar resistive switching due to indium oxide nanoparticles integration.
- Strong Improvement of  $I_{ON}/I_{OFF}$  ratio and retention time thanks to indium oxide NPs.

## Author's Biography

**Pierre-Vincent Guenery** received his M. S. degree in material science and engineering in 2016 and his PhD in 2019 from INSA de Lyon (France) in close collaboration between INL CNRS (Lyon) and LTM CNRS (Grenoble).



His work is focused on emerging resistive memories technology that includes indium oxide nanoparticles. Research activities include material growth, fabrication process, material characterization and electrical device characterization and simulation.

**Edgar LEON PEREZ** received the M.S. degree in Nanoscale Engineering from INSA Lyon-UCBL1-Ecole Centrale de Lyon (2012), and the Ph.D degree in Nanoelectronics and Nanotechnologies from University of Grenoble Alpes (2016), France.



During his Ph.D. he developed devices prefiguring a force/displacement sensor based on individually contacted vertical ZnO nanowires exploiting the piezotronic effect. In 2016, he conducted a postdoctoral training at Institute of Nanotechnologies of Lyon, France, concerning the use of indium oxide nanoparticles for non-volatile memory applications.

Since 2018, he is with the STMicroelectronics Company, Crolles, France, where he is working in the development of CMOS Imaging Sensors as a R&D Engineer.

**Khaled AYADI** is engineer assistant at CNRS and specialized in clean room microfabrication processes. After studying Physical Measurements at IUT of Clermont Ferrand. he joined the Laboratory of Multimaterials and Interfaces in 2000 as a technician for elaboration and characterization of boron nitride fibers.



In 2002, he joined the CNRS in Genoble with a permanent technician position of thin film processing at CNRS Néel Institute. In 2008, he joined the Nanolyon technological platform at the INL laboratory in Lyon. He got an engineer assistant position in 2010 and was appointed as technical manager of the INL-INSA clean room in 2017.

In 2018, he joined the CNRS-CRHEA laboratory in Valbonne, as a process engineer for developing GaN-based transistors.

**Damien DELERUYELLE** is full professor at INSA Lyon (France) and at INL (Institut des Nanotechnologies de Lyon). His research activities concern emerging memory technologies (NC-Flash, RRAM, FeRAM, ...) spanning from multi-scale electrical characterization up to physical modeling and simulation.

**Serge BLONKOWSKI** After a PhD in Physics on III-V compounds/electrolyte interface charge transfer, S. Blonkowski was engaged in the scientific database constitution of the Centre National d'Etudes des Télécommunications (CNET).



His center of interest moved then to Ta2O5 PECVD deposition for MIM and MOS application. He was then in charge at STMicroelectronics of dielectric reliability characterization and modeling in the framework of HK/ metal gate for the 28 nm Program. During this time, he proposed a filamentary approach of dielectric breakdown and the use of extreme values statistics for the metallic interconnect failures and dielectric breakdown. He introduced a systematic approach of nanoscale electrical statistical measurements using UHV CAFM in collaboration with CNRS. Currently he is involved in the nonvolatile memories program at CEA-Leti. His centers of interest are the modeling of OxRRAM, PCM based resistive memories, as their nanoscale electrical characterization. He joined CEA Leti since January 2020.

**Thierry BARON** is director of research at CNRS-Grenoble. He received his Ph.D. at University Grenoble Alpes in 1996. His thesis focused on II-VI semiconductor for optoelectronic applications and his post-doc at the University of Wurzburg (Germany) was on the fabrication and characterization of II-VI LEDs. He joined the CNRS in 1998 to work on the elaboration of silicon nanocrystals on insulating substrates, the study of their physical properties and their integration in memory devices. Then he investigated the catalytic growth of Si, Ge and heterojunction nanowires and their integration to demonstrate specific functions in an industrial environment. His current research focuses hetero-epitaxy of III-V semiconductor on silicon to improve electronic and optoelectronic devices.



**Liviu MILITARU** received the M.S. degree in electrical engineering in 1997, the PhD degree in semiconductors physics in 2000, both from the Institut National des Sciences Appliquées (INSA) of Lyon, France.



In 2011 he obtained French post-doctoral degree allowing its holder to supervise PhD students, HDR. During his PhD thesis, his research activities were related to the electrical characterization of SiGe/Si heterojunction bipolar transistors. From 2000 to 2002, he was a research assistant and since 2002, he has been Associate Professor at INSA-Lyon. His main research interests are electrical characterization of MOS devices including transistors and memories, alternative high-k dielectrics used as oxide gate and the development of new characterization techniques adapted at nanoscale.

**Abdelkader SOUFI** received his Ph.D. in 1993 at National Institute of Applied Sciences (INSA Lyon). From 1994 to 1995, he joined the Institute of Thin Films at Julich Research Center in Germany, where he was involved in the



studies of nanostructures for silicon-based nanodevices. In 1995, he joined INSA Lyon as Assistant Professor in the field of heterojunction-based devices. Since 1998, his research activities is focused on silicon-based Nanoelectronics. He obtained a full Professor position in 2002 and leded the Silicon Electron Device Group of Lyon Institute of Nanotechnology from 2002 to 2007. From 2008 to 2014, he was Director of the international CNRS Lab. with the University of Sherbrooke in Quebec, Canada. His current research interests include nanofabrication and characterizations of advanced memory devices and ultra-low power sensor systems.