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## GaN-on-silicon transistors with reduced current collapse and improved blocking voltage by means of local substrate removal

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We report on the demonstration of low trapping effects above 1200 V of GaN-on-silicon transistors using a local substrate removal (LSR) followed by a thick backside ultra-wide-bandgap AlN deposition. Substrate ramp measurements show reduced hysteresis up to 3000 V. It has been found that the LSR approach not only enables the extension operation voltage capabilities of GaN-on-silicon HEMTs with low on-resistance but also allow for the reduction of trapping effects directly affecting their dynamic behavior. This work points out that a large part of the electron trapping under high bias occurs at the AlN nucleation layer and Si substrate interface. © 2021 The Author(s). Published on behalf of The Japan Society of Applied Physics by IOP Publishing Ltd

For future efficient and low-cost power electronics, GaN high-electron-mobility transistors (HEMTs) on silicon (Si) substrate are highly promising owing to their superior intrinsic properties such as large bandgap, high breakdown field strength and high electron saturation velocity.<sup>1–12</sup> GaN-on-Silicon HEMTs offer the potential to revolutionize power electronics by enabling important energy savings and new flexibility for advanced power circuits.<sup>13</sup> However, these types of devices suffer from poor critical electric field strength of the Si substrate together with a parasitic conduction at the buffer/substrate interface leading to device breakdown.<sup>14–17</sup>

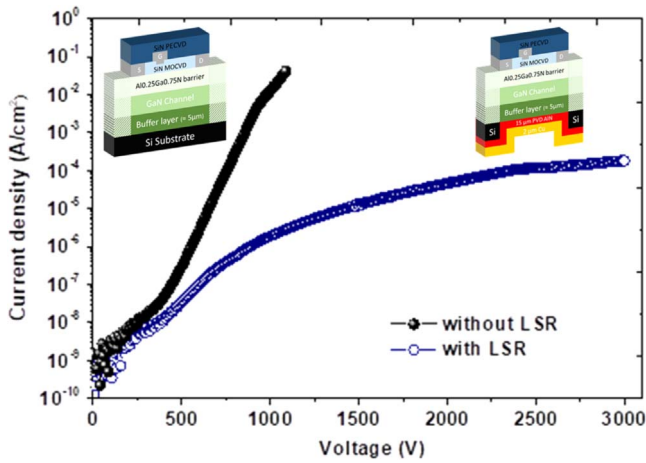
That is why, the highest reported three-terminal breakdown voltage (VBD) values for grounded GaN-on-Si HEMTs defined at an off-state leakage current of  $1 \mu\text{A mm}^{-1}$  are still below 1.5 kV, which is basically limited by the Si substrate and material quality. Consequently, applications requiring voltage operation above 1 kV cannot currently be covered by GaN-on-Si HEMTs, although thicker buffers with high associated material quality have been developed.<sup>18–20</sup>

A solution to suppress the parasitic conduction phenomenon and thus enhance the breakdown voltage (BV) is to remove the Si substrate.<sup>21–24</sup> Indeed, the Si substrate removal around the drain electrode enabled electrical isolation of the gate and source contacts from the drain across the buffer layer/Si interface. Using this approach, GaN-on-Si based transistors with a significantly improved blocking voltage of 3000 V have been reported.<sup>25</sup> Recently, we have demonstrated GaN-on-Si metal insulator semiconductor HEMTs (MISHEMTs) with LSR under the entire device followed by a backside deposition of the ultra-wide bandgap AlN material.<sup>26</sup> The use of an in situ SiN gate dielectric and local substrate removal (LSR) technique combined with 15  $\mu\text{m}$  thick AlN layer enabled state-of-the-art GaN based HEMTs with remarkably low off-state leakage current ( $<1 \mu\text{A mm}^{-1}$ ) up to 3000 V. On the other hand, a key figure of merit for GaN power devices is the current collapse that hindered for instance the commercialization of 650 V-rated GaN-on-Si devices.

In this work, we assessed the DC, high voltage and dynamic characteristics of high voltage transistors with and without LSR. We demonstrate the possibility to benefit from low electron trapping effects on lateral GaN-on-Si based transistors while extending the blocking voltage capabilities as compared to transistors without LSR.

The AlGaN/GaN heterostructure has been grown by meta-organic chemical vapor deposition (MOCVD) on a 6 inch Si (111) substrate. The HEMT structure consists in a 5  $\mu\text{m}$  buffer thickness, a 310 nm undoped GaN channel followed by a 24 nm  $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$  barrier layer and an 11 nm in situ  $\text{Si}_3\text{N}_4$  cap layer. Ohmic contacts were formed directly on top of the AlGaN barrier by alloying Ti/Al/Ni/Au stack using an 875 °C rapid thermal annealing resulting in contact resistances of 0.3  $\Omega \cdot \text{mm}$ . Device isolation was performed by  $\text{N}_2$  implantation. Hall measurements reveal a sheet carrier concentration of  $0.9 \times 10^{13} \text{ cm}^{-2}$  with a mobility of  $2100 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ , and a sheet resistivity of 330  $\Omega/\square$ . Metal-insulator-semiconductor (MIS) gate structure was employed by using Ni/Au metal stack inside the in situ  $\text{Si}_3\text{N}_4$  cap layer without any additional field-plate. A 200 nm thick SiN film was deposited by plasma enhanced chemical vapor deposition (PECVD) as extra passivation. Once the front-side processing was completed, the Si substrate was locally etched up to the AlN nucleation layer around the entire device using a highly selective Bosch process etching. It is important to note that our mask design consists of devices with and without LSR patterns, which eliminates any processing or epi variation during the device characterization. Then, 15  $\mu\text{m}$  thick nanocolumnar crystalline AlN was deposited on the backside by physical vapor deposition (PVD) at 300 °C, which is post front-side process compatible as it complies with the thermal budget. The AlN film delivers a high breakdown field well-above 4  $\text{MV cm}^{-1}$  despite the low temperature deposition as checked through vertical measurements on a reference doped silicon wafer. Finally, 2  $\mu\text{m}$  of copper is deposited on top of the PVD AlN into the backside trenches. Hall measurements remains identical after full backside processing and subsequent AlN and metal depositions.





**Fig. 1.** (Color online) Room temperature vertical leakage characteristics of the AlGaIn/GaN epitaxial structure with and without LSR.

As expected, the vertical leakage current measurements conducted on isolated patterns with LSR show a remarkable increase from 1000 V to above 3000 V (limitation of our set-up) as compared to patterns without LSR (Fig. 1). This confirms the suppression of the substrate conduction phenomena and effectiveness of the AlN dielectric thick film.

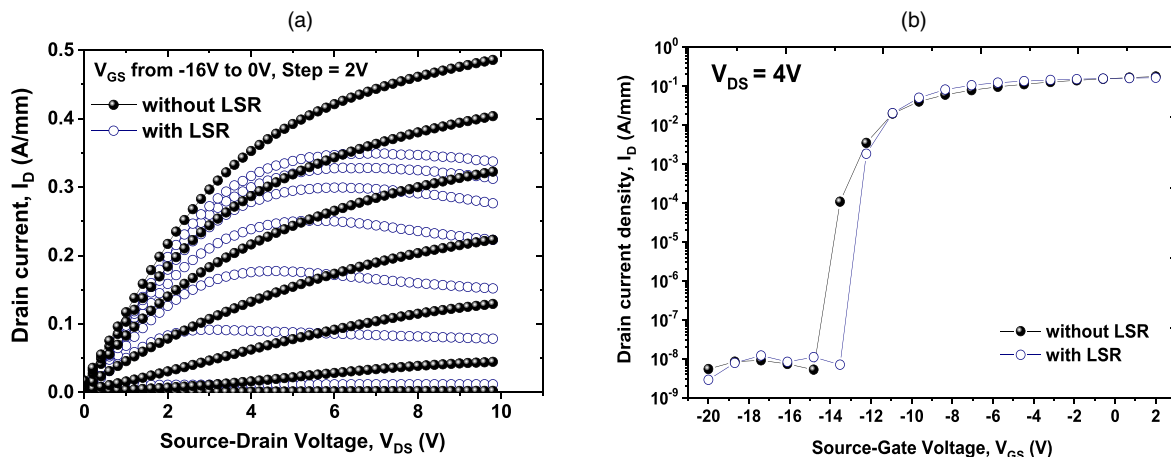
DC characterizations were carried out on devices with a gate width/length = 50  $\mu\text{m}/2 \mu\text{m}$  and various gate-to-drain spacing ( $L_{\text{GD}}$ ) with and without LSR on the same wafer. Maximum current density of transistors with  $L_{\text{GD}} = 5 \mu\text{m}$  at  $V_{\text{DS}} = 10 \text{ V}$  and  $V_{\text{GS}} = 0 \text{ V}$  decreased from 490 to 340  $\text{mA mm}^{-1}$  after the Si substrate removal under the active region due to self-heating [Fig. 2(a)]. It can be pointed out that a significant recovery of the maximum current density occurs after the Cu deposition, which in turn enables the reduction of self-heating.<sup>27,28)</sup> Consequently, a thicker Cu heat sink ( $>10 \mu\text{m}$ ) is expected to mitigate the current density reduction. Nevertheless, the extracted static specific on-resistance ( $R_{\text{ON-STATIC}}$ ) values are found to be below 10  $\text{m}\Omega \text{ cm}^{-2}$  in both cases. The corresponding transfer characteristics of AlGaIn/GaN MISHEMTs with  $L_{\text{GD}}$  of 5  $\mu\text{m}$  are shown in Fig. 2(b). Despite a slight shift of the threshold voltage, it appears that the off-state leakage currents with and without LSR are similar and well-below 0.1  $\mu\text{A mm}^{-1}$  at low drain bias.

The three-terminal off-state leakage characteristics of the AlGaIn/GaN MISHEMTs are plotted as a function of  $L_{\text{GD}}$  in

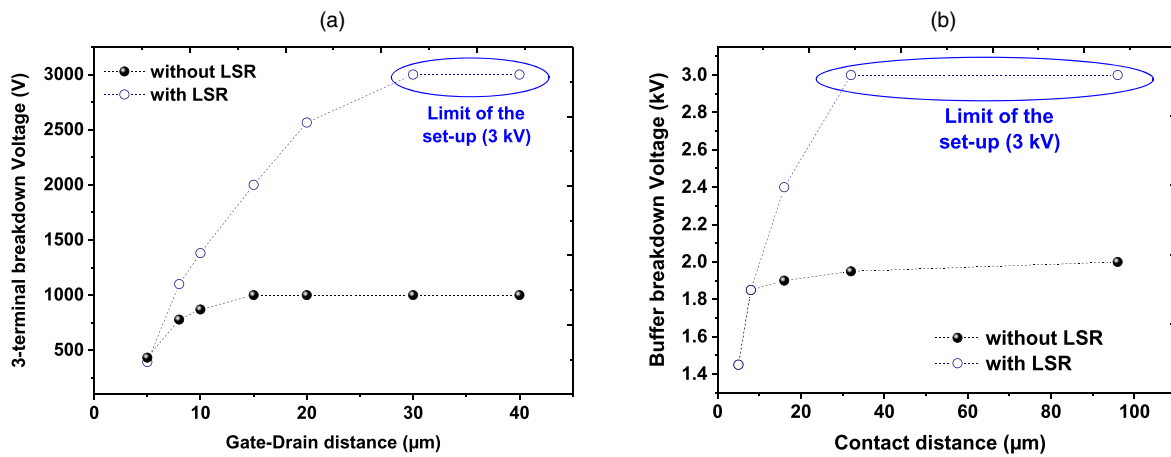
Fig. 3(a). The devices without LSR show a BV plateau around 1000 V due to the buffer thickness limitation. For devices with LSR, the BV as a function of the gate-drain distance increases almost linearly reaching more than 3000 V for large designs ( $L_{\text{GD}} > 30 \mu\text{m}$ ). In the same way, lateral buffer BV conducted on isolated patterns as a function of contact distances with and without LSR show a strong improvement from 1900 V to well above 3000 V [Fig. 3(b)] with a reduction of the leakage current, confirming the suppression of the substrate conductive path contribution.

The substrate bias ramp technique has been shown to be very efficient in order to highlight the trapping effects and related current collapse in GaN-on-Si power switching transistors.<sup>29,30)</sup> As a matter of fact, in properly passivated structures, buffer charge storage is the main source of dynamic on-resistance.<sup>31)</sup> Substrate bias measurements have been performed on a Keysight B1505A Power Device Analyzer. Two ohmic contacts with a spacing of 20  $\mu\text{m}$  have been used and the bias is set at 1 V. By ramping the substrate to a high (negative) potential, mimicking the off-state operation under the drain contact in a transistor, any charge redistribution in the buffer upon reverse bias will change the electric field. As such, the buffer charge trapping or storage will be visible in the substrate ramp characteristic. This approach is surface insensitive and applies a 1-D vertical field. The sweep rate was set to 22  $\text{V s}^{-1}$ . The devices without LSR reveals low hysteresis in the substrate ramps performed up to 600 V [see Fig. 4(a)]. This reflects the excellent material quality and the low charge storage within the heterostructure. Trapping effects are observed above 600 V as seen Fig. 4(b) through 1 kV substrate ramp measurements. Interestingly, the devices with LSR show low hysteresis and thus reduced charge storage all the way to 3000 V [Fig. 4(c)]. This means that the substrate removal followed by the additional thick AlN deposition not only preserve the integrity of a low charge trapping buffer but could also extend significantly the trap-free bias operation capability.

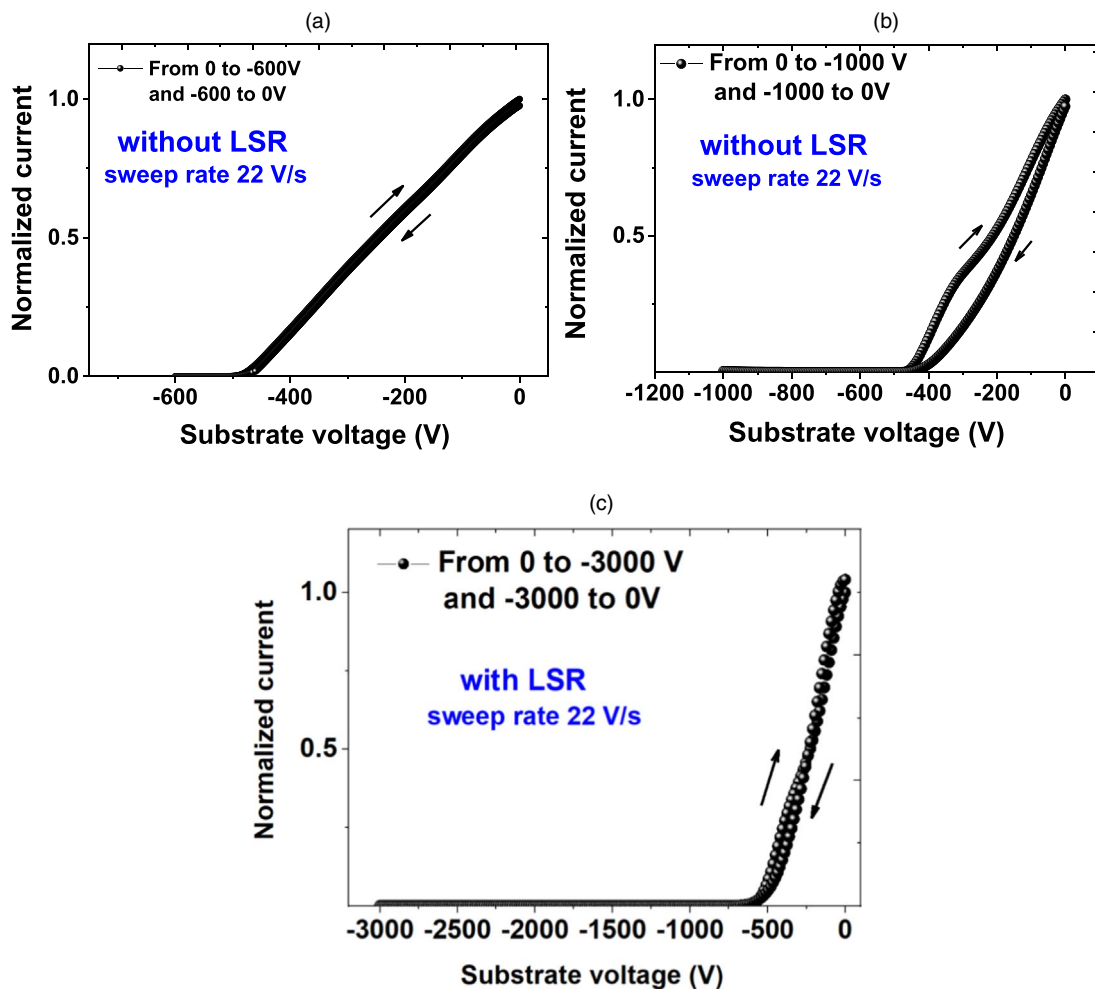
In order to verify these observations and further assess the trapping effects of transistors with and without LSR, we performed back-gating current transient measurements at room temperature on both samples. This technique allows to separate buffer charge trapping effects from surface ones. The measurement procedure is divided into stress and



**Fig. 2.** (Color online) (a)  $I_{\text{D}}-V_{\text{DS}}$  and (b) DC transfer characteristics of AlGaIn/GaN MISHEMTs ( $L_{\text{GD}} = 5 \mu\text{m}$ ) with and without LSR characteristics.



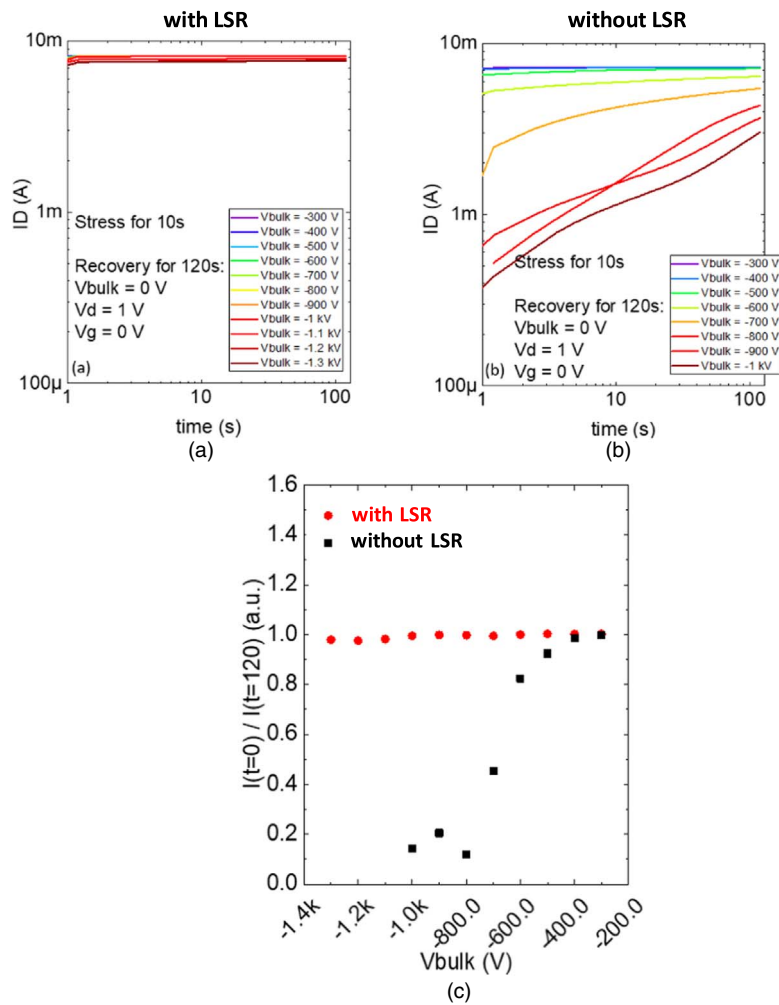
**Fig. 3.** (Color online) (a) Evolution of  $L_{GD}$ -dependent three-terminal breakdown voltage and (b) buffer breakdown versus contact distances of AlGaIn/GaN MISHEMTs with and without LSR.



**Fig. 4.** (Color online) Substrate ramps performed on TLM for the AlGaIn/GaN epitaxial structure (a) at 1000 V without LSR and (b) at 3000 V with LSR.

recovery phases. For the stress phase, the device is kept in trapping conditions for 10 s, during which a high electric field is induced on the buffer, as a result charge trapping occurs mainly in this region. Then, the recovery phase is immediately carried out by keeping the device in rest conditions. The recovery drain current transient is recorded for 120 s. Several bulk bias stresses are tested, from  $-200$  V up to  $-1.3$  kV. During the stress the drain, gate and source terminals are kept at 0 V, whereas during the recovery the drain terminal is at

1 V, the source at 0 V and the gate is at 0 V. The plots of the drain current transients as a function of time for the different bulk bias stress are reported in Figs. 5(a) and 5(b). In agreement with the substrate ramp characterizations, the back-gating measurements show no trapping effects all the way to 1.3 kV for devices with LSR with a monotonic behavior over time regardless of the back bias. On the other hand, the same devices without LSR under similar conditions deliver significant trapping above 600 V. Figure 5(c)



**Fig. 5.** (Color online) Back-gating current transient measurements with various trapping voltages and normalized current after stress as a function of the back bias of AlGaN/GaN MISHEMTs with and without LSR.

summarizes the back-gating transient measurements of devices with and without LSR by showing the normalized current after stress (initial current after stress over current after 120 s recovery) as a function of the back bias. The remarkable monotonic evolution of the current after stress for devices with LSR while observing a drastic drop for devices without LSR within the same wafer show that under high bias most of the electron trapping occurs at the AlN nucleation layer/silicon substrate vicinity.

In conclusion, current collapse characteristics of GaN-based MISHEMTs with and without LSR followed by thick PVD AlN and Cu deposition were investigated on the same wafer. Trapping effects directly affecting the dynamic behavior of power switching transistors have been studied by means of high voltage substrate ramps as well as back-gating current transient measurements. This work demonstrates that the substrate removal approach not only enables the drastic extension of operation voltage capabilities of GaN-on-Silicon HEMTs but also potentially enables a drastic trapping reduction. This key additional benefit provided by the LSR approach is attributed to the removal of the interface between the AlN nucleation layer and the silicon substrate. Further removal of the full AlN nucleation layer and eventually part of the transition layers may allow GaN devices with current collapse-free operating well-beyond 1 kV. These results show that power applications above 1000 V covered currently by SiC and silicon-based devices

could benefit from the high electron mobility offered by GaN-on-silicon heterostructures enabling much lower  $R_{ON}$ .

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