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Reliable Technology Evaluation of SiGe HBTs and MOSFETs: f_{MAX} Estimation from Measured Data

Bishwadeep Saha, Sébastien Frégonese, Bernd Heinemann, Patrick Scheer, Pascal Chevalier, Klaus Aufinger, Member, IEEE, Anjan Chakravorty, Member, IEEE and Thomas Zimmer, Senior Member, IEEE

Abstract—Maximum oscillation frequency (f_{MAX}) of mmwave transistors is one of the key figures of merit (FOMs) for evaluating the HF-performance of a given technology. However, accurate measurements of f_{MAX} are very difficult. Determination of f_{MAX} is significantly affected by the measurement uncertainties in the admittance (y) parameters. In order to get rid of the random measurement error and to obtain a reliable and stable f_{MAX} value, the frequency dependent y-parameters are described by rational functions formulated from the smallsignal hybrid π -model of the transistor under investigation. The parameters of these functions are determined following a least square error technique that minimizes the functional error with the measured data. The approach is especially useful for a fast and reliable evaluation of f_{MAX} value. Devices from two different SiGe and an FDSOI (Fully Depleted Silicon On Insulator) MOS technology are measured and stable f_{MAX} values are estimated following this approach.

Index Terms—SiGe HBTs; MOS; y-parameters; maximum oscillation frequency; analytical modeling; small-signal model.

I. INTRODUCTION

T HE demand for increased functionality and speed of modern communication system drives the evaluation of various transistor technologies [1]. These unique technologies differ from one another in terms of doping profiles, geometries and structures. In this rapid development, heterojunction bipolar transistors (HBTs) or advanced CMOS technologies find applications in millimeter and sub-millimeter wave frequency range [2], [3], [4], [5]. In this region of applications, realizations of power amplifiers and low noise amplifiers are limited by transit frequency (f_T) and maximum oscillation frequency (f_{MAX}). Also to achieve the required functionality, f_T and

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 f_{MAX} should be at least three to four times higher than the operating frequency. The present state-of-the-art SiGe HBTs are shown to have f_T above 500 GHz and f_{MAX} above 720 GHz at room temperature [6]. Additional studies reveal that these parameter values are heading towards terahertz level [7], [8]. For a trustworthy evaluation of such a technology under development, it would be very useful to have a quick and reliable estimation methodology for the corresponding f_T and f_{MAX} .

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Traditionally, f_{MAX} is extrapolated to zero from U(f) characteristics as demonstrated in [9], [10] with U being the Mason's gain [11] expressed in two-port parameters as

$$U = \frac{|y_{21} - y_{12}|^2}{4[Re\{y_{11}\}Re\{y_{22}\} - Re\{y_{12}\}Re\{y_{21}\}]}.$$
 (1)

In [10], a single pole transfer function is fitted to U(f) allowing to determine f_{MAX} by the intercept of the fitted line with the x-axis. In both the works, the extrapolated f_{MAX} values are more than 1 decade higher than the measurement range. It is well known that the extrapolation is very sensitive to the measurement noise. Hence, the extrapolated values are prone to under- or overestimation from the actual value. An alternative method [5], [6], [12] to obtain the f_{MAX} is to use the approximation

$$f_{MAX} = f\sqrt{U} \tag{2}$$

where f is the frequency of measurement.

In a first approximation f_{MAX} is supposed to be independent of frequency since U varies inversely with the square of frequency in (2). It appears that f_{MAX} starts to decrease slightly from the mid-frequency range where the -20 dB/decade roll-off approximation of the power gain is no more valid. This decrease is mainly due to the influence of the substrate capacitance; and depending on the technology, its influence is more or less pronounced. Other second order effects can also play a role in the decrease of f_{MAX} when the measured frequency approaches f_{MAX} value. But even in the lower frequency range, it is quite difficult to obtain a nearly constant frequency-independent f_{MAX} using (2) mainly because of the extremely low magnitude and measurement uncertainty of some of the measured y-parameters [13], [14]. Recently a study has been carried out in [15] showing the uncertainty in extracting the f_{MAX} in the low frequency regime (below 80 GHz) for the two most advanced CMOS processes.

As a consequence, the extracted f_{MAX} is very noisy over frequency. Such a fluctuation poses serious confusion to the technologist while evaluating and optimizing a given technology. Very often, an already obtained performance improvement is masked by the measurement and estimation error in f_{MAX} ; subsequently an unambiguous announcement of the actually obtained technology advancement is hindered. Hence, it is desirable to adopt a strategy that quickly estimates a frequencyindependent f_{MAX} even from a noisy experimental data.

In this paper, first we develop analytical formulations of yparameters based on small-signal hybrid π -model (presented in section II). Then we extract the parameters used in the formulations by properly interpolating the measured data. Subsequently we apply these formulations to extract f_{MAX} using (2) (detailed in section III). Since the analytical formulations are not prone to noise, this approach yields reliable values for f_{MAX} over the entire range of frequency at which measurement is carried out. The limitations of this method have been discussed in section IV and finally, we conclude in section V.

A. Case study

In order to highlight the need for reliable f_{MAX} determination method, we consider some specific HBT structures (with thermally aware BEOL design) realized in a state-of-theart SiGe BiCMOS HBT technology from Infineon (B11HFC) having an f_T = 250 GHz, f_{MAX} = 370 GHz and 6 levels of metallization [16]. The investigated test structures consist of a transistor cell having specially designed metal stacks in the BEOL, which act as heat spreaders, as can be observed in Fig. 1 (left). The test-structures under study are designed in-house and consist of a single transistor having a CBEBC arrangement for the contacts and are connected in common emitter configuration. Different configurations for BEOL metallization upon the active part of the component have been fabricated. For the first set of test structures the metal bars are stacked one on top of the other and connected by vias; the additional metal dummies have a gradually increasing width till 1.52 μ m for the M4_{wide} structure as shown in Fig. 1 (left). These structures are named as M2wide, M3wide and M4wide, where the number stands for the level of the last metal stack that is added and M indicates that the metal dummies are placed above the emitter contact. A complete DC and RF electrical characterization is performed on this test structures (and de-embedded using the same open and short structures for all the transistors under study) in order to investigate the performance improvements. The results for the f_{MAX} determination using (1) and (2) are plotted in Fig. 1 (right). Although we can identify an impact of the contact configuration, a clear assessment is not possible due to the noisy nature of the data.

II. ANALYTICAL FORMULATIONS AND PARAMETER EXTRACTION

The noisy f_{MAX} has its origin from the measured yparameters, in particular from $Re\{y_{12}\}$ and $Re\{y_{22}\}$. Now to minimize the measured noise and to form the analytical relationship of the admittance parameters, we have used a small-signal hybrid π -model [17] as a vehicle and the following formulations are interpolated over measured data using



Fig. 1. 3D representation of the $M4_{wide}$ test structure with drawn emitter window 5 μ m x 0.34 μ m (left) and frequency-dependent f_{MAX} for the different BEOL contact configurations (right).



Fig. 2. Frequency-dependent admittance parameters for 130 nm BiCMOS SiGe HBT 8x (0.105 μ m x 1 μ m) biased at V_{BE} = 0.89 V and V_{CB} = 0.25 V and 55 nm BiCMOS SiGe HBT (0.09 μ m x 4.8 μ m) biased at V_{BE} = 0.88 V and V_{CB} = 0.5 V and 28 nm FDSOI MOS transistor (on right y-axis) biased at V_{GS} = 0.6 V and V_{DS} = 1 V unit.

least-mean square technique. The formulations in the form of rational functions are expressed as (with angular frequency, ω and ij = 11, 12, 21 and 22)

$$\operatorname{Re}\{y_{ij}\} \simeq \frac{a_{1,ij} + a_{2,ij}\omega^2}{1 + a_{3,ij}\omega^2},\tag{3}$$

$$\operatorname{Im}\{y_{ij}\} \simeq \frac{b_{1,ij}\omega}{1 + b_{2,ij}\omega^2}.$$
(4)

Note that for $Re{y_{12}}$, $a_{1,12} = 0$. The determination of the parameters appearing in (3) and (4) are straight-forward and done in the following way. First, the technique of division of polynomial is performed to normalize with respect to the first term in the denominator up to second order in ω since we have observed that even higher order terms contribute insignificantly over the characteristics. Then the quadratic regression is applied to obtain the parameters. The advantages of this procedure are that (i) the interpolated *y*-parameters are obtained immediately and (ii) the measurement noise is eliminated. Also the use of optimization procedure such as the well-known Levenberg-Marquardt algorithm yields comparable results.

III. RESULTS AND DISCUSSIONS

To test the utility of the closed-form equations, small-signal *s*-parameter measurements of SiGe HBT are performed on two different technologies. One of them represents an intermediate status of HBT developments within the DOTSEVEN project [16] based on a 130 nm BiCMOS platform. The corresponding 8-fingers transistor with an effective emitter area of $8 \times (0.105 \ \mu m \times 1 \ \mu m)$ is biased at $V_{CB} = 0.25$ V and $V_{BE} = 0.89$ V. The second technology concerns a 55 nm BiCMOS platform [18] and the corresponding SiGe HBT with an effective emitter area of $0.09 \ \mu m \times 4.8 \ \mu m$ is biased at $V_{CB} = 0.5$ V and $V_{BE} = 0.88$ V. Measurements of both the devices are carried out from 1 GHz to 67 GHz using Agilent network analyzer (E8361A) and Agilent DC source (E5270B).

To calibrate the network analyzer, off-wafer SOLT (Short-Open-Load-Through) calibration has been performed on Impedance Standard Substrate followed by an on-wafer OPEN-SHORT de-embedding to remove the effect of pad capacitance and feeding inductance [12], [19]. The generality of this work is also verified by employing measured data from 28 nm FDSOI technology [20]. The measured MOS transistor contains 40 fingers of 0.5 μ m width and nominal gate length of 30 nm. To measure the s-parameters, off-wafer SOLT calibration on Impedance Standard Substrate along with the on-wafer Pad-Short-Open de-embedding [21] was carried out from 1 GHz to 67 GHz. Fig. 2 shows the interpolation results for the y-parameters from all three technologies using equation (3) and (4). Fig. 3 (above) shows the f_{MAX} value obtained from the interpolated y-parameters for the three technologies. Fig. 3 (below) also shows the f_{MAX} results obtained from the interpolation for the technology flavors as presented in Fig. 1. It is observed that the use of the analytical formulations discussed in section II results in a clear technology assessment concerning the improvement obtained by the addition of BEOL metals.

IV. LIMITATIONS

The proposed method is valid if the measured *s*-parameters have only random measurement errors but no systematic measurement errors. Even in the latest measurement



Fig. 3. Frequency-dependent f_{MAX} for 130 nm BiCMOS SiGe HBT 8x (0.105 μ m x 1 μ m) biased at $V_{BE} = 0.89$ V and $V_{CB} = 0.25$ V and 55 nm BiCMOS SiGe HBT (0.09 μ m x 4.8 μ m) biased at $V_{BE} = 0.88$ V and $V_{CB} = 0.5$ V and for 28 nm FDSOI MOS transistor (on right y-axis) biased at $V_{GS} = 0.6$ V and $V_{DS} = 1$ V (above) and frequency-dependent f_{MAX} for the different BEOL contact configurations obtained by interpolated y-parameters (below).

equipment, systematic errors can be observed due to coupling of the probes with the wafer surface for a given frequency range [22]. Accordingly, the frequency range in which the elimination of the systematic measurement error is guaranteed, this approach can be used. Moreover, the operator must be very careful to avoid any probe positioning mismatch and to ensure reliable and repeatable pad contacts.

V. CONCLUSIONS

In this work, we have demonstrated an approach to predict f_{MAX} by formulating analytical equations of admittance parameters $(y_{11}, y_{12}, y_{21}, y_{22})$ based on the small-signal hybrid π -model. The proposed approach addresses the problem of predicting f_{MAX} in the low frequency regime in spite of noisy measurement data. To that aim the least mean square based interpolation technique is applied to obtain the most reliable estimation in contrast to the traditional method that is very sensitive to the measurement noise. Our approach also takes care of the f_{MAX} roll-off mainly observed in the high frequency regime which can not be obtained following the conventional f_{MAX} extraction from the unilateral gain versus frequency characteristics with a fitting line having a slope of -20 dB/decade. Observations carried on 130 nm and 55 nm BiCMOS as well as on 28 nm FDSOI technologies lead to the conclusion that the use of rational function in the Mason's gain formula can provide accurate, robust and reliable estimation of f_{MAX} . This is extremely important for a reliable assessment of a technology under evaluation. However, there is still some uncertainty in the f_{MAX} value estimated from the low frequency measurements. In order to obtain the true f_{MAX} value, measurement beyond 100 GHz (close to the f_{MAX}) needs to be carried out.

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