



**HAL**  
open science

## High-Speed and Low-Energy Dual-Mode Logic based Single-Clock-Cycle Binary Comparator

Ricardo Escobar, Luis Miguel Procel, Lionel Trojman, Marco Lanuzza,  
Ramiro Taco

► **To cite this version:**

Ricardo Escobar, Luis Miguel Procel, Lionel Trojman, Marco Lanuzza, Ramiro Taco. High-Speed and Low-Energy Dual-Mode Logic based Single-Clock-Cycle Binary Comparator. IEEE LASCAS 2021, Feb 2021, Arequipa, Peru. pp.1-4, 10.1109/LASCAS51355.2021.9459151 . hal-03107004

**HAL Id: hal-03107004**

**<https://hal.science/hal-03107004v1>**

Submitted on 12 Jan 2021

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

# High-Speed and Low-Energy Dual-Mode Logic based Single-Clock-Cycle Binary Comparator

Ricardo Escobar<sup>1</sup>, Luis Miguel Prócel<sup>1</sup>, Lionel Trojman<sup>1,2</sup>, Marco Lanuzza<sup>1,3</sup> and Ramiro Taco<sup>1</sup>

<sup>1</sup>*Instituto de Micro y Nanoelectrónica (IMNE), Universidad San Francisco de Quito (USFQ)*

Email: rpescobar@estud.usfq.edu.ec; lprocel@usfq.edu.ec; rtaco@usfq.edu.ec

<sup>2</sup>*Laboratoire d'Informatique, Signal, Image, Télécommunication et Électronique (LISITE), Institut Supérieur d'Électronique de Paris (ISEP)*

Email: lionel.trojman@isep.fr

<sup>3</sup> *Dipartimento di Ingegneria Informatica, Modellistica, Elettronica e Sistemistica (DIMES), Università della Calabria*

Email: lanuzza@deis.unical.it

**Abstract**—This paper presents an energy-efficient single-clock-cycle binary Dual-Mode Logic (DML)-based comparator optimized to operate in the dynamic mode. The parallel-prefix architecture is implemented to ensure high speed, whereas low power consumption is guaranteed by reducing the switching activities of internal nodes. Domino Logic (DL) and DML implementations are compared in terms of delay and energy for different supply voltages in the 32 nm technology. We demonstrate an average improvement of 5% in both energy and delay when the DML design is operating in the dynamic mode compared to its conventional domino counterpart. Moreover, the DML design operating in the static mode allows to save up to 43% energy consumption compared to the equivalent domino logic-based implementation.

**Index Terms**—Dual mode logic; CMOS; binary comparator; arithmetic circuits

## I. INTRODUCTION

Binary magnitude comparators are largely used in modern digital circuits. Comparators are key-component in Arithmetic Logic Units [1]. It is mainly used for processing and sort data in communication systems such as LDPC and MIMO decoders algorithms which require extensive iterations of binary comparison [2]. The number of iterations in a LDPC decoder is determined by the noise in the channel that varies during time thus a Bit Error Rate (BER) performance-aware LDPC decoders with built-in adaptive digital circuits could enable an energy-performance optimization on the fly [3]. Since the operation of binary magnitude comparator is largely used in modern digital communication systems it is necessary to utilize on-the-fly energy-speed adaptive designs.

Conventionally, high performance binary comparison is achieved by a high speed adder. In [4] a tree-based comparator is proposed where Manchester structures are used with dynamic logic. In [5] and [6] high speed is achieved by combining bit-wise competition logic (BCL) and priority encoding algorithm (PE) respectively, also with dynamic logic. Although, dynamic logic has demonstrated superior performance compared to static logic, it is not suitable for energy-efficient operation because of high activity factor [7], [8]. Additionally, energy savings through low voltage

operation (i.e. near/sub threshold) is not feasible due to undesired charge/discharge voltage in the dynamic node at low frequencies [9].

The Dual-Mode Logic (DML) proposed in [10] allows digital circuits to achieve either high performance or low energy consumption at the run-time [11]. This is achieved thanks to the flexibility of a DML gate to operate either in dynamic mode (high speed) or static mode (low energy) according to the computational workload.

In this paper, a parallel prefix single-clock-cycle binary comparator based in DML has been designed in 32 nm bulk technology. The proposed DML comparator achieves higher speed operation compared to state of the art design and offers an additional low energy operation mode. The DML comparator shows an improvement of 5% in speed and 43% energy savings operating in dynamic mode and static mode respectively. Furthermore postlayout simulations for process and temperature variations demonstrate that advantage of DML is maintained for a wide range of voltage.

In this work, section II describes basics of DML and Parallel prefix comparator. In section III discusses DML implementation of the single clock binary comparator, Section IV shows post-layout simulation results under nominal conditions and PVT variations. Finally, in the last section the main conclusions are addressed.

## II. BACKGROUND

### A. Dual Mode Logic

The distinctive characteristic of a DML gate is the possibility to operate in two different modes, either static or dynamic modes. In dynamic mode operation, high performance is achieved at expense of high energy consumption. In the static mode, lower energy is consumed at the expense of lower performance. When the DML gate operates in the static mode, the clock (CLK) is disabled, thus retaining the functionality of its static CMOS core. When the CLK is enabled, the DML gate runs in the dynamic mode by alternating the pre-charge/discharge and evaluation operating phases via CLK toggling [12]–[14].

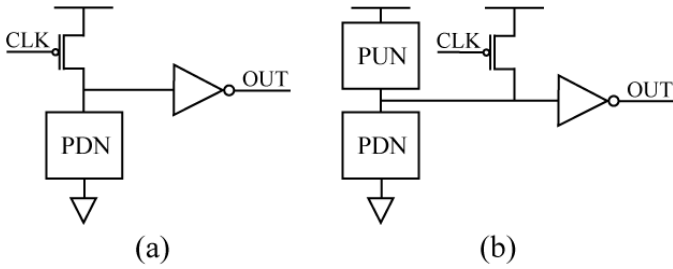


Fig. 1. Schematics of generic (a) Domino and (b) DML gates.

As shown in Fig. 1 (b), contrary to the conventional domino gate shown in Fig. 1 (a), during the evaluation phase the output node of a DML gate is never floating thus robust operation is guaranteed at low voltages [9].

### B. Parallel-Prefix algorithm

In a comparison between two n-bit numbers A and B, the carry out signal will be equal to a logic 1 if  $A \geq B$  or 0 if  $A < B$ . The parallel-prefix algorithm compute only the carry bits required to evaluate the final carry out.

For a 64 bit comparator, the pre-processing stage takes 128 bits corresponding to the two numbers. The i-th processing element (PE) will compute the signals generate (GG) and propagate (GP). These signals will take their values based on the following rules:

$$GP_{[i]} = 1 \text{ if } A_{[2i+1:2i]} = B_{[2i+1:2i]} \text{ else } GP_{[i]} = 0$$

$$GG_{[i]} = 1 \text{ if } A_{[2i+1:2i]} < B_{[2i+1:2i]} \text{ else } GG_{[i]} = 0$$

A total of 32 PE will be needed to compute the GG and GP signals. The logic expression for each gate can be found by the truth table and it leads to:

$$GG_{[i]} = B_{[2i+1]} \cdot [B_{[2i]} \cdot (A_{[2i]} \oplus B_{[2i]}) + \overline{A_{[2i+1]}} \cdot (A_{[2i+1]} \oplus B_{[2i+1]})] + B_{[2i]} \cdot \overline{A_{[2i+1]}} \cdot (A_{[2i]} \oplus B_{[2i]}) \quad (1)$$

$$GP_{[i]} = \overline{A_{[2i+1]} \oplus B_{[2i+1]}} \cdot \overline{A_{[2i]} \oplus B_{[2i]}} \quad (2)$$

The parallel recursive stage takes 32 GG and GP signals corresponding to the outputs of the previous stage. The i-th DOT operator will compute the signals grouped-generate (GGG) and grouped-propagate (GGP). These signals will take their values based on the following rules:

$$GGG_{[i]} = 0 \text{ and } GGP_{[i]} = 0 \text{ if } A_{[4i+3:4i]} > B_{[4i+3:4i]}$$

$$GGG_{[i]} = 1 \text{ and } GGP_{[i]} = 0 \text{ if } A_{[4i+3:4i]} < B_{[4i+3:4i]}$$

$$GGG_{[i]} = 0 \text{ and } GGP_{[i]} = 1 \text{ if } A_{[4i+3:4i]} = B_{[4i+3:4i]}$$

A total of 8 DOT operators are needed to compute the GGG and GGP signals. The logic expression for each gate can be found by the truth table and it leads to:

$$GGG_{[i]} = GG_{[4i+3]} + \sum_{k=0}^2 (GG_{[4i+k]} \cdot \prod_{l=k+1}^3 GP_{[4i+l]}) \quad (3)$$

$$GGP_{[i]} = \prod_{l=0}^3 GP_{[4i+l]} \quad (4)$$

The Post-processing stage consists of two logic levels, 2 DOT operators on the first logic level, and 2 OUT gates where each one computes one output of the device. The logic equations of the OUT signals can be expressed as:

$$OUT_{[0]} = G_2 + G_1 \cdot P_2 \quad (5)$$

$$OUT_{[1]} = P_1 \cdot P_2 \quad (6)$$

Where the signals G and P are the products of the 2 DOT operators. The parallel-prefix algorithm does not permit the condition  $OUT_{[0]} = OUT_{[1]} = 1$ . Therefore, there are only three possible outputs that correspond to the comparison of the two numbers A and B. These outputs are:

$$OUT_{[0]} = 0 \text{ and } OUT_{[1]} = 0 \text{ if } A_{[63:0]} > B_{[63:0]}$$

$$OUT_{[0]} = 1 \text{ and } OUT_{[1]} = 0 \text{ if } A_{[63:0]} < B_{[63:0]} \quad (7)$$

$$OUT_{[0]} = 0 \text{ and } OUT_{[1]} = 1 \text{ if } A_{[63:0]} = B_{[63:0]}$$

### III. DUAL MODE LOGIC BASED SINGLE-CLOCK-CYCLE BINARY COMPARATOR

The top-level architecture of the implemented DML comparator is based on the computational architecture demonstrated in [4] and here shown in Fig. 2. Inherent from Domino logic the DML based comparator is also able to perform within a single clock cycle, the signals GGG and GGP are latched [15]–[17], and Post Processing Stage evaluates during the clock low half-cycle. In the static mode the latch is transparent to the clock signal.

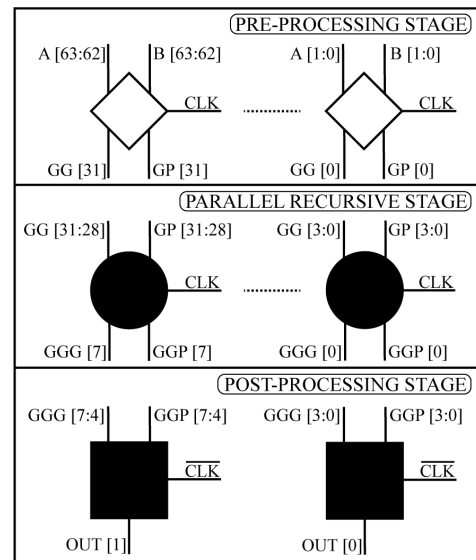


Fig. 2. Top-level architecture of the full comparator.

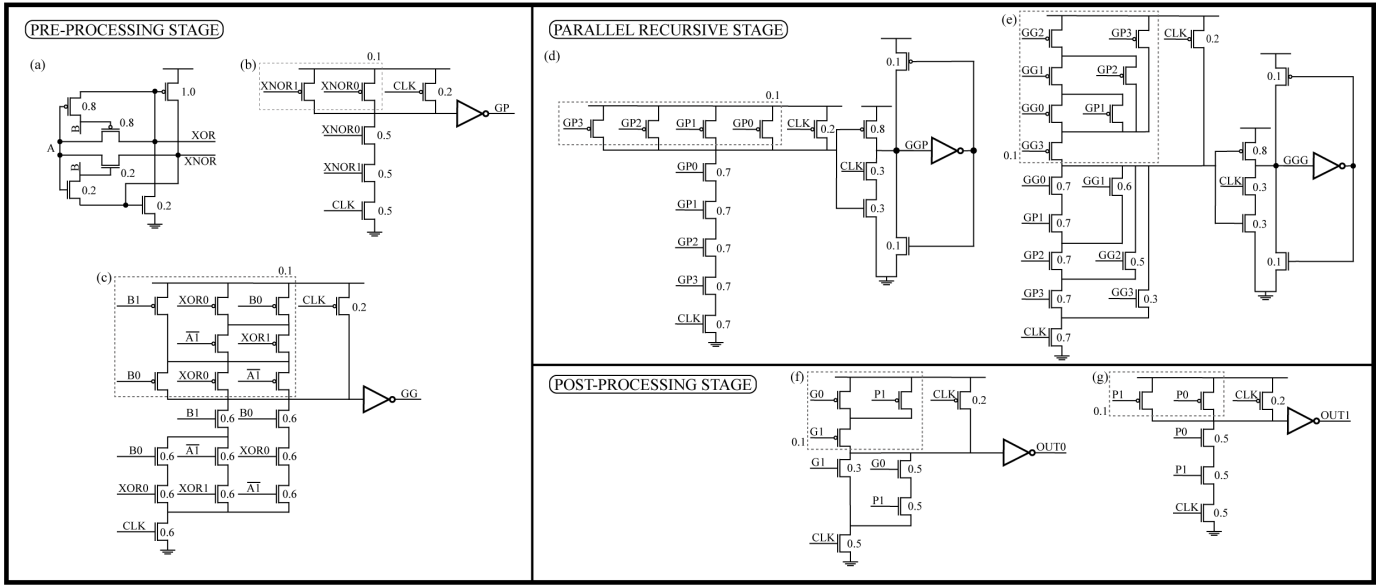


Fig. 3. Transistor level schemes of the gates needed to implement the DML-based binary comparator with the sizing for every transistor in  $[\mu\text{m}]$ : a) pass transistor implementation of the XOR/XNOR gate b) propagate gate (GP) c) generate gate (GG) d) grouped propagate gate (GGP) e) grouped generate gate (GGG) f,g) OUT gates

Fig. 3 shows transistor-level schemes for each gate that conforms the full comparator implemented with DML. The PE has static pass-transistor-based XOR/XNOR gates to decrease the amount of transistors in series, to avoid using inverters for the signal  $A[2i+1]$ . All pre-charging transistors driven by the CLK signal are  $0.2\mu\text{m}$  wide to ensure that the pre-charge is less than the evaluation delay. For all gates, the width of the NMOS transistors within the PDN were chosen to make the evaluation path equivalent to a  $0.2\mu\text{m}$  wide NMOS transistor and the width of the PMOS transistors within the PUN were set  $0.1\mu\text{m}$ .

#### IV. SIMULATION RESULTS

Simulations were performed for the typical (nmos) - typical (pmos) process corner at  $25^\circ\text{C}$  for a range of voltages from  $0.5\text{ V}$  to  $1.2\text{ V}$  nominal supply voltage. Similar to [18], registers control the input signals and each output node of the comparator has been loaded with a 4x D-type Flip-Flop.

The E-D comparison is shown in Fig. 4. When the DML implementation is operating on dynamic mode, it outperforms the Domino logic implementation by an average of 5% in speed and energy per operation, leading to an average EDP reduction of 9%. This improvement is obtained at the expense of a reasonable 25% increase on the transistor count. However, this is not reflected in the total occupied area ( $787\mu\text{m}^2$ ) essentially due to the minimum sized PMOS transistors in DML gates [11]. Relative advantages of our design operating in the DML dynamic mode are shown in Fig. 5.

Finally, the proposed comparator was also investigated from the point of view of the delay and energy variability due to process variation. Table I summarizes the mean ( $\mu$ ) and standard deviation ( $\sigma$ ) of energy and delay variation

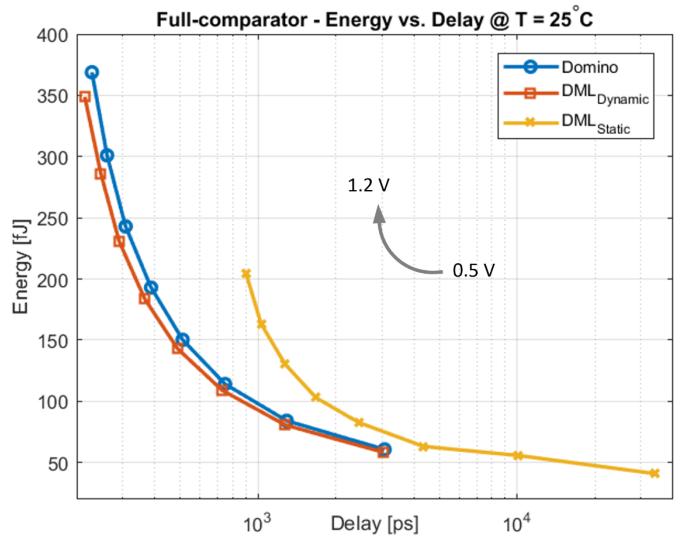


Fig. 4. ED comparison for the DML and Domino logic implementations.

measured through 1000 Monte Carlo simulation runs at  $1\text{ V}$  nominal supply voltage for the typical process corner at  $25^\circ\text{C}$ . The results demonstrate high robustness of DML implementation to process variations.

TABLE I  
MONTE CARLO RESULTS OF THE COMPARATOR DELAY AND ENERGY

	Delay		Energy	
	$\mu$ [ps]	$\sigma$ [ps]	$\mu$ [fJ]	$\sigma$ [fJ]
Domino	309.49	10.38	238.58	3.26
DML dynamic	292.58	11.18	226.94	3.40
DML static	1395.31	81.48	131.27	3.08

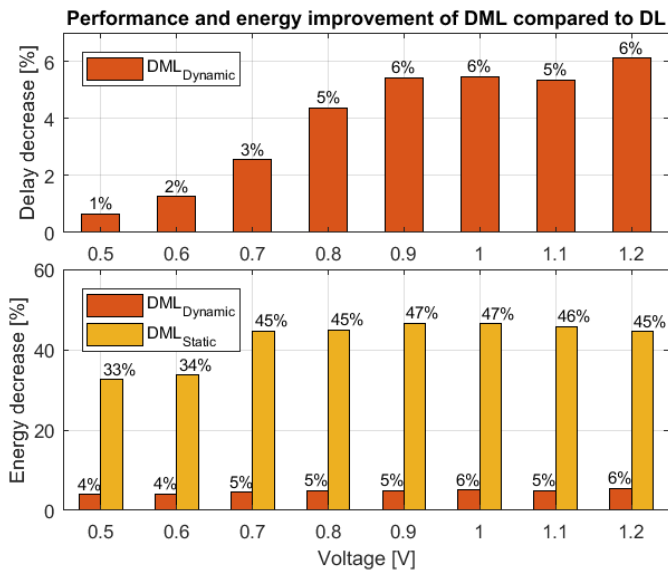


Fig. 5. Energy-Delay DML advantages over Domino logic implementation

## V. CONCLUSIONS

A high-speed energy-efficient parallel-prefix binary full comparator designed with the DML design style has been presented with the goal to explore its performance for different supply voltages and its robustness to process variations. The parallel-prefix algorithm was implemented in a way that the switching activities of internal nodes is reduced and also some possible short-circuits have been prevented from previous designs, therefore the energy consumption decreases significantly. As a consequence, DML implementation operating in the dynamic mode outperforms the Domino logic-based implementation by an average of 5% in speed and energy savings, thus leading to an average EDP reduction of 9%. DML design also allows a static mode of operation to achieve an average energy dissipation reduction of 43%.

## ACKNOWLEDGMENT

The authors would like to thank Sara Benedictis and Kevin Vicuña for their constructive comments and discussions.

## REFERENCES

- [1] S.-M. Kang and Y. Leblebici, "Cmos integrated circuits: Analysis and design," 2003.
- [2] M. Shabany and P. G. Gulak, "A 0.13  $\mu\text{m}$  cmos 655mb/s  $4 \times 4$  64-qam k-best mimo detector," in *2009 IEEE International Solid-State Circuits Conference-Digest of Technical Papers*. IEEE, 2009, pp. 256–257.
- [3] X. Zhao, Z. Chen, X. Peng, D. Zhou, and S. Goto, "A ber performance-aware early termination scheme for layered ldpc decoder," in *2010 IEEE Workshop On Signal Processing Systems*. IEEE, 2010, pp. 416–419.
- [4] F. Frustaci, S. Perri, M. Lanuzza, and P. Corsonello, "A new low-power high-speed single-clock-cycle binary comparator," in *Proceedings of 2010 IEEE International Symposium on Circuits and Systems*. IEEE, 2010, pp. 317–320.
- [5] J.-Y. Kim and H.-J. Yoo, "Bitwise competition logic for compact digital comparator," in *2007 IEEE Asian Solid-State Circuits Conference*. IEEE, 2007, pp. 59–62.

- [6] C.-H. Huang and J.-S. Wang, "High-performance and power-efficient cmos comparators," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 2, pp. 254–262, 2003.
- [7] N. H. Weste and D. Harris, *CMOS VLSI design: a circuits and systems perspective*. Pearson Education India, 2015.
- [8] P. Chuang, D. Li, and M. Sachdev, "A low-power high-performance single-cycle tree-based 64-bit binary comparator," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 59, no. 2, pp. 108–112, 2012.
- [9] L. Yavits, R. Taco, N. Shavit, I. Stanger, and A. Fish, "Dual mode logic address decoder," in *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2020, in press.
- [10] A. Kaizerman, S. Fisher, and A. Fish, "Subthreshold dual mode logic," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 21, no. 5, pp. 979–983, 2012.
- [11] I. Levi and A. Fish, "Dual mode logic—design for energy efficiency and high performance," *IEEE access*, vol. 1, pp. 258–265, 2013.
- [12] R. Taco, I. Levi, M. Lanuzza, and A. Fish, "An 88-fj/40-mhz [0.4 v]–0.61-pj/1-ghz [0.9 v] dual-mode logic  $8 \times 8$  bit multiplier accumulator with a self-adjustment mechanism in 28-nm fd-soi," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 2, pp. 560–568, 2018.
- [13] N. Shavit, I. Stanger, R. Taco, M. Lanuzza, and A. Fish, "A 0.8 v, 1.54 pj/940 mhz dual mode logic-based 16x16-bit booth multiplier in 16-nm finfet," *IEEE Solid-State Circuits Letters*, 2020.
- [14] I. Stanger, N. Shavit, R. Taco, M. Lanuzza, and A. Fish, "Silicon evaluation of multimode dual mode logic for pvt-aware datapaths," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 9, pp. 1639–1643, 2020.
- [15] M. Lanuzza, R. De Rose, F. Frustaci, S. Perri, and P. Corsonello, "Comparative analysis of yield optimized pulsed flip-flops," *Microelectronics Reliability*, vol. 52, no. 8, pp. 1679–1689, 2012.
- [16] M. Lanuzza, "A simple circuit approach to improve speed and power consumption in pulse-triggered flip-flops," *Journal of Low Power Electronics*, vol. 9, no. 4, pp. 445–451, 2013.
- [17] M. Lanuzza, R. De Rose, F. Frustaci, S. Perri, and P. Corsonello, "Impact of process variations on flip-flops energy and timing characteristics," in *2010 IEEE Computer Society Annual Symposium on VLSI*. IEEE, 2010, pp. 458–459.
- [18] F. Frustaci, S. Perri, M. Lanuzza, and P. Corsonello, "Energy-efficient single-clock-cycle binary comparator," *International Journal of Circuit Theory and Applications*, vol. 40, no. 3, pp. 237–246, 2012.