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# Technology Route towards SiC Thyristor Devices with Amplifying Gate Design

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Silicon carbide (SiC) is a wide-bandgap semiconductor material of great interest for very high power and pulsed power electronics. In this context, the thyristor is the device of choice due to its bipolar conduction, low conduction losses, and high-current handling capabilities. In order to make use of SiC thyristors in pulsed power electronic systems, their power handling capabilities need to be further increased. This can be achieved by both implementing larger device area and parallel connection of devices. In both cases, optical triggering as recently demonstrated in a joint cooperation of ISL and Ampère Laboratory by using SiC thyristors is an advantageous technology to eliminate a source of electromagnetic interference and to facilitate the control of high-voltage device stacks.

In view of the tremendous progress made in SiC crystal quality and wafer size, large-area SiC thyristors become more and more feasible. One major challenge along this route, however, is the development of advanced gate structures. For electrical as well as optical triggering, the amplifying gate is state of the art in silicon (Si) thyristor technology and thus needs to be thoroughly revamped for SiC thyristors: in this context, a device conception was set up for 1.2 kV amplifying gate thyristor (AGT) structures with mesa termination and optimized based on two-dimensional numerical simulations (both using mixed-mode and finite-element methods). Mixed-mode simulations successfully demonstrated the amplifying gate turn-on by means of conventional thyristors. Fabrication of functional thyristor devices  $3 \times 3 \text{ mm}^2$  in size on 100-mm epi-wafer level was demonstrated for the present by means of forward conducting and reverse blocking behavior between gate and anode regions, see figure 1 and 2.

Prior to that, optimization of thyristor termination geometries, process development critical to wafer processing, and characterization of intrinsic material and device parameters were subject to intense investigations at ISL: using the innovative graded-etched junction termination extension (JTE) a breakdown voltage of 8 kV was accomplished for the first time ever in connection with a non-implanted termination of SiC gate turn-off (GTO) thyristors. This high blocking voltage is close to the optimum of the individual epi-wafer capability. On-state characteristics revealed stable operation at repetitive current stress up to 15 A (equivalent to  $800 \text{ A/cm}^2$ ); pulse current characteristics demonstrated that the typical device under test sustains a current pulse of 20  $\mu\text{s}$  as high as 200 A and  $10 \text{ kA/cm}^2$ , respectively.

Together with its cooperation partner Ampère Laboratory, ISL was the first to demonstrate optical triggering of SiC thyristors using UV LEDs. Functional demonstrators were designed, fabricated, and experimentally characterized with respect to their static and pulse current capabilities: blocking voltages as high as 6.3 kV were accomplished while pulse current densities were demonstrated in two different settings with  $4 \text{ kA/cm}^2$  (referring to a pulse width of 650  $\mu\text{s}$ ) and  $15.6 \text{ kA/cm}^2$  (10  $\mu\text{s}$ ). This definitely shows their performance is comparable to electrically triggered SiC thyristors and, particularly, applications taking advantage of Si light-triggered thyristors today will be able to benefit from the use of SiC. In conclusion, herewith, a technology platform becomes available at ISL which allows for developing SiC devices for operational purposes such as high temperature, harsh environment, and ultra-high (> 10 kV) voltages.

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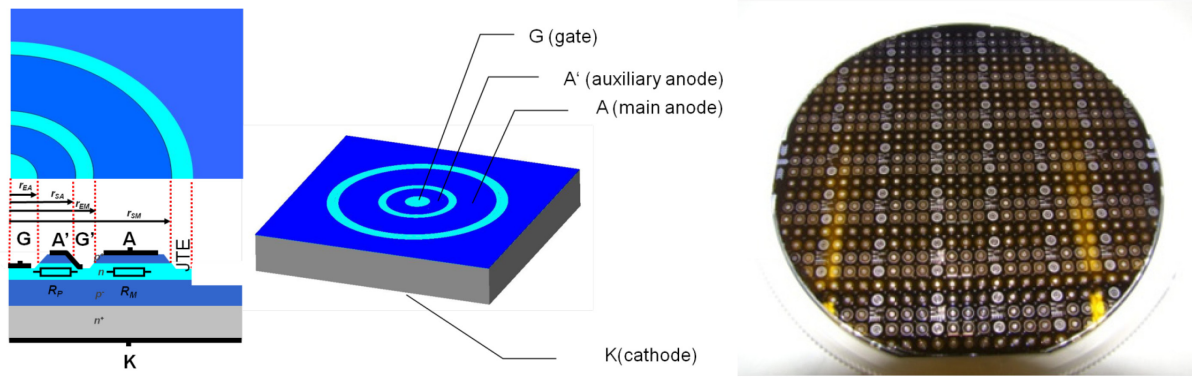


Fig. 1. Scheme of an amplifying gate thyristor (AGT) based on SiC (left); 100-mm SiC wafer featuring amplifying gate thyristors and test structures (right).

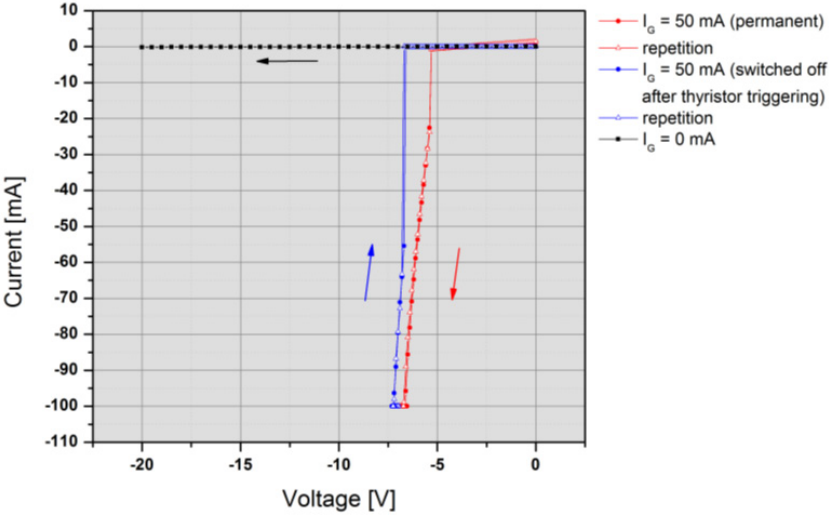


Fig. 2. Thyristor on-state characteristics (arrows indicate sweep direction) recorded via on-wafer probing.