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3D growth of silicon nanowires under pure hydrogen plasma at low temperature (250°C)

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The synthesis of silicon nanowires is carried out at 250°C under pure hydrogen plasma from monocrystalline silicon substrates or amorphous silicon thin film, using indium as a catalyst. Studies have been carried out in function of the duration of the hydrogen plasma. The results showed a growth of smooth surface nanowire arrays (diameter 100 nm, length 500 nm) from an indium thickness of 20 nm and a hydrogen plasma duration of 30 min. The growth of nanowires for longer hydrogen plasma durations has led to silicon nanowires with larger diameters and rougher surfaces, revealing the onset of secondary nanowire growth on these surfaces, probably due to the presence of indium residues. The results present a new procedure for the 3D Solid Liquid Solid (SLS) growth mode of silicon nanowires.

1. Introduction

The use of silicon nanowires (SiNWs) as functional building blocks for electronics has been demonstrated in several studies. Indeed, their nanometric size and their high surface-to-volume ratio make them very interesting as channel conduction in field effect transistors and for the detection of biological, chemical or gaseous species [1][2]. Another technological advantage is that many synthesis methods are CMOS compatible, providing the fabrication of the sensor and the integration of its detection electronics on the same platform [3].

Numerous methods of silicon nanowires synthesis have been reported. One of the most commonly used is the VLS (Vapor Liquid Solid) method firstly reported by Wagner and Ellis [4], which uses gold as catalyst and silane as precursor gas. In this case the growth temperature (compared to the eutectic temperature of the Au/Si alloy $T=360^{\circ}\text{C}$) is generally higher than 400°C . The nanowires grow in a 3D disordered configuration, with random growth direction at low temperature ($<600^{\circ}\text{C}$), gold impurities act as trapping centers of carriers, and their integration requires a transfer method for electronic applications in classical planar silicon technology. Otherwise, the use of such three dimensional (3D) nanowires configuration is of a great interest for the fabrication of biological or chemical sensors thanks to its capacity of a very large exchange surface as sensitive part for the detection of species [5]. Other elaboration methods have also been developed in a planar silicon technology. Some of them include high cost lithography tools (using ebeam lithography) for direct patterning of SiNWs on silicon on insulator (SOI) substrates [6]. In addition, an alternative method of in-plane Solid-Liquid-Solid (IPSL) growth of SiNWs was also proposed by L. Yu *et al* [7].

Currently, the development of flexible electronics and sensors on conformable substrates is of great interest. Thanks to the light weight and cost of the fabrication process and the easy handling of the substrates, such devices will offer great potential for high performance flexible and/or transparent electronics for flexible displays, touch screens, and also for conformable

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3 (mechanical and biological) sensors. In this area of applications, SiNWs can offer potentialities.
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5 However, the challenge is to develop highly reliable low-cost manufacturing technologies with
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7 a low environmental impact (including a low thermal budget and a low cost of production). In
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9 this case, two main technological keys should be overcome: development of a report technology
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11 of the SiNWs on flexible substrates, or direct growth of SiNWs with a maximum temperature
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13 of the process ($<300^{\circ}\text{C}$) compatible with low cost flexible substrates. In the second alternative,
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15 the direct SiNWs growth could be achieved thanks to advances in the development of growth
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17 and crystallization techniques at low temperatures. Indeed, silicon materials (re-)crystallisation
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19 processes using a metal catalyst [8][9] could be considered for SiNWs synthesis at low
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21 temperature. This last point would allow the fabrication of micro- and nano-devices based on
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23 SiNWs on any type of support, in particular cheap flexible (plastic) substrates that do not
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25 withstand high manufacturing temperatures ($>300^{\circ}\text{C}$). In the latter case, the control of such
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27 processes will contribute to an emerging field of applications in high-performance flexible
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29 visualization systems [10] [11] or sensors (artificial skin, NEMs...) [12] [13].
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36 In this study, we present the synthesis of silicon nanowires induced by metal catalysis using
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38 indium (In). This interest of this approach is a low eutectic temperature (157°C) of the Si/In
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40 alloy allowing the SiNWs synthesis at low temperature. In many cases, the indium catalyzed
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42 3D silicon nanowire growth follows the VLS growth method. In this growth procedure, the
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44 indium is firstly deposited, and because indium oxide acts as a growth inhibitor, the indium
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46 particles are submitted to a hydrogen plasma for desoxidation before the growth of nanowires.
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48 Then, in same reactor, the silane is introduced as the gas precursor to trigger the growth of
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50 silicon nanowires (in the range of 250°C to 600°C)[14][15][16][17]. The growth at low
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52 temperature ($300\text{-}500^{\circ}\text{C}$) of IPSLS silicon nanowires using indium as catalyst has also been
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54 reported by L. Yu's group [7]. In this method In nanoparticles catalyst are produced after
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3 reduction of a thin layer of Indium Tin oxide (ITO) under hydrogen plasma, and then a capping
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5 amorphous silicon layer is deposited and used as a precursor during the growth procedure.
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8 In this work, the growth of indium catalyzed silicon nanowires at 250°C under pure
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10 hydrogen plasma using a solid silicon based precursor is firstly reported. The precursor is either
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12 an amorphous silicon layer or a monocrystalline silicon substrate. The growth of SiNWs is
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14 discussed, and a SLS growth mode is proposed.
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22 **2. Experimental details**

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25 The study of nanowire synthesis was conducted on samples coated with a 50nm thick layer of
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27 amorphous silicon (a-Si) deposited at 230°C on a monocrystalline silicon (mono-Si) substrate
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29 in a plasma enhanced chemical vapor deposition (PECVD) reactor. Then, samples were
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31 submitted to thermal evaporation of indium ingot from resistively heated tungsten crucible to
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33 deposit a 20nm thick layer (In/a-Si/mono-Si sample). A sample with indium directly deposited
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35 on a <100> oriented monocrystalline silicon substrate was also studied as test sample (In/mono-
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37 Si sample). For each sample, indium was deposited with a constant rate at 5nm/min. After
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39 thermal evaporation of indium, In/a-Si/mono-Si and In/mono-Si samples were introduced into
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41 the PECVD reactor, and the growth of the nanowires was carried out under pure hydrogen
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43 plasma at 250°C, with a pressure of 0.8mbar and a radiofrequency power adjusted at 15W. The
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45 values of these parameters have been optimized for the growth of the nanowires (under pure
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47 hydrogen plasma).
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52 Thermal annealing of some samples was carried out at 250°C under nitrogen atmosphere after
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54 hydrogen plasma exposure in the same reactor. Experimental details are summed up in the table
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SEM (Scanning electron microscopy) and AFM (atomic force microscopy) observations were carried out to characterize indium deposition after thermal evaporation. The analysis of the morphology of indium nanoparticles was carried out by using Image J software. The average size of particles was calculated as the diameter of a circular particle having the same area. Silicon nanowires growth characterization was made by SEM and high resolution transmission electron microscopy (STEM) analysis. SEM analyses were carried out using a JEOL7600 FEG microscope, and a JEOL 2100 microscope for electron diffraction patterns and high resolution TEM (HRTEM) images. High-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) and energy-dispersive X-ray spectroscopy (EDS-STEM) were made using a Thermo Fisher Scientific S/TEM Themis Z G3 microscope. AFM analyses were carried out with a Multimode 8-HR microscope.

Table 1. Parameters of H₂ plasma treatment and annealing of samples.

	H ₂ plasma treatment	Annealing
Gas mixture	H ₂	N ₂
Temperature (°C)	250	250
Pressure (mbar)	0.8	0.8
RF power (W)	15	-

3. Results

First, the morphology of evaporated indium layers is analyzed, and secondly indium catalyzed silicon nanowires growth is studied in function of thermal annealing and H₂ plasma treatment.

3.1. Analysis of indium nanoparticles morphology

We firstly investigated the indium particles morphology after thermal evaporation. At this stage, the indium material did not undergo any thermal treatment. As shown in the SEM and AFM pictures of figure 1, indium particles show a flat polygonal shape and nanocrystalline structure, with a thickness around 20nm (fig. 1. c) corresponding to the thickness of the deposited indium layer. In addition, statistical study of the indium droplet size distribution was carried out. The histogram of the size distribution of indium nanocrystals reported in the figure 1. d follows a Gaussian fit, and shows that sizes are quasi symmetrically distributed from 20 to 110nm, and highlighting the preponderant nanocrystals sizes in the 50-80 nm range. These results are similar for both In/mono-Si and In/a-Si/mono-Si samples (not shown).

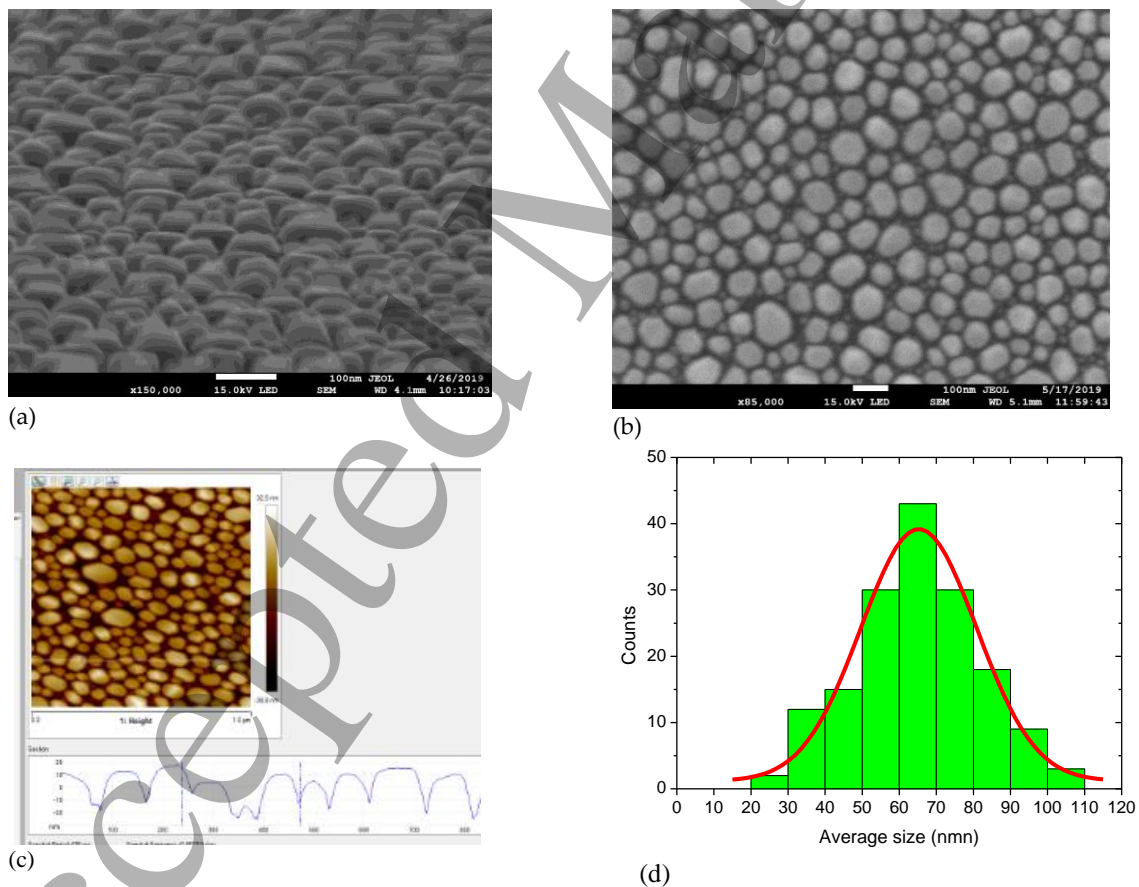


Figure 1: Lateral (a) and top (b) views of the SEM images, AFM profile (c), and distributions of nanoparticles indium sizes (d) of the 20nm thick indium deposited on 50nm a-Si/mono-Si.

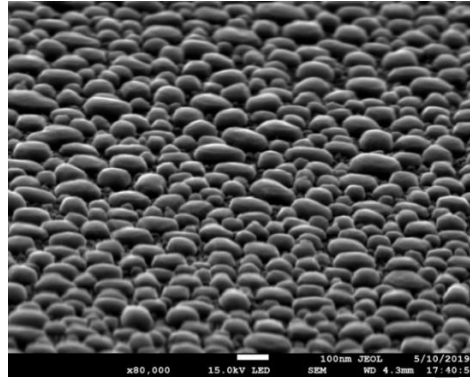
3. 2. Analysis of Silicon nanowires growth

For VLS and SLS processes, hydrogen plasma plays several roles in the growth of silicon nanowires catalyzed by indium. Its initial contribution is to remove the oxide layer on the surface of the catalyst, acting as an inhibitor for the growth of nanowires. Indeed in contrast to noble metals (such as gold), an oxide forms rapidly on the surface of the indium nanocrystals and cannot be thermally dissociated at low operating temperatures. A reactive treatment such as a hydrogen plasma is a procedure to reduce this oxide surface before growth of the nanowires. In addition, for VLS process, another benefit of hydrogen plasma is to increase the chemical potential of the silicon particles in the gas phase, thus increasing the super saturation of the silicon in the catalyst and the growth rate of the nanowires.

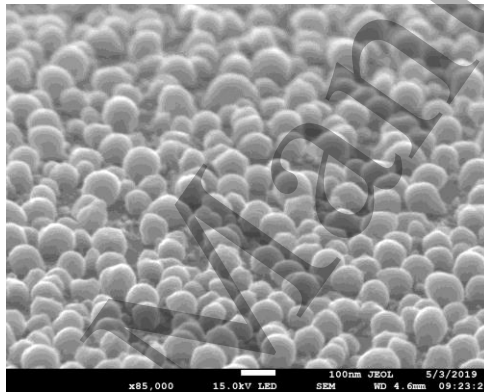
At first, a 30 minutes thermal annealing has been carried out on samples with a-Si layer covered by indium nanoparticles. SEM picture in the figure 2 (a) shows that there is no nanowire, and that after the thermal annealing the indium nanoparticles show slightly domed surfaces instead of flattened tops. For the sample that underwent one minute of plasma treatment followed by 30 minutes of annealing, the indium nanoparticles have a spherical shape indicating the start of growth of the nanowires. For sample under 1 minute of pure hydrogen plasma followed by 60 minutes of thermal annealing, nanowires with a length of 100nm appear. Therefore, these observations suggest that the short hydrogen plasma duration is related to the growth of silicon nanowires.

The effect of a longer hydrogen plasma treatment for nanowires growth was then investigated. The results are shown in the SEM pictures of the figure 3 for samples under pure hydrogen plasma for 10 and 30 minutes without thermal annealing. In this case of procedure, longer nanowires are obtained with a length of up to 400nm for 30 minutes under hydrogen plasma, with a conical shape, indicating a decrease of the indium size droplet due to a possible consumption of indium during growth. In comparison with results obtained under 1 min under

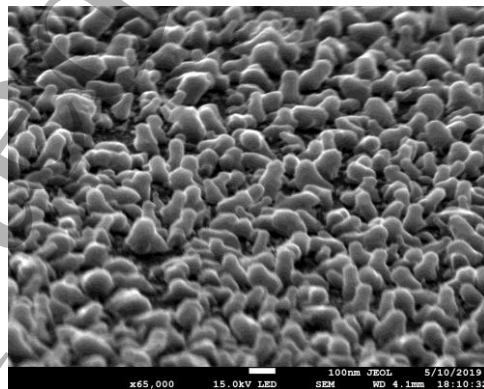
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3 hydrogen plasma exposure one can deduce that hydrogen plasma activates growth process of
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5 SiNWs.
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23 (a)

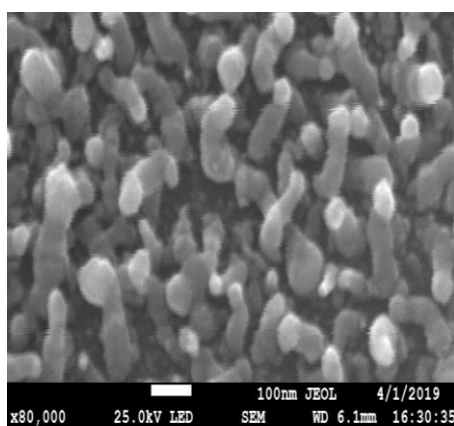


34 (b)

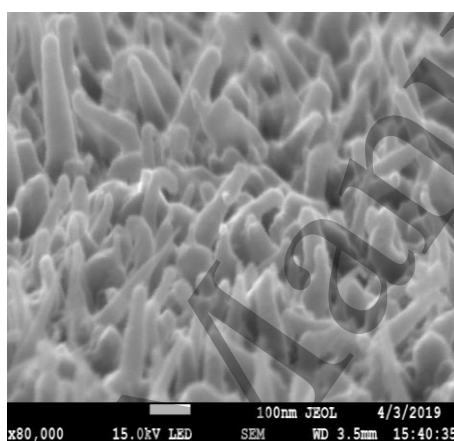


39 (c)

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54
55 Figure 2: SEM images of 20 nm In/50 nm a-Si/mono-Si samples tested under (a) no H₂
56 plasma + 30min annealing; (b) 1min H₂ plasma + 30min annealing; (c) 1min H₂ plasma +
57
58 60min annealing. Scale bars 100nm.
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(a)



(b)

Figure 3: SEM images of 20 nm In/50 nm a-Si/mono-Si samples tested under (a) 10 min, (b) 30 min H_2 plasma exposure

In order to investigate indium distribution, EDS spectrometry and TEM analysis were carried out along nanowires. First, EDS analysis was checked on three different parts of a sample (20 nm In/50 nm a-Si/mono-Si) submitted to a 30 min H_2 plasma exposure; at the base (dark part of the image), along (grey area) and at the top (bright part) of a nanowire. The results reported in the figure 4 show that indium is no present on the analyzed part at the base (estimated 0%), that its concentration is higher along the nanowire (8.1%), and finally that it is found in high concentration at the top of the nanowire (18.2%), the part where the indium drop is located.

These results are supported by HAADF and EDS STEM mapping reported in the figure 5. HAADF imaging method provides much more information at the atomic-scale and EDS-STEM performs chemical mapping at atomic-resolution. HAADF images of the figure 5 show that indium is homogeneously distributed along the nanowires, with a higher concentration at the top corresponding to the droplet. Moreover, TEM image observation of a single nanowire reported in the figure 6 shows that the surface is smooth, coated by 3-4nm thick homogeneous glossy layer on the surface of the nanowire and of the indium droplet, suggesting the presence of continuous native (indium or silicon) oxide that would have been formed during the preparation of the sample for analysis.

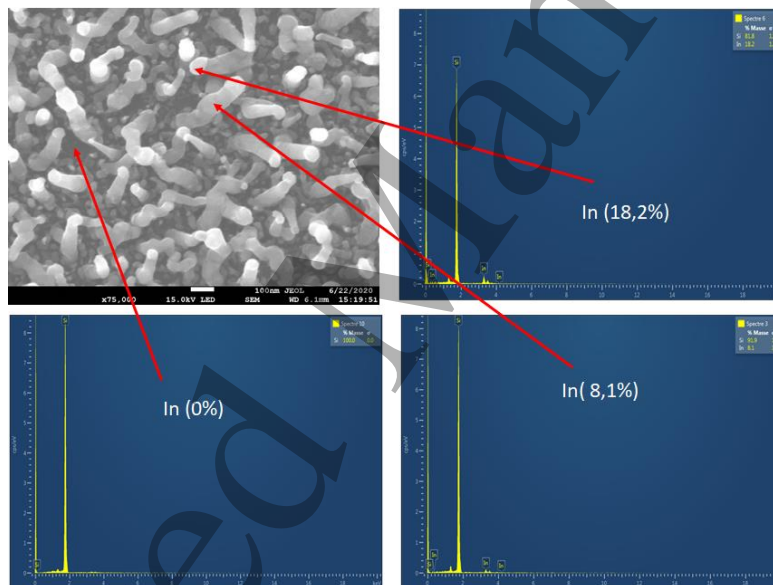


Figure 4: EDS analysis at the base (dark part of the image), along (grey area) and at the top (bright part) of a nanowire for 20 nm In/50 nm a-Si/mono-Si samples tested under 30 min H₂ plasma exposure.

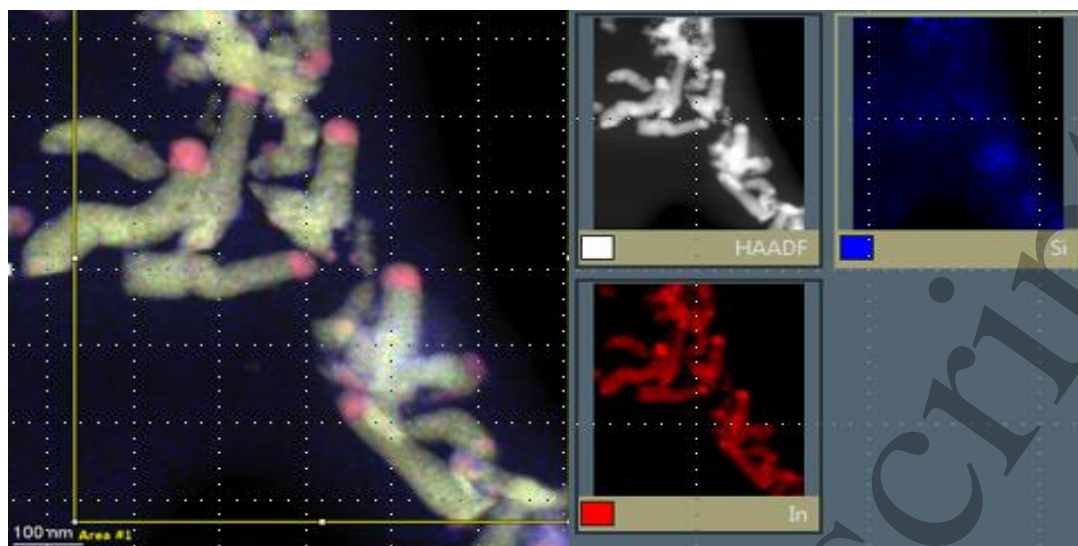


Figure 5: HAADF and EDS STEM images of nanowires for 20 nm In/50 nm a-Si/mono-Si samples tested under 30 min H₂ plasma exposure.

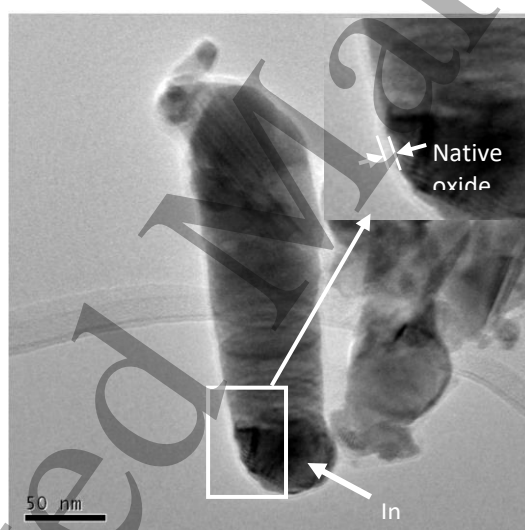
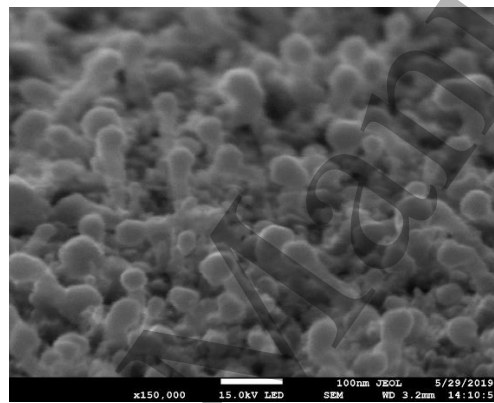


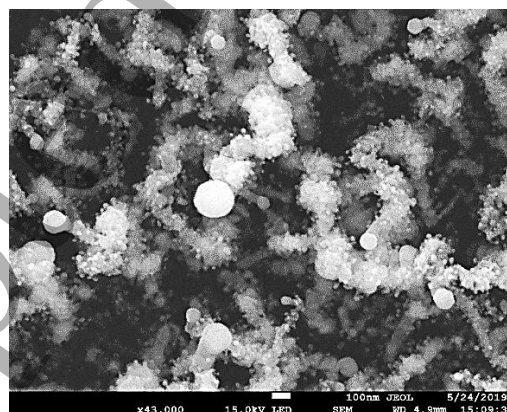
Figure 6: TEM image of single nanowire for 20 nm In/50 nm a-Si/mono-Si samples tested under 30 min H₂ plasma exposure.

The effect of long durations of hydrogen plasma (60 and 90 minutes) was also investigated (figure 7). After 60 minutes under H₂ plasma treatment, the nanowires are tilted with a quite rough surface, whereas after 90 minutes they are longer and show a bent shape and are decorated with bumps on their surface. These bumps are formed because of secondary growth on the

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3 surface of the nanowires due to the presence indium residues as revealed by high resolution
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5 TEM analysis. Indeed, HRTEM picture of nanowire grown under 60 minutes hydrogen plasma
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7 treatment reported in the figure 8 shows that the core of the nanowire has a crystalline structure
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9 with a $\langle 111 \rangle$ growth direction, and secondary crystalline clusters on surface with no
10
11 preferential growth direction. Moreover, twins are also observed on the tip of the nanowires
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13 below the indium droplet. Such crystalline structure in the core of the nanowires has also been
14
15 reported previously for indium catalyzed SiNWs grown by VLS method [18]. In addition, for
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17 a long duration (90 min) under hydrogen plasma, the bent shape of the nanowires shows that
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19 the $\langle 111 \rangle$ growth direction is not preferred anymore.
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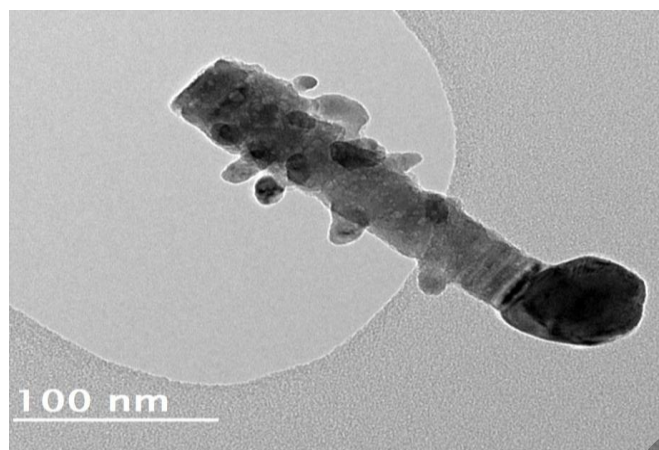
(a)



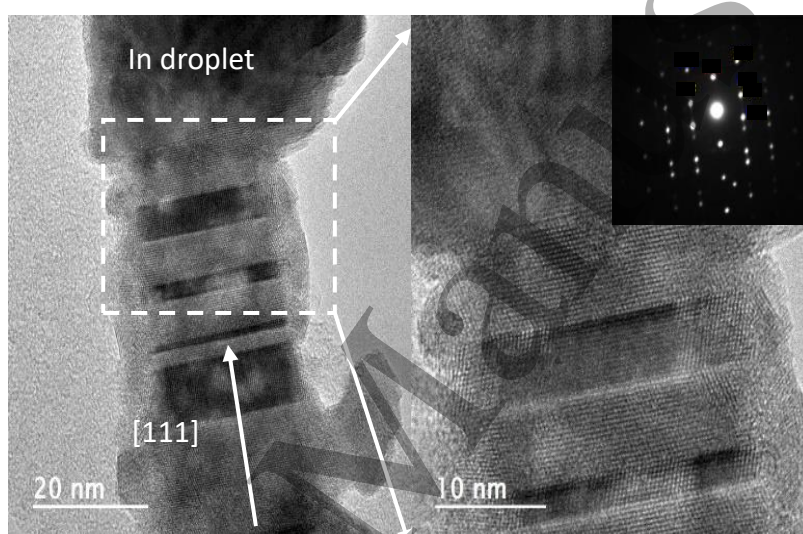
(b)

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Figure 7: SEM images of 20 nm In/50 nm a-Si/mono-Si samples tested under (a) 60 min H₂ plasma (b) 90 min H₂ plasma. Scale bars 100nm.



(a)

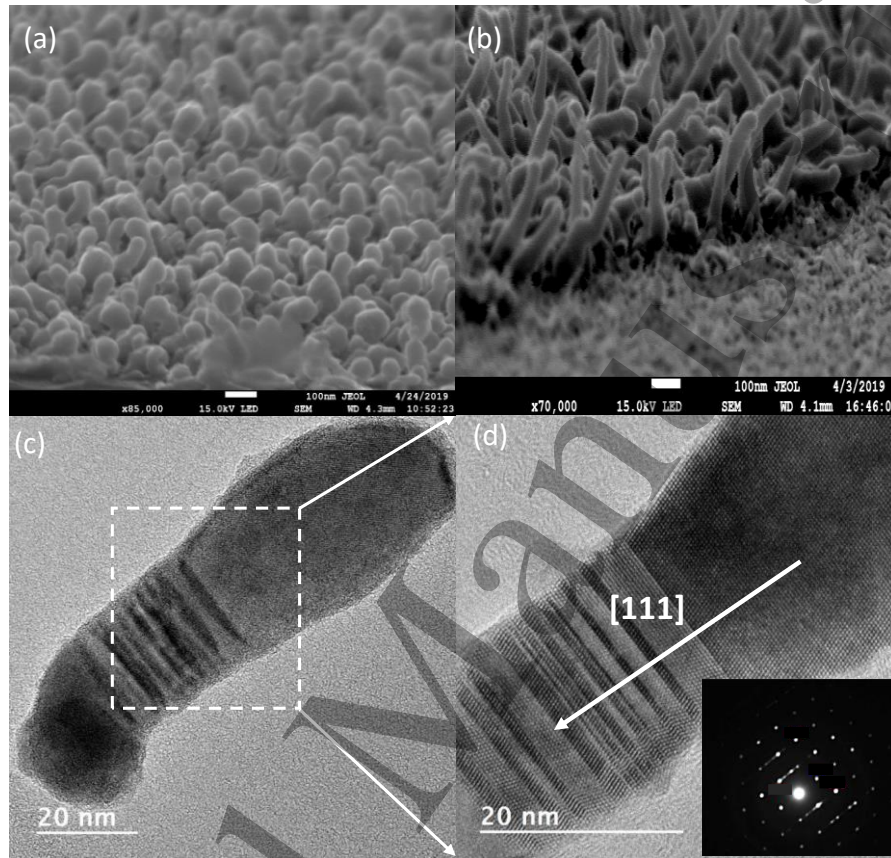


(b)

Figure 8: HRTEM images of a single nanowire for 20 nm In/50 nm a-Si/mono-Si samples tested under 60 min H_2 plasma exposure. (a) complete view , (b) partial views (Inset: electron diffraction pattern).

The direct growth of SiNWs on a $\langle 100 \rangle$ oriented monocrystalline silicon substrate under pure hydrogen plasma during 10 and 30 minutes was also demonstrated. The figure 9 shows that the characteristics of the SiNWs in terms of orientation, shape and sizes are similar to those grown on a-Si layer. Moreover, HRTEM analysis has also revealed the same crystalline structure with a $\langle 111 \rangle$ growth direction as for SiNWs grown on a-Si layer (fig.

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3 9 (c) and (d)), indicating that the crystallinity of the precursor silicon material does not
4 significantly influence the growth direction of SiNWs, and that epitaxial growth is not
5 promoted in our process of growth.
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41 Figure 9: SEM images of 20 nm In/mono-Si samples tested under (a) 10 min H₂ plasma; (b)
42 30 min H₂ plasma. HRTEM images of single nanowire after 10 min under H₂ plasma
43 treatment (c) and (d) (inset: electron diffraction pattern)
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50 4. Discussion

51 The mechanism responsible for the growth of nanowires in our process raises questions. The
52 presence of the indium droplet at the top of the nanowires suggests a VLS-like growth
53 mechanism. However, the assumption of a VLS mode is wrong since gaseous silicon-based
54 species are not introduced during the growth process. Indeed, some complementary tests were
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3 carried out to reject the hypothesis that silicon species could be found in the reactor acting as
4 gas precursors, due to a hypothetical sputtering effect under hydrogen plasma exposure. In this
5 way, tests were performed on samples coated with a hard mask made of opened windows, and
6 submitted to hydrogen plasma corresponding to the growth conditions of our nanowires. AFM
7 surface analysis of the protected and unprotected areas after removing of the hard mask of the
8 corresponding samples have shown that no etching effect of the precursor material (a-Si layer
9 or monocrystalline silicon substrate) was observed due to hydrogen plasma exposure.

10
11 Since the only silicon-based precursor element in the synthesis procedure is in solid form
12 (amorphous silicon thin film or monocrystalline silicon substrate), this makes to believe that
13 the growth process to be considered could be of the SLS type. However, this needs to be
14 clarified.

15
16 According to our knowledge, few results were reported on SLS mode growth of silicon
17 nanowires, and two modes have been described. First one, a 3D SLS mode growth of SiNWs
18 at high temperature (950°C) using nickel (Ni) as catalyst and monocrystalline silicon substrate
19 as solid precursor [19][20]. In this case, eutectic silicon-liquid(Ni) droplet forms at the stage of
20 procedure, and then silicon atoms diffuse through the substrate-liquid interface into the liquid
21 droplets, and the nanowires grow through the liquid-nanowire interface. This growth
22 mechanism is known as the root growth mode *ie* where catalyst remains at the bottom of the
23 nanowires [21]. The other case is for in-plane SLS growth of SiNWs at lower temperature
24 ranging from 300 to 500°C, using indium as catalyst and amorphous silicon thin film as solid
25 precursor. In this process, indium nanoparticles are embedded in the amorphous silicon layer.
26 Under the effect of thermal annealing, the indium nanoparticles move in the amorphous silicon
27 layer by diffusion of the silicon atoms of the amorphous silicon layer through the
28 liquid(In)/solid(Si) interface to form crystalline SiNWs [7].

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3 Due to the indium nanodroplet at the top of the nanowires, the 3D growth mechanism of our
4 nanowires does not correspond to the two SLS mechanisms described above. However, a
5 possible explanation could be an approach based on a mix of mechanisms combining the
6 classical 3D SLS growth mode (root mode) and the diffusion of Si adatoms on the surface of
7 the nanowires [22]. In the early stages of growth, indium nanocrystals are transformed into
8 spherical nanodroplets under the effect of temperature and hydrogen plasma. The growth of the
9 nanowires starts following the classical SLS mode (*ie* diffusion of the silicon atoms of the solid
10 precursor into the liquid indium). In addition the growth mechanism may involve diffusion of
11 silicon adatoms from solid precursor to the top along the nanowires surface thanks to a sidewall
12 wetting indium layer (see illustration in figure 10). This effect would contribute to the vertical
13 growth, and in lower contribution to the lateral growth of the nanowire. For long periods of
14 growth, a dewetting of the sidewall indium layer would lead to the formation of nanodroplets
15 that could induce secondary growth of nanowires at the surface, as observed in the figures 7 (b)
16 and 8. It should be noted that the process of diffusion of silicon adatoms along the surface of
17 the nanowires is similar to another process for the growth of ZnO nanoneedles on zinc foils
18 under thermal annealing ($T > 420^{\circ}\text{C}$), for which zinc in the liquid phase plays a catalytic role
19 in mediating the mass transport of from the root to the growth front of a nanowire and thus
20 contributes to the growth [23]. In our model hydrogen plasma activates the growth of silicon
21 nanowires. One possible explanation could be that the hydrogen plasma increases the chemical
22 potential of the silicon atoms of the solid precursor which could enhance their diffusion through
23 the substrate-liquid interface into the liquid Indium droplets. However, this phenomenon is not
24 well understood and should be clarified in further study.
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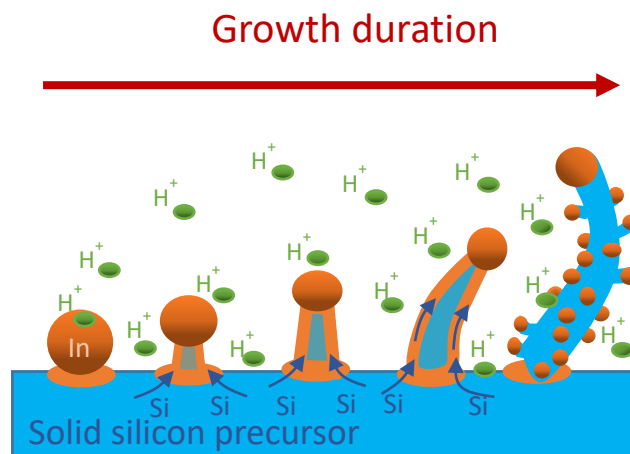


Figure 10: Schematic illustration of the SLS growth model under pure hydrogen plasma of SiNWs at different stages of growth

5. Conclusion

We report on new synthesis process of 3D silicon nanowires at low temperature (250°C) using indium as catalyst and solid silicon material as precursor. Indium is first thermally evaporated and indium nanocrystals with flat polygonal shape are obtained. Nanowires are grown into a PECVD reactor under a pure hydrogen plasma, and amorphous silicon layer or monocrystalline silicon act as precursors. A mechanism for the growth of crystalline silicon nanowires is proposed, based on SLS mode combined with diffusion of adatoms of silicon in a sidewall wetting indium layer covering the nanowires.

The growth temperature in this method is lower than mainly works reported either on the VLS or SLS methods, making this mode growth compatible for new applications, in particular for elaboration of silicon nanowires based devices on low-temperature flexible substrates.

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