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# XbarGen: a Memristor Based Boolean Logic Synthesis tool

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**Abstract**—The shrinking process of CMOS technology is reaching its physical limits, thus impacting on several aspects, such as *performances, power consumption and many others*. Alternative solutions are under investigation in order to overcome CMOS limitations. Among them, the memristor is one of the promising technologies. Several works have been proposed so far, describing how to implement boolean logic functions employing memristors in a crossbar architecture. In this paper, we propose a tool able to automatically map any boolean function to a memristor based crossbar implementation. The proposed tool helps to perform a design space exploration to identify the best implementation w.r.t. performances and area overhead.

**Index terms**—Memristor crossbar, Design Space Exploration, Boolean Functions. Circuit Synthesis

## I. INTRODUCTION

Today’s computing devices are based on the CMOS technology, that is the subject of the famous Moore’s Law [1] predicting that the number of transistors in an integrated circuit will be doubled every two years. Despite the advantages of the technology shrinking, we are facing the physical limits of CMOS. Among the multiple challenges arising from technology nodes lower than 20 nm, we can highlight the high leakage current (i.e., high static power consumption), reduced performance gain, reduced reliability, complex manufacturing process leading to low yield and complex testing process, and extremely costly masks [2], [3], [4], [5].

Additionally, the expected never-ending increasing of performances is indeed no longer true. Looking in more detail, the classical computer architectures, either *von Neumann* or *Harvard*, divide the computational element (i.e., CPU) from the storage element (i.e., memory). Therefore, data have to be transferred inside the computational element in order to be processed and then transferred back to be stored. The main problem of this paradigm is the bottleneck due to the data transfer time limited by the bandwidth. For example, transferring one TeraByte at the rate of 1Gbit/second requires more than two hours.

Many new technologies are under investigation, among them the *memristor* is a promising one [9]. The memristor

is a non-volatile device able to act as both storage and information processing unit that presents many advantages: CMOS process compatibility, lower cost, zero standby power, nanosecond switching speed, great scalability, high density and non-volatile capability [10], [11]. Thanks to its nature (i.e., computational as well as storage element), the memristor is exploited in different kind of applications, such as neuro-morphic systems [12], non-volatile memories [13], computing architecture for data-intensive applications [6].

A fundamental component of any kind of computing architecture is the implementation of boolean logic functions. In [14], the authors proposed a methodology for the synthesis of boolean logic function on a memristor crossbar. Their work showed that is possible to implement any kind of boolean function on a memristor crossbar. However, the experimental results have been carried out on a couple of small circuits only due to the lack of an automated synthesis tool. In this paper, we aim to extend the work of [14] by presenting a tool able to automatically map any boolean function to a memristor based crossbar implementation. Moreover, we investigate the impact of different synthesis optimization parameters on the memristor crossbar to evaluate area and performances.

The remainder of the paper is structured as following. Section II presents the state of the art and provides the required background on the memristor based computation. Section III details the proposed memristor and crossbar model as well as the synthesis methodology, while the Section IV gives the experimental results. Finally, the Section V draws the conclusions.

## II. BACKGROUND AND STATE OF THE ART

In this section we provide the basics about the memristor modeling, as well as the way how the memristor can be exploited to implement a given boolean function.

### A. Memristor model

A memristor is a non-linear electrical component whose electrical resistance is not constant but depends on the history of the charge flowed through the device itself. Since we intend to implement a digital circuit, we refer to the memristor Voltage-Current relation depicted in Figure 1, detailed in [8],

as the best solution for modeling the memristor's behavior (i.e., thanks to the ideal response to a pulse-wave). Thus, as the Figure 1 shows, the voltage applied to the memristor's terminals does not change its resistance until it crosses a threshold. In the adopted ideal model, the upper and the lower thresholds have the same absolute value.

We resort to the Snider Boolean Logic (SBL) [8] convention whereby a lower resistance (steeper curve denoted as  $R_{ON}$ ) represents a logic '0' while a higher resistance (lower slope curve denoted as  $R_{OFF}$ ) represents a logic '1'.

Two basic operations can be performed, defined as SET and RESET. The first one allows to program the memristor to  $R_{ON}$  and thus at logic '0', while the second one programs the memristor to  $R_{OFF}$  that corresponds to logic '1'. The Figure 1 depicts SET and RESET operations as described by Xie et al. in [14]

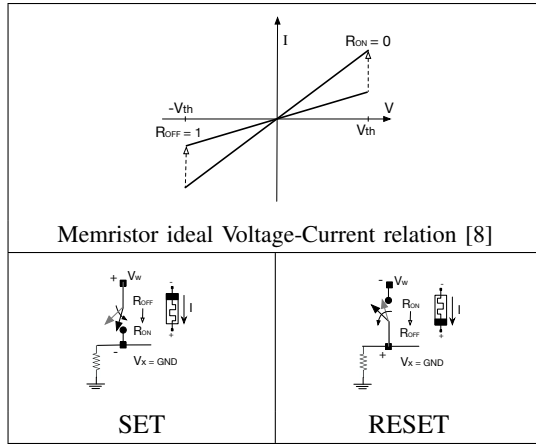


Figure 1. Set and Reset operations [14]

### B. Fast Boolean Logic Circuits

Snider proposed in [8] a design methodology for memristor crossbar that aimed to implement boolean functions. This design was then improved by Xie et al. in [14]. Let us briefly recall their proposition referring to it as Fast Boolean Logic Circuit (*FBLC*). First, the logic circuit requires that the Boolean function is expressed in the SOP format:

$$f = M_1 + M_2 + \dots + M_n = \overline{\overline{M_1 \cdot M_2 \cdot \dots \cdot M_n}}_{\text{AND}} \text{ NOT}$$

Then, as Figure 2-a shows, FBLC is divided in blocks, useful to accomplish FSM's steps (fig 2-b) which are:

INA: **initialize all** the memristors to  $R_{OFF}$ ;  
 RI: **the input block receives the inputs**;  
 CFM **configure all minterms simultaneously**, in parallel;  
 EVM: **evaluate all minterms simultaneously** (NAND);  
 EVR: **evaluate results**:  $f$  is calculated (AND);  
 INR: **invert results**:  $\bar{f}$  need to be inverted to achieve  $f$   
 SO: **send outputs**: the result captured in OL is sent out.

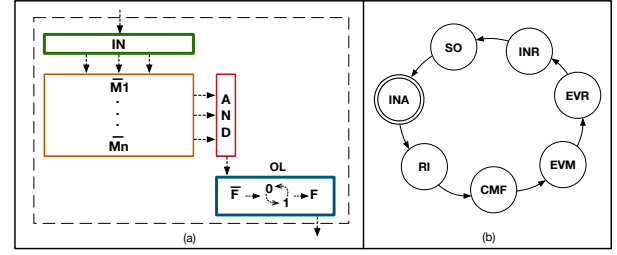


Figure 2. Fast Boolean Logic Circuit

Below, the description of the blocks:

- **input block**, where inputs are stored during the RI step;
- **minterms block**, where minterms are configured during CFM and evaluated during EVM;
- **AND block**, where results of EVM are stored and AND operation is performed during EVR;
- **output block**, where results of EVR are stored and inversion operation is performed during INR;

For the purpose of realizing each step of the FSM, the authors proposed some *primitive operations* that we summarize in Figure 3.

Each of these operations can be performed using as many input and output memristors as desired.

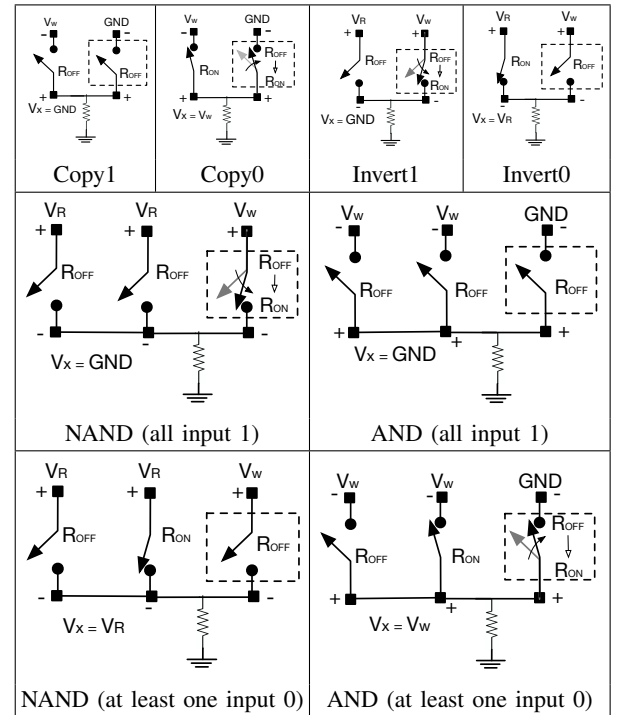


Figure 3. FBLC primitive operations

By driving the crossbar's nano-wires with the right voltages during each step, it is possible to calculate a boolean function in a constant number of steps. We report below in Figure 4 an example of crossbar for a simple 2 inputs / 1 output function, built following the FBLC approach.

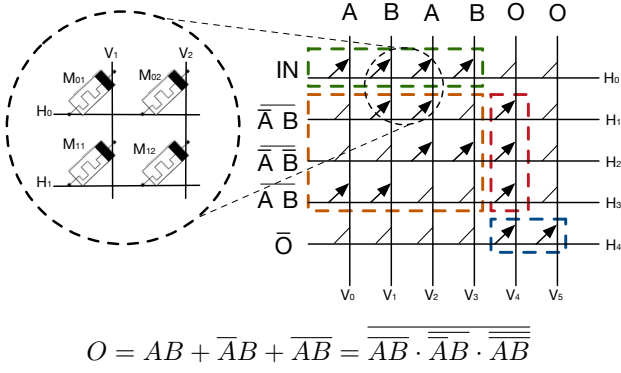


Figure 4. FBLC example

### III. TOWARDS AUTOMATIC CROSSBAR SYNTHESIS

Due to the lack of an automated process of translation from a given boolean function to a memristor based crossbar architecture, deeply investigating about memristor based crossbar circuits turns out to be really hard to accomplish. Therefore, in order to overcome these problems, we developed XbarGen.

XbarGen is a command line tool written in C++ which, starting from a boolean function described in the Synopsys equation format - EQN - (fig 5), executes the mapping to a memristor based crossbar architecture and produces a schematic view of the crossbar(s).

```

INORDER = a b c;
OUTORDER = o1;
n5 = !b * c;      INORDER = a b c;
n6 = a * !n5;     OUTORDER = o1;
n7 = b * !c;      o1 = !a*b*c +
n8 = !n5 * !n7;   !a*!b*c + a*!c + a*b;
n9 = !a * !n8;
o1 = n6 + n9;

```

Figure 5. Synopsys equation format (EQN)

First, the tool operates an analysis of the given function. As the figure 5 shows, it is possible either that a function's output depends directly on its inputs either that it depends on "intermediate values", which indeed depends on inputs.

Thus, we will call level a set of inputs and outputs such that:

- inputs are independent from one another
- each output depends only on inputs

In this way we are able to describe a boolean function as a set of levels each one dependent from one another (figure 6)

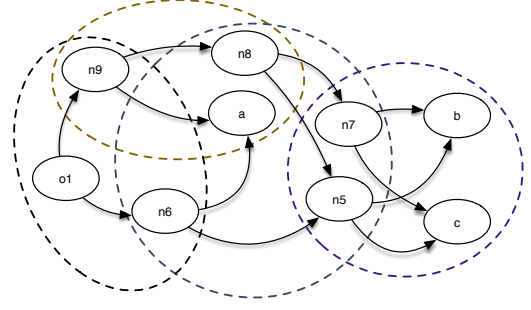


Figure 6. Function's levels

Second, the tool performs a mapping to one or more crossbars depending on how many levels it finds. Mapping to a crossbar means that inputs, outputs and related minterms of each level are translated into a FBLC, as explained in [14] and briefly reminded above. It is worth noting that, when more crossbars are produced, they must be connected together in series, as proposed by Snider in [8] and depicted in figure 7. Consequently, the latency of the circuit grows proportionally to the number of serially connected crossbars.

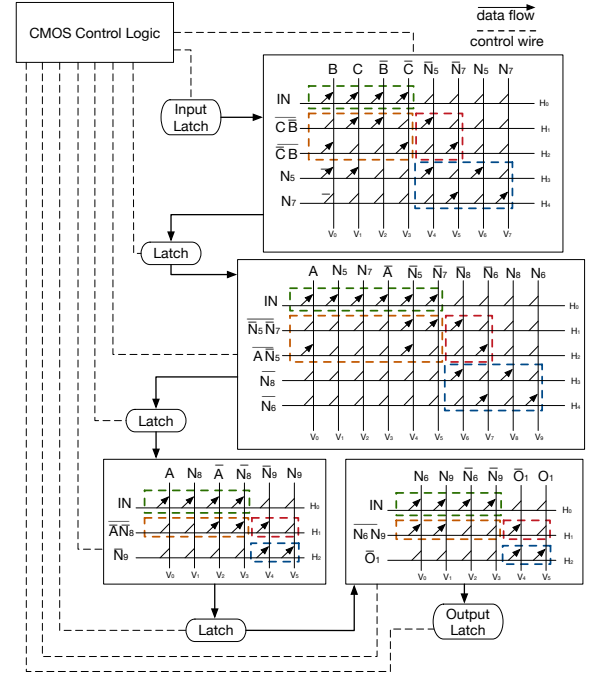


Figure 7. Snider Boolean Logic Circuit

### IV. EXPERIMENTS AND RESULTS

This section provides the experimental results achieved by the proposed synthesis tool and the adopted crossbar model. We also compare the proposed approach with the state of the art.



Symbol	Description	Expressed as
$p_{ij}$	Whether the $i$ -th minterm is in the $j$ -th level (boolean)	Given
$N_{in}(l_j)$	Num. of input for the $j$ -th level	Given
$N_{out}(l_j)$	Num. of output for the $j$ -th level	Given
$N_{occ}(m_i, l_j)$	Num. of occurrences of the $i$ -th minterm in the $j$ -th level	Given
$N_{lit}(m_i)$	Num. of literals of the $i$ -th minterm	Given
$N_{mem}$	No. of memristors in the circuit	$\sum_j \left[ 2 * N_{in}(l_j) + \sum_i (N_{occ}(m_i, l_j)) + \sum_i (N_{lit}(m_i) * p_{ij}) + 2 * N_{out}(l_j) \right]$
$N_{min}$	No. of minterms in the circuit	Given
A	Total area	$\sum_j \left\{ \left[ 2 * N_{in}(l_j) + 2 * N_{out}(l_j) \right] * \left[ 1 + \sum_i (p_{ij}) + N_{out}(l_j) \right] \right\}$
$t_M$	Memristor switching time	Given
$N_{Steps}$	Num. of steps of a Crossbar computation	Given
$T_C$	“Latency” of a Crossbar	$t_M * N_{Steps}$
$N_C$	Num. of Crossbar in the circuit	Given
C	Needed Cycles to complete computation	$T_C * N_C$
$T_{XbG}$	Time (in milliseconds) needed by XbarGen to execute	Experimental
$T_{sim}$	Time (in milliseconds) for simulate VHDL design (50ns long)	Experimental
<b>Chakraborti et al. [7]</b>		
$M_s$	No. of memristors (serial)	
$OP_s$	No. of memristor micro-operations (serial)	
$M_p$	No. of memristors (parallel)	
$OP_p$	No. of memristor micro-operations (parallel)	

Table II  
LEGEND

In addition, with regard to feasibility of translation and simulation of memristor crossbar behavioral circuits, we collected the time that XbarGen needs to translate a boolean function and produce the crossbar schematic view (table I). XbarGen experiments were run on a dual-core i7 MacBook Pro with 2.8GHz clock, 4 GB RAM and running OSX v10.11.4.

### C. Comparison

Chakraborti et al. in [7] proposed an architecture based on material implication operation implemented using memristors. In brief, they came up with a realization of 2-to-1 multiplexer using memristors, and a synthesis methodology that represents a given Boolean function as a Reduced Ordered Binary Decision Diagram (ROBDD) and maps it to memristor implementation. They carried out some benchmarks too (table I), reporting interesting results: comparing experiments that exploit parallelism and those that do not, the inverse ratio time-area is respected; from our side, instead, it is not true. On the other hand, execution time of the architecture in [7] depends on the function under consideration; execution time of Snider architecture could be independent from the function, if it is translated to a single crossbar. This could mean that one would prefer an architecture such as proposed in [7] in case of area constraints and an architecture such as Snider proposed in [8] in case of time constraints.

### V. CONCLUSION

The memristor is one of the most promising technologies which is able to deal with the CMOS limitations. In particular, since the memristor is inherently able to behave also as a non-volatile device, it allows to overcome the bottleneck of the data transfer to the computational unit and back to storage elements. The research community is facing with the synthesis of boolean functions by exploiting memristor-based crossbars

and, in this paper, we advanced the state-of-the-art with a comparison with the state-of-the-art of performances w.r.t. several benchmarks. Indeed, we developed XbarGen, a tool which is able to process boolean equations for the mapping over memristor crossbars.

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