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# Improving the ability of bulk built-in current sensors to detect Single Event Effects by using triple-well CMOS

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- I. Introduction
  - SET mechanism, BBICS principle
- II. Zhang et al. BBICS architecture

Experimental results & unexpected weakness

III. Analysis

Experimental measurements

Improving BBICS efficiency: use of triple-well CMOS

IV. Validation

A new BBICS design

Simulation results

- □ Integrated circuits in radioactive environment
- Suffer from various types of Single Event Effects (SEE)
  - Single Event Transient (SET),
  - Single Event Upset (SEU),
  - Single Event Latchup (destructive)
  - Single Event Gate Rupture, etc.
- Bulk Built-In Current Sensor (BBICS)
  - Design to monitor the advent of SETs and SEUs
- Not to prevent their effects

## □ SET mechanism – The inverter case



Sensitive area: reverse biased PN junction (drain of the off transistor)

## □ SET mechanism – The inverter case



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## □ SET mechanism – The inverter case



SEE current flows through substrate and its biasing TAPs



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#### BBICS: monitor SEE current through node NMOS\_bulk



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### II. Zhang et al. BBICS architecture

- □ Zhang et al. BBICS architecture [zhang2010]
  - Published in 2010, experimental validation reported in 2013
    NMOS monitoring less effective than expected?!



### II. Zhang et al. BBICS architecture

• NMOS-BVIS : NMOS monitoring / PMOS-BVIS : PMOS monitoring



### II. Zhang et al. BBICS architecture

Experimental testing of NMOS-/PMOS-BVIS [zhang2013]

Test chip CMOS bulk 90 nm:

- many instances of NMOS-/PMOS-BVIS,
- multiplier as a test element.



Experimental testing of NMOS-/PMOS-BVIS [zhang2013]
 Ionizing particle effect emulation with a laser source:

-  $\lambda$  = 800 nm, laser spot Ø = 1.6 µm, pulse duration = 1 ps

# of biasing contact (NTAPs or PTAPs)	10	40	80	160
Multiplier SEE sensitivity threshold	82 p J	82 p J	82 p J	82 p J
PMOS-BVIS detection threshold	15 p J	42 pJ	75pJ	n.d.
NMOS-BVIS detection threshold	110 pJ	149pJ	n.d.	n.d.

n.d. = not detected

- $\implies$  PMOS monitoring: efficient up to 80 biasing contacts
- NMOS monitoring: inefficient SEE sensitivity always < BBICS detection threshold</p>

## Experimental measurements

### Understanding SEE currents in NMOS/PMOS

Test chip: CMOS 90 nm, bulk and triple-well, single NMOS and PMOS

Experiment settings: measure of laser-induced currents

at  $\lambda = 1064$  nm, laser spot  $\emptyset = 5 \mu m$ , pulse duration = 20  $\mu s$ , 1.25 W (settings outside ionizing particle emulation)



#### EMSE laser facility

## Experimental measurements

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### III. Analysis



#### Analysis:

- $\implies$  Bulk current an order of magnitude above drain current
- $\implies$  Promote detection over SEE generation



# □ Improving BBICS efficiency

- Use of triple-well CMOS
  - > NMOS in Pwell to mimic PMOS properties



# □ Improving BBICS efficiency

- Use of triple-well CMOS
  - > NMOS in Pwell to mimic PMOS properties

#### NMOS current:



Pwell-DNwell junction unbiased



- Bulk current an order of magnitude above drain current
  - $\Rightarrow$  Promote detection over SEE generation

# □ Single BBICS architecture

- Design of a test chip: CMOS 65-nm (bulk and triple-well)
- New BBICS architecture: the *single* BBICS (design to bring together NMOS and PMOS monitoring ability)



- Validation on the basis of simulation
- Post-layout electrical simulation (parasitic R and C extracted)
- Current source to model SEE currents:

current pulse, double exponent, 50 ps rise time, 150 ps fall time, µA range

Investigation of SEE and BBICS detection thresholds



- Validation on the basis of simulation
- 1. CMOS bulk (NMOS on Psub, ie. no triple-well)

# of inverters	40	80	120	200
Threshold of NMOS SET	102µA	104 µA	104 µA	104 µA
Single BBICS detection threshold	56 µ A	82µA	107 µA	155 µA

Th	reshold of PMOS SET	126 µA	131µA	134 µA	137 µA
	corresp. PMOS bulk current	>1.2mA	>1.3mA	>1.3mA	>1.3mA
Sir	ngle BBICS detection threshold	45µA	67 µA	107 µA	134 µA

 $\implies$  NMOS monitoring weakness confirmed on the basis of simulation

- Validation on the basis of simulation
- 2. <u>Triple-well CMOS</u> (NMOS in Pwell)

# of inverters	40	80	120	200
Threshold of NMOS SET	94 µA	95µA	98µA	100 µA
Corresp. NMOS bulk current	>0.9mA	>0.9mA	>0.9mA	>1 mA
Single BBICS detection threshold	75µA	112µA	147 µA	212µA

Th	reshold of PMOS SET	118µA	125 µA	127 µA	130 µA
	corresp. PMOS bulk current	>1.1mA	>1.2mA	>1.2mA	>1.3mA
Sir	ngle BBICS detection threshold	84 µA	125 µA	163µA	237 µA

⇒ Triple-well restore NMOS monitoring ability of BBICS

- □ Review of BBICS principle
- Exp. revealed a weakness in monitoring NMOS
- □ Analysis and proposal of a solution
- Use of triple-well CMOS (NMOS in Pwells)
- Validation on simulation basis (new BBICS architecture)
- Perspectives
- Experiments on a CMOS 65-nm test chip



# Thank you for your attention

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[zhang2010], Zhang et al., CCECE 2010 A new bulk built-in current sensing circuit for single-event transient detection

[zhang2013], Zhang et al., Journal of electronic testing 2013 A Bulk Built-In Voltage Sensor to Detect Physical Location of Single-Event Transients