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Abstract:

Silicon (Si) used as negative electrode in a Li-ion battery (LIB) is highly attractive for its high energy density, safe cycling, and nontoxicity. However its alloying mechanism with Li induces material pulverization, which leads to a rapid capacity fade. In this work, annealing post treatment was used in order to tune the morphological properties of porous silicon. Playing on annealing temperature, the morphological modification induces electrochemical behavior changes in LIB. The porosification is an interesting way to accommodate the volume expansion occurring during the alloying process. Increase of the annealing temperature leads to porous Si pores and walls reorganization, which has a positive impact on battery performance likely due to a higher wettability of the Si electrode with electrolyte. 700°C appeared to be the optimized annealing temperature.

I. INTRODUCTION

Silicon (Si) is one of the most attractive candidate material for next-generation Li-ion battery (LiB) anodes. Indeed, Si anode works at low potential (370 mV vs Li^{+}/Li)[1] leading to a high energy density and safe cycling conditions. It could theoretically lead to ten time higher gravimetric capacity (3579 mAh g^{-1})[2] than currently commercialized graphite anodes. Furthermore, being the second most abundant element on earth it is inexpensive and it is nontoxic. However, despite its remarkable advantages, silicon shows some limiting intrinsic properties. The Li/Si alloying reaction induces a large volume expansion (310 %) causing material pulverization which leads to active material electrical isolation. [3] This volume change is the first cause responsible for rapid capacity fade of silicon based negative electrodes. The use of nanostructured silicon is one of the key of success for Si-based negative electrode in Li-ion battery application. Indeed, reducing the silicon dimensionality limits the structural stress during the lithiation/delithiation mechanism responsible for its pulverization. Huang J. et al. have demonstrated that no cracks occur with a silicon particle size limit below 150 nm [1]. Moreover downsizing active materials influences Li ion diffusion kinetics and the stability of SEI layer [2,[4]. That is the reason why many efforts are presently still provided by proposing new rapid and cost-effective methods to produce nanostructured silicon materials. Many different types of structures have been produced and tested in Li-ion batteries applications: from 0D (Si nanospheres/nanoparticles), 1D (nanowires or nanotubes), 2D (Si thin films) to 3D nanostructured materials as porous silicon [5]. It is also well established that Si-C composites are efficient to stabilize the electrode electrochemical behavior. In fact limiting the Si content in the composite allows decreasing the volume expansion drawbacks [6]. On the other hand controlling the interactions binder-Si [7],[8],[9] or

improving the electron transfer by adding conducting coating at Si surface have shown to be interesting ways.[10][11] The choice of the electrolyte plays also a key role in capacity retention especially since most of them are electrochemically unstable in the working potential window and lead to a solid electrolyte interface (SEI) continually generated on the Si electrode surface. In order to form stable SEI layer, chemicals additives like vinylene carbonate (VC) and fluoro-ethylene carbonate (FEC) can be added in the electrolyte.[12] Regarding cycling conditions, it is recognized that limiting the low potential window to prevent the $Li_{15}Si_4$ crystalline phase formation may improve the cyclability.

Despite these numerous limitations, good electrochemical performance can be observed in literature for porous Si structures thanks to the free spaces in the material able to buffer the volume expansion. Highly porous Si sponge structure (80% of porosity, pore size around 50 nm, wall thickness of 10 nm) with high surface area of ~495 $m^2.g^{-1}$, showed interesting performance with a capacity of 750 mAh g^{-1} and more than 80% of its capacity could be retained after over 1000 cycles [13]. Even higher capacity has been reached (2500 mAh g^{-1} at a current rate of 0.5 C for 100 cycles) with 3D porous silicon particles [14], presenting larger interconnected pores (200 nm) and wall thickness (40 nm). Similarly, Ge et al. reported porous doped Si nanowires synthesized from P-doped Si wafer [15]. Such nanowires exhibit smaller pore diameter and wall thickness (8 nm) and lead to extremely stable cycling behavior over 2000 cycles. These studies verified that managing the porosity can improve the capacity retention by providing a free volume for the Si expansion and maintaining the structural integrity of the Si anodes. To the best of our knowledge, no systematic study showing the link between silicon morphological properties and electrode performance has been reported. For example, for mesoporous silicon sponge particles [16], the optimal

overall porosity was proposed around 70% to limit volume expansion under 75%. On the other hand Si with walls of 10 nm and pores of 10 nm have shown a capacity of 570 mAh g^{-1} and 87% of capacity retention over 1000 cycles. At last porous Si microparticles [17] with an average pore size ranged between 5–16 nm and a porosity around 50% have shown a better behavior for 10-20 µm sized particles. Needless to say, a comparative analysis of Si based electrodes is tricky due to the huge variety of possible cycling conditions which have a considerable impact on performance.

Porous Si can be prepared following two classes of methods including top-down or bottom up. The top-down approach provides the pore formation from a bulk material while the bottom-up approach generally uses a porous template that will be filled and then dissolved. Generally, the top-down methods leads to material dissolution by hydrofluoric acid (HF) attack. The morphological properties of the porous material, as the pore shape and size, the walls shape and thickness or the overall porosity, can be tuned by controlling the applied current density and HF concentration [18]. The electrochemical performance of the silicon electrode varies significantly with the morphology, and the latter is highly dependent on the nature (p or n) and concentration of the dopant within the Si wafer [19], [20]. It is also possible to start the synthesis from porous silica and modify it by magnesiothermic reaction [21,22], aluminothermic reaction [23] or from an alloy as Si-Al dissolving specifically Al [24], and also from silicon particles by electroless etching [25,26]. Those technics allow complex architecture but a lower control of the porous silicon morphology determined by the mother material, the global material porosity is more often discussed than the pores shape and dimensions. [18]

In this work, our approach consists in using electrochemical etching of silicon wafers as the easiest and most reproducible method to obtain highly porous silicon films and

to tune their morphological properties by applying a rapid thermal annealing post treatment. This process allows a wide variety of pore morphologies and textures without modifying the dopant level. The main goal is to study the morphological properties impact on silicon-based anode performance in Li-ion batteries.

II. EXPERIMENTAL

A. Porous silicon preparation

a. Electrochemical etching process

Commercially available, boron doped p-type crystalline Si wafers (0.001 – 0.002 Ω cm) were porosified in a single bath electrochemical etching Teflon cell. The Si wafer ((100) oriented) was placed between the Cu working electrode and Pt counter-electrode. The porous Si film was obtained by applying a pulsed current in a HF (49 %): ethanol (1:1, v:v) electrolyte. Anodic and cathodic current density were respectively -150 mA cm^{-2} and 0 mA cm^{-2} during a same pulse time of 1 sec. The total etching time was 100 min, which led to a 200 µm-thick porous silicon. Then, the separation of the porous Si layer from its mother substrate was performed by electropolishing at a current density of 300 mA cm^{-2} during 3 sec in an HF (49 %): ethanol (1:3, v:v) electrolyte. Finally, the porous film was rinsed with ethanol several times and dried under a N_2 flow. The layer porosity was experimentally evaluated around 60 % by gravimetry (SI.1.).

b. Annealing post treatment

Rapid Thermal Annealing device, JetFirst from J.I.P.ELEC, was used to perform the annealing post-treatment. Samples were placed under a nitrogen environment and exposed to three different annealing temperature 500, 700 and 900°C respectively with a same duration of 30 sec.

c. Characterization

i. SEM

The porosity evolution with annealing temperature was observed by scanning electron microscopy (SEM) using Hitachi S-4800. All dimension (pore diameters, wall thicknesses) measurements were realized using imageJ software.

ii. Nitrogen sorption analysis

The surface area was evaluated according to the Bruner–Emmett–Teller (BET) nitrogen gas sorption method with ASAP2000 system. Prior to each measurement, a degassing step of 12 h at 50°C under a pressure of 0.01 torr was performed.

iii. XRD – Rocking curve scan

The phase characterization was performed by powder X-ray diffraction (XRD) on a Philips X'Pert 2theta/omega diffractometer equipped with an X'Celerator detector and Cu Kα1 radiation (λ = 1.510562 Å). The results are displayed in SI.2. Rocking curve measurements have been carried out using a PANalytical X'Pert MRD diffractometer in high-resolution configuration. This configuration includes one mirror and one primary beam monochromator to remove the $K_{\alpha 2}$ and K_{β}, so the radiation source is pure Cu-$K_{\alpha 1}$ (λ = 1.5405929 Å). As the wafer is (100) orientated, the measurements were

carried out around the Si(400) reflection, using the substrate peak centered on 34.5645° ω as reference. The two axes ω and ϕ were systematically optimized before each measurement to ensure the reproducibility of the results. The spatial homogeneity of the sample has been verified by collecting five rocking-curves for different positions of the sample (sample center, centers of four quarter of the sample). Rocking-curves ω scan were measured for different ϕ values, from 0° to 180°, to investigate the parallelism between the bulk and the porous frameworks. Cartography and rotation measurements are presented in SI.3.

iv. Surface wettability analysis

The contact angle analysis of the electrolyte solution droplets ($LiPF_6$ 1M in EC/PC/3DMC + 1 % VC + 5 % FEC) at the porous Si material surfaces was performed with an automated goniometer. 5 µL droplets were deposited and two images of their profiles were taken using a CCD camera (at 10 s time intervals) and ImageJ software for the analysis.

B. Preparation of electrodes and coin cell fabrication

Silicon porous films were grinded in agate mortar and used as active material, Super P (H30253 Carbon black Alpha Aesar) and Vapor growth fibers (VGCF-H, BET = 15 m^2/g, Showa Denko) were used as conducting agent in a 50:50 weight ratio and sodium carboxymethyl cellulose (MW = 250 000; DS = 0.9, Sigma Aldrich) was used as binder. The electrode components were thoroughly mixed in a pH = 3 buffered aqueous solution (700 µL) with a weight ratio of 18:70:12 (Si:VGCG/SP:CMC) respectively to prepare a slurry. The slurry was spread on copper foil with a controlled

thickness of 150 µm using a 3540 bird film applicator from Elcometer, and subsequently air-dried at room temperature for 24 h. The electrodes were then punched into 12.7 mm-diameter disks and dried at 80 °C under dynamic vacuum overnight. The dry electrodes were not calendered. The total material loading was approximately 1.2 mg cm^{-2} (0.25 mg cm^{-2} for Si), corresponding to a density of 0.4 g cm^{-3} approximately.

Coin cells (2032) were assembled in an Argon filled glovebox and used for the evaluation of electrochemical cycling performance. The coin cell was composed of the porous Si-based working electrode and a lithium foil at the counter electrode, the two electrodes were separated by a glass-fiber paper (GF/D, Whatman) soaked with the electrolyte. The electrolyte used was $LiPF_6$ 1 M in EC/PC/3DMC (Solvionic), 5%v of FEC (98% purity, Alfa Aesar) and 1%v VC (80 ppm BHT as stabilizer, 99% purity) were added.

C. Electrochemical measurements

The electrochemical galvanostatic measurements were performed between 1.5 and 0.01 V vs Li^+/Li at a current density of C/20 (178 mA g^{-1}) for the first cycle, referred to as the formation cycle, and then at C/5 (716 mA g^{-1}) for the further cycles. The weight of carbons (Super P, carbon fibers) and the silicon particles were considered for the gravimetric capacity calculated per gram of silicon and carbon. The expected specific capacity is approximately 775 mA h $g^{-1}_{(Si+C)}$ corresponding to a theoretical amount of inserted Li^+ close to 0.40 in the electrode. This capacity is calculated by considering the molar composition of the composite from its mass composition ($C_{0,9}Si_{0,1}$), and the values of the experimental capacity of the carbon composite (185 mA h g^{-1}) and

theoretical capacity of silicon (3580 mA h g^{-1}) considering the formation of the alloy $Li_{15}Si_4$ as an end-product of the lithiation. The expected capacity calculation with complete explanation is shown in SI.4. In all case, it is important to note that capacity value is not perfectly reproducible, these variations come from the masse evaluation depending on the film homogeneity. The following tests were carried out using a Neware BTS4000 battery cycler at 25 °C. All the electrochemical measurements were repeated a minimum of three times. Variable current density tests have also been carried out from C/20 to 20C to investigate the rate capability.

III. RESULTS AND DISCUSSION

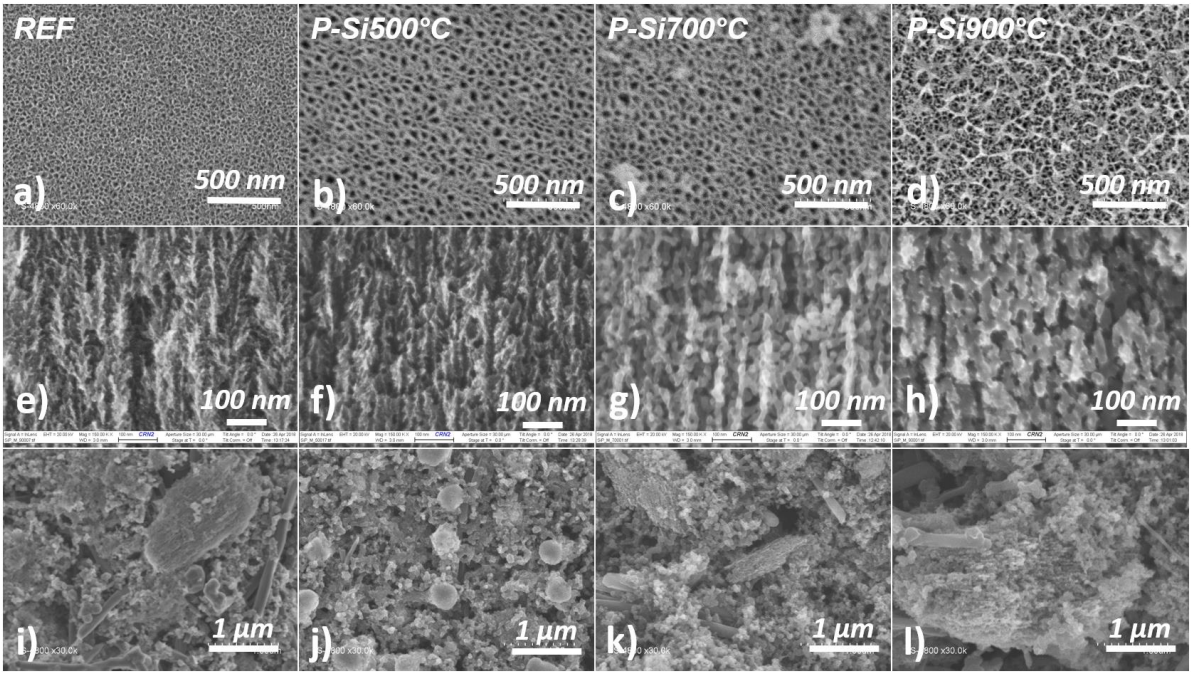

Figure 1: SEM image of a)PSi(REF) ,b) PSi(500°C), c) PSi(700°C), d) PSi(900°C) from top of the film ; Cross section of e)PSi(REF) ,f) PSi(500°C), g) PSi(700°C), h) PSi(900°C) ; Electrode view of I) PSi(REF) ,j) PSi(500°C), k) PSi(700°C), l) PSi(900°C)

The SEM images are displayed on Figure 1, the a. b. c and d. images show top views from the PSi(REF), PSi(500°C), PSi(700°C) and PSi(900°C) respectively. A

mesoporous morphology is observed for the PSi(REF) obtained by electrochemical etching with pores diameter around 25 nm and walls thickness of 10 nm (fig.1a). Increase of the pore diameter from 25 to 50 nm, together with increase of the walls thickness from 10 to 25 nm is observed upon annealing treatment at 500 °C, without major texture modification from the reference sample (Figure 1.b). Swelling of the walls was due to the material rearrangement during annealing post treatment. After annealing at 700 °C and 900 °C, no important changes is seen thanks to top view images (Figure 1.c and d.). Cross section images show for all vertically orientated pores (Figure 1. e,f,g and h) and an important change in the porous silicon films textures for PSi(700 °C) and PSi(900 °C). Silicon walls appeared as a chain of silicon particles of 25-50 nm (fig 1.c and g) and over 50 nm (Fig. 1.d and h) for films annealed at 700 °C and 900 °C respectively. Finally, the electrode views (Fig. 1 I, j, k and l) prove the porous silicon architecture conservation during the electrode elaboration through the observation of orientated lines corresponding to the pores on the biggest particles. It is also possible to observe the carbon fibers (longest particles) and super P (smallest particles).

This is known from the literature that post annealing treatment of porous silicon at high temperatures (over 350 °C) allows material rearrangement generating bigger pores and thicker walls as observed for the different porous films annealed. During high temperature treatments, porous silicon undergoes pores growth by stress induced lattice diffusion and surface diffusion. The pore shape modification is driven by silicon surface diffusion. The surface atoms have one, two or three bonds, whereas bulk atoms have four neighboring Si bonds. In fact as they have vacant nearest neighbor sites the silicon surface atoms move to lower surface energy. Moreover, the thermal

stress creates excess vacancies diffusing to the pore edges contributing to void growth and to the smallest pores shrinkage closed by sintering. [27],[28][29]

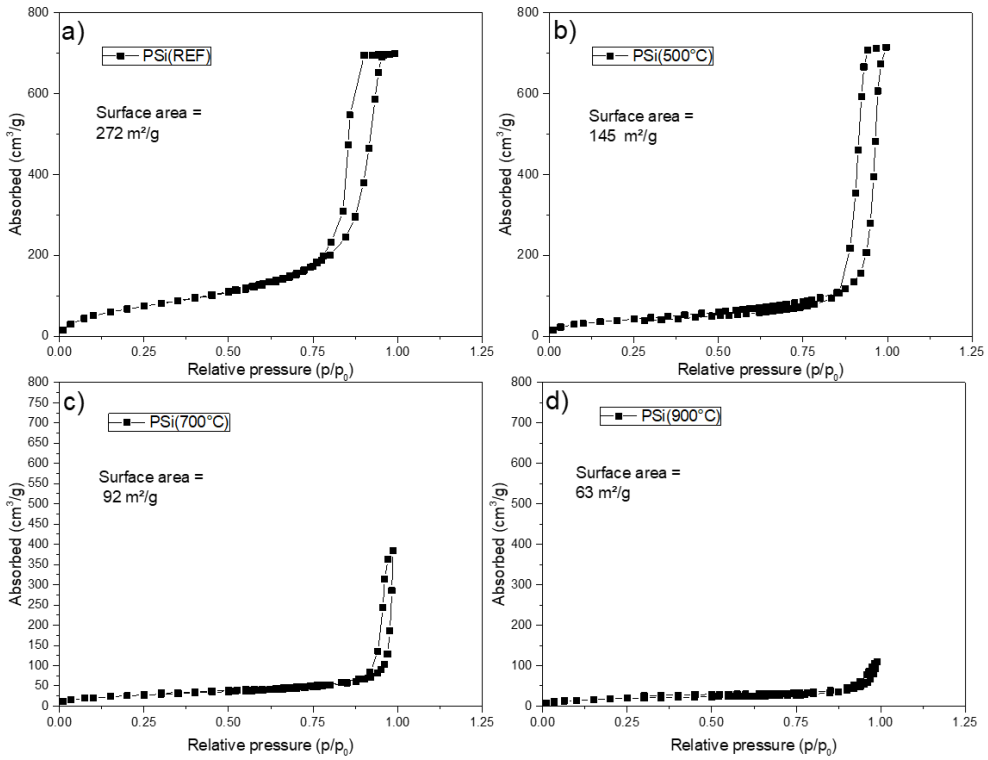

Figure 2: Nitrogen sorption isotherms for a) PSi(REF), b) PSi(500°C), c) PSi(700°C), d) PSi(900°C)

In order to complete the textural organization understanding, nitrogen sorption analysis was performed. The results are presented in Fig.2. PSi(REF) and PSi(500 °C) pre and post annealed materials respectively, exhibit type IV isotherms typical from mesoporous structures. In the case of PSi(REF) the hysteresis loop does not show parallel and vertical adsorption and desorption branches probably indicating a large pore size distribution and interconnected pores. After the first annealing at 500 °C (Fig.2b), an important reduction of the surface area is observed (from 272 to 145 $m^2 g^{-1}$), consistently with the increase of the pore diameters. Moreover, the two

adsorption/desorption branches are vertically aligned indicating a better pore size homogeneity. The isotherms obtained for PSi(700°C) and PSi(900°C) are consistent with a macroporous structure and exhibit lower surface areas with a decreasing contribution of the microporosity confirming the small pores coalescence and so the possibility to use annealing post treatment as an efficient way to tune the porosity.

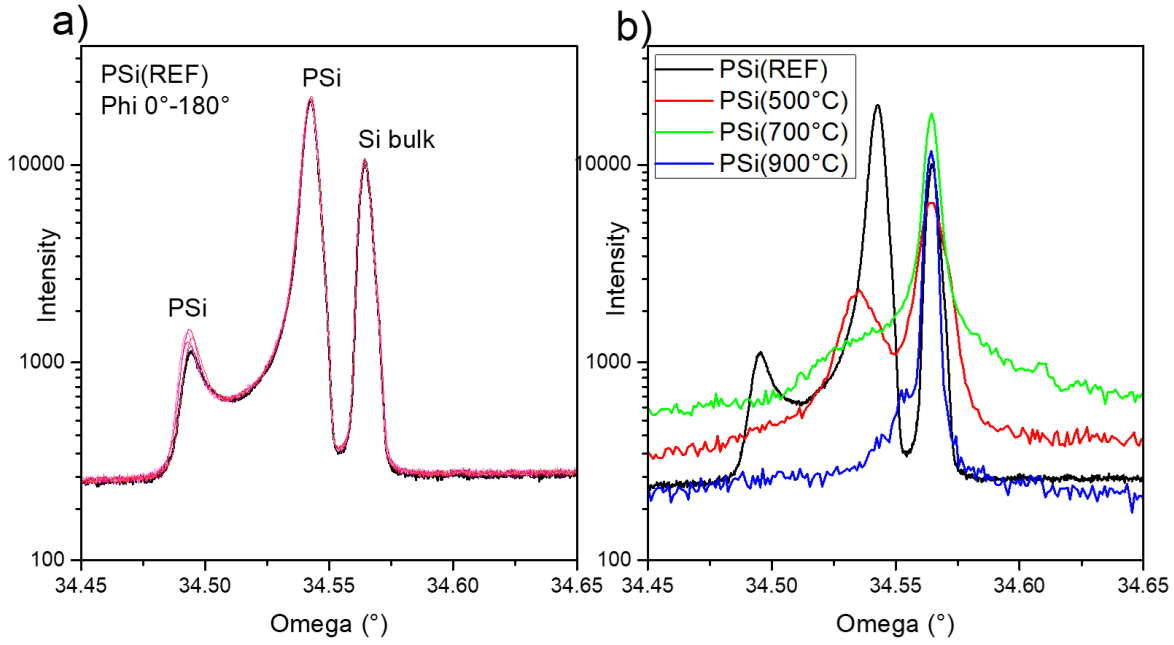

Figure 3: a) Rocking curve of porous silicon membrane PSi(REF) with different ϕ orientation b) Rocking curves of the annealed materials PSi(500°C), PSi(700°C), PSi(900°C) compared to PSi(REF).

No broadening nor shift of the Si peaks can be observed using regular Bragg-Brentano powder XRD (SI.2). Wafer crystalline purity and orientation are conserved by electrochemical etching and annealing post treatment. Higher accuracy is needed to observe the crystalline modifications (SI.2). The crystalline properties of the porous silicon (PS) film obtained by ω scan rocking curve X-ray diffraction are presented in Fig. 3. For the PSi(REF) sample presented in Fig.3a), three peaks can be observed.

The peak at Ω = 34.57° corresponds to the expected position of the lattice planes parallel (400) to the Si(100) bulk Si surface reflection. The two other peaks observed at lower ω angle are due to the porous layer which suffers from lattice distortion and lower crystalline quality. As already demonstrated by Bellet et al., the porous lattice parameter mismatchs the wafer's one as a function of the layer porosity.[30]. These peaks appear at a smaller angle than the bulk silicon and thus corresponds to a higher lattice parameter. This shift toward lower angle is due to the chemical adsorption of hydrogen on the porous surface which constrains the lattice parameter [27]. The two peaks coming from porous structures observed in the PSi(REF) sample, are probably due to the formation of a heterogeneous porous membrane. Indeed, in the case of thick membrane elaboration, the fluoride ions diffusion can be limited modifying the etching rate and creating different porosities [31]. Moreover, the peak observed at the lowest ω position shows a fluctuating intensity (SI.3 - Fig.2.a) while observing different positions of the surface sample. This also plead for a non-homogenous layer. After 500°C annealing, only two peaks left, it seems that the peak previously observed at lowest ω vanished and the one coming from the porous structure decreased significantly due to the material reorganization. The peak from the porous layer appears larger due to the surface change during annealing. Indeed, the reorganization starts by hydrogen desorption around 260°C and from 350°C the lattice spacing starts to decrease [30]. Hydrogen desorption creates dangling bonds increasing Si-Si bonds formation. Moreover, Ogata et al. explained that amorphous-crystalline transition takes place when the temperature is higher than 700 °C justifying the diffuse pattern observed for the 700°C annealed. With higher temperature (900 °C), the porous layer reorganizes entirely leading to the smallest in plane lattice mismatch.

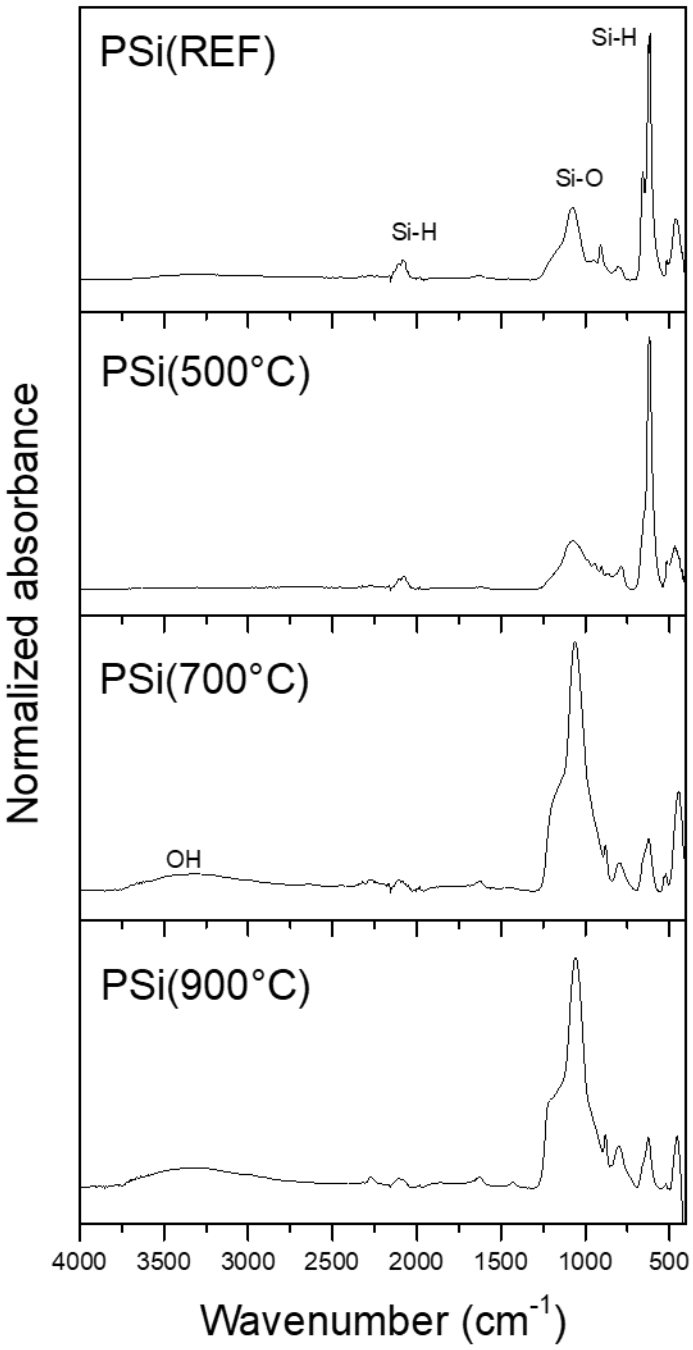

Figure 4: *ATR-FTIR spectra of porous REF film and Porous Si film annealed at 500°C, 700°C, and 900°C*

Fourier transform infrared (ATR-FTIR) was used to characterize the sample chemical surface evolution with annealing (Figure 4). The PSi(REF) exhibits a silicon hydride surface with the characteristic vibration bands for Si-H bond at 2100 cm^{-1} and 622 cm^{-1}. In addition, low surface oxidation was observed with the presence of a

relatively small band at 1070 cm^{-1} corresponding to the Si-O vibration mode.[32] The 500 °C annealing post treatment did not induce significant change in the chemical surface properties of the porous Si film. In contrast, annealing at higher temperatures (700 °C and 900 °C) induced a larger surface oxidation of the porous Si film with a more intense Si-O vibration band observed at 1070 cm^{-1}, and with the appearance of a broad band centered at 3300 cm^{-1} assigned to the -OH bond vibration. These two observations are in good accordance with the previous rocking curve measurements. Literature indicates that the surface of freshly etched silicon without or with low temperature annealing treatment exhibits hydrogen on the surface and that higher temperature annealing leads to hydrogen desorption and so a higher reactivity to atmospheric oxygen inducing surface oxidation.[27]

These different characterizations have shown that the annealing post treatment proved its efficiency to adjust the porous silicon morphological properties as pore shape, pore size and wall thickness (crystallite size). Indeed, annealing allows material reorganization, both the pores and the walls grow reducing the surface area and retaining a highly crystalline and porous structure. This surface driven reorganization also plays on the later surface oxidation. At 500°C annealing temperature, only a slight morphological change is observed which already double the pore diameter and thickness. Above 700°C, the morphology is impressively changed with increasing characteristic dimensions. It is interesting to study the impact of these structural/morphological properties on the electrochemical behaviour in lithium battery.

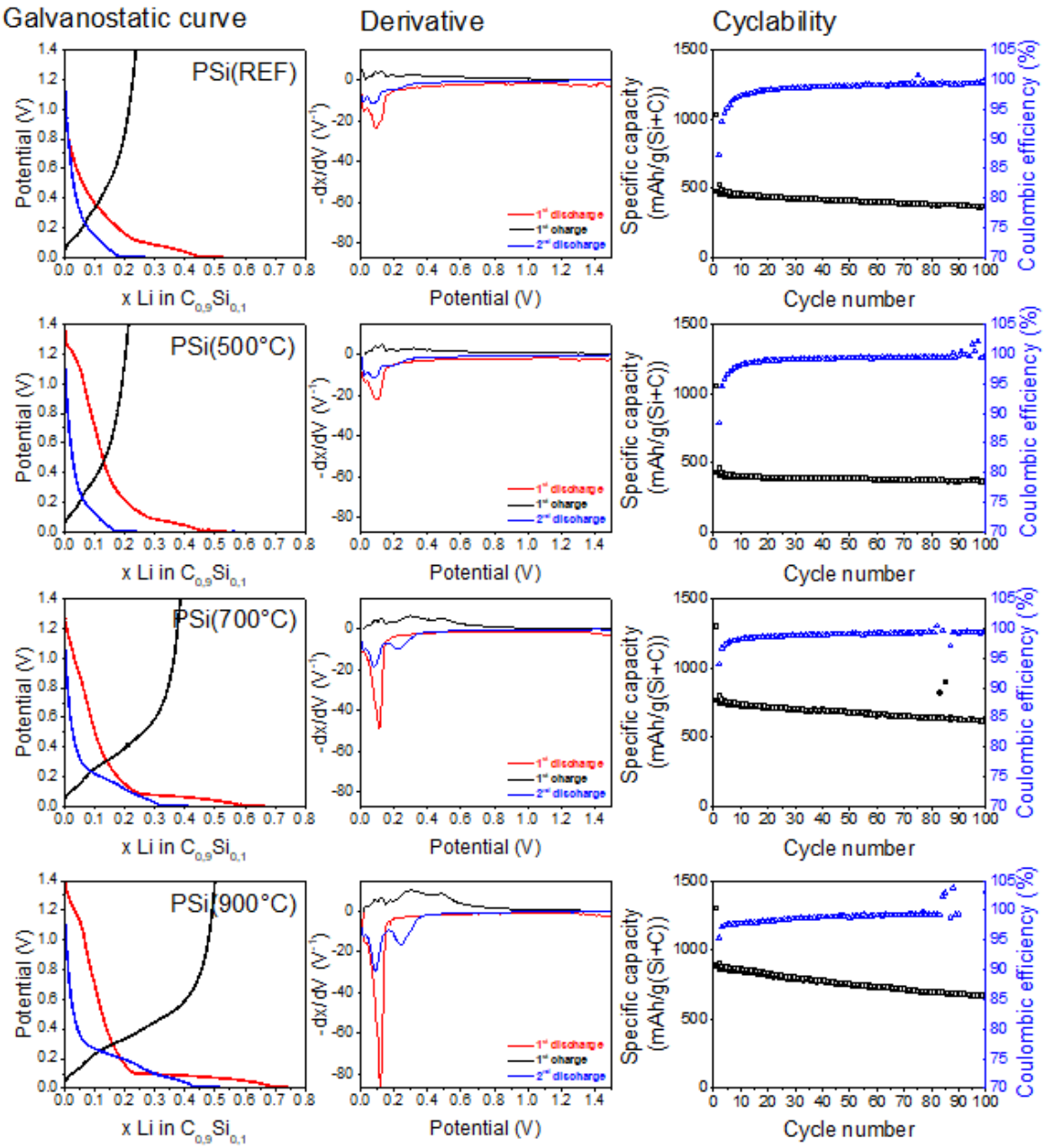

Figure 5:

a)d)g)j) Galvanostatic profils of the first and a half cycles at 0,178 A $g^{-1}_{(Si+C)}$ for the first cycle and 0,716 A $g^{-1}_{(Si+C)}$ b)e)h)k) Derivatives c)f)i)l) Capacity retention over 100 cycles. Formulation 18%SiP/70%(SuperP/VGCF)/12%CMC – 0,01-1.5 V

The silicon-based electrodes were electrochemically tested by galvanostatic assays in order to compare their performance *versus* Li^+/Li. The first cycle profiles measured at

a current of 178 mA $g^{-1}_{(Si+C)}$, the second discharge measured at 716 mA $g^{-1}_{(Si+C)}$ between 0.01 and 1.5 V. The corresponding derivative curves, as well as the capacity retention and the coulombic efficiency over 100 cycles are represented on Fig. 5.

In first discharge the potential of PSi(REF) decreases slowly down to 0.01 V, which represents the consumption of 0.3 Li. This characteristic potential evolution can be ascribed to the electrolyte reduction to form the solid electrolyte interphase (SEI) which leads to a very low coulombic efficiency for the first cycle of 46 %. The derivative curve of the 1st discharge shows a small pic at 0.1 V corresponding to the lithium silicon amorphous alloy formation.[33] In further cycling around 0.25 Li are reversibly exchanged resulting in a capacity of 450 mAh $g^{-1}_{(Si+C)}$. Considering 3,75 Li/Si as the higher theoretical lithiation ($Li_{15}Si_4$) with a capacity of 3580 mA g^{-1}, the experimental capacity of carbon additives around 185 mAh $g^{-1}_{(Si+C)}$ (SI.4) and the atomic ratio between silicon and carbon in the electrode, a capacity of 775 mAh $g^{-1}_{(Si+C)}$ is expected (insertion of 0,40 Li in $C_{0,9}Si_{0,1}$). The low lithiation of PSi(REF) electrode could be due to a limited electrolyte accessibility to the silicon. [34]

The galvanostatic curves obtained for the 500 °C annealed porous Si-based electrode is very close to that of PSi(REF). In all the three cases of annealed samples the potential progressively decreases in first discharge from 1.3 V to 0.1 V where a voltage plateau takes place. However for higher annealing temperatures 700 °C and 900 °C, an increasing reactivity vs Li is observed, through a longer voltage plateau at 0.1 V. The associated derivate curves confirms it through the intensity rise of the peak at 0.1 V in first discharge but also by the presence of the two other broad peaks at 0.25 and 0.1 V in further discharges corresponding to the electrochemically-driven solid state amorphisation accompanying the Li-Si alloys formation [33]. In second cycle reversible oxidative peaks appear at 0.3 and 0.45 V. These derivative peaks are in

good agreement with those described in the literature for the lithiation/delithiation of Si [33]. The cyclability over 100 cycles with a current density of 715 mA $g^{-1}_{(Si+C)}$ was measured for the four samples and the performance are reported in table 1. Close performance are reported for PSi(REF) and PSi(500°C) electrodes with low reversible capacity of 475 and 427 mAh g^{-1} in first cycle but a good stability with a capacity retention above 70 % after 100 cycles with a coulombic efficiency around 99.5 %. As discussed above the first cycle coulombic efficiency is improved for high temperature annealing Si electrodes from 46 % for PSi(REF) and 40 for PSi(500°C) to around 59 % for PSi(700°C) and to 68 % for PSi(900°C). PSi(900 °C) shows the highest first coulombic efficiency which is correlated with the lowest surface area accessible for the electrolyte reduction. Lowering the surface area limits SEI formation and consequently the first irreversible capacity. However, only 73% of the capacity is retained after 100 cycles. This is probably due to the volume buffer effect loss. Indeed, at such a high annealing temperature, the PSi(900°C) material exhibits the largest constituting pore walls inducing internal stress rise during lithiation.

In comparision, PSi(700°C) still shows higher initial coulombic efficiency than PSi(REF) and PSi(500°C) thanks to its lower surface area. PSi(700°C) also exhibits a higher capacity which could be linked with a more efficient contact between the electrolyte and the active material, in fact increasing the electrolyte access with larger pore, probably enhances lithium diffusion and thus Si reactivity. Finally, a better cyclability is also observed for PSi(700°C) compared with PSi(900°C) attributed to its limited crystallites size composition.

Table 1: Capacity evolution over 100 cycles

Active material	*Capa. D1*	*EC (%) D1*	*Capa. D2*	*Capa. D10*	*EC (%) D10*	*Capa. D100*	*EC (%) D100*	*100/ D2*
PSi(REF)	1029,7	46,1	525.4	458,5	97,3	369,4	99,3	70%
PSi(500°C)	1054,3	40,6	460,6	404,5	98,1	362,8	99,4	78%
PSi(700°C)	1302,0	58,8	796,9	740,2	98,2	616,3	99,4	77%

PSi(900°C)	1302,3	68,2	904,6	862,1	97,8	666,1	99,3	73%

In order to confirm the hypothesis of the better electrolyte penetration in the annealed material PSi(700°C) and PSi(900°C) and explain the variations in electrochemical performance, contact angle experiments with the electrolyte were performed. The contact angle images are available in SI.5 and Table 2 summarizes the results. For the PSi(REF) and the PSi(500°C) the electrolyte drop forms a contact angle around 30° and 20° respectively and it is not possible to observe the drop absorption before its evaporation. In these two examples the electrolyte shows limited penetration in the porous material, this behavior can be associated either to poor chemical interaction between electrolyte and silicon hydride surface or to too small pores limiting the electrolyte diffusion. From 700°C, the drop disappears quickly indicating enhanced electrolyte penetration in the porous structure which can still be related with the oxidized surface or pore size. These results (cf. Table2) show a positive impact of the annealing post treatment on the electrode wettability by the electrolyte leading to obvious improvement of the electrochemical performance.

Table 2 : Electrolyte wettability test sum-up

	Left angle	Right angle	Observations
PSi(REF)	32,2	30,7	The drops does not penetrate and had time to evaporate
PSi(500°C)	20,6	18,4	The drops does not penetrate and had time to evaporate
PSi(700°C)	close to 0	close to 0	The drop disappears in 8s
PSi(900°C)	0	0	The drop disappears in 5s

Finally, variable current-rate (C-rate) tests were carried out on porous Si-based electrode. As presented on the Fig. 6 the material annealed at 700°C and 900°C

exhibits correct resistance of the capacity to current rise, a capacity of 600 mAh $g^{-1}_{(Si+C)}$ is maintained up to C. This good behavior observed at high rate for the annealed material confirms the benefit from larger pore on the total interface resistance and Li diffusion. The poor cycling at high rate for the PSi(REF) and PSi(500°C) seems to verify this hypothesis, the smallest pores may be blocked by the large amount of SEI in the pores. Higher rate shows a rapid capacity fading. The porous Si obtained here by etching and annealing at 700 and 900 °C has shown morphological and chemical modification, which appears favorable for the lithiation/delithiation in the electrode. Indeed higher capacity and rate capability were measured specifically for the 700 °C annealed sample.

Gavouze et al. indicate that the electrochemical etching of a p-type (100) oriented wafer follows the (100) direction and the resulting porous material exhibits (111) facets at the bottom of the pores and (110) along the walls.[35] According to Kuzma-Filipek [36] the annealing of a porous material causes the reorganization of the surface Si atoms to minimize the energy and this would thus favor the formation of (111) and also (100) facets but in a smaller amount, which possess the lowest energies.

To use as a negative electrode active material in LiBs, it is interesting to note that the Li diffusion rate varies with respect to the crystalline orientation. A theoretical study suggests, for example, that lithium diffuses at least two orders of magnitude quicker along the Si crystal direction (100) than along the (111)[37], which should be responsible for the anisotropic volume expansion of silicon. The insertion of lithium would be energetically favored according to (110) plans compared with (100) or (111). These calculations perfectly match the experimental observations.[38]

In this study and according to the literature, the annealing post treatment should increase the number of facets (111) and facets (100) and these facets do not facilitate

the lithiation for kinetic reasons. Therefore, the observed improvement in cycling performance cannot benefit from it and should be entirely due to the optimization of pore size and surface composition.

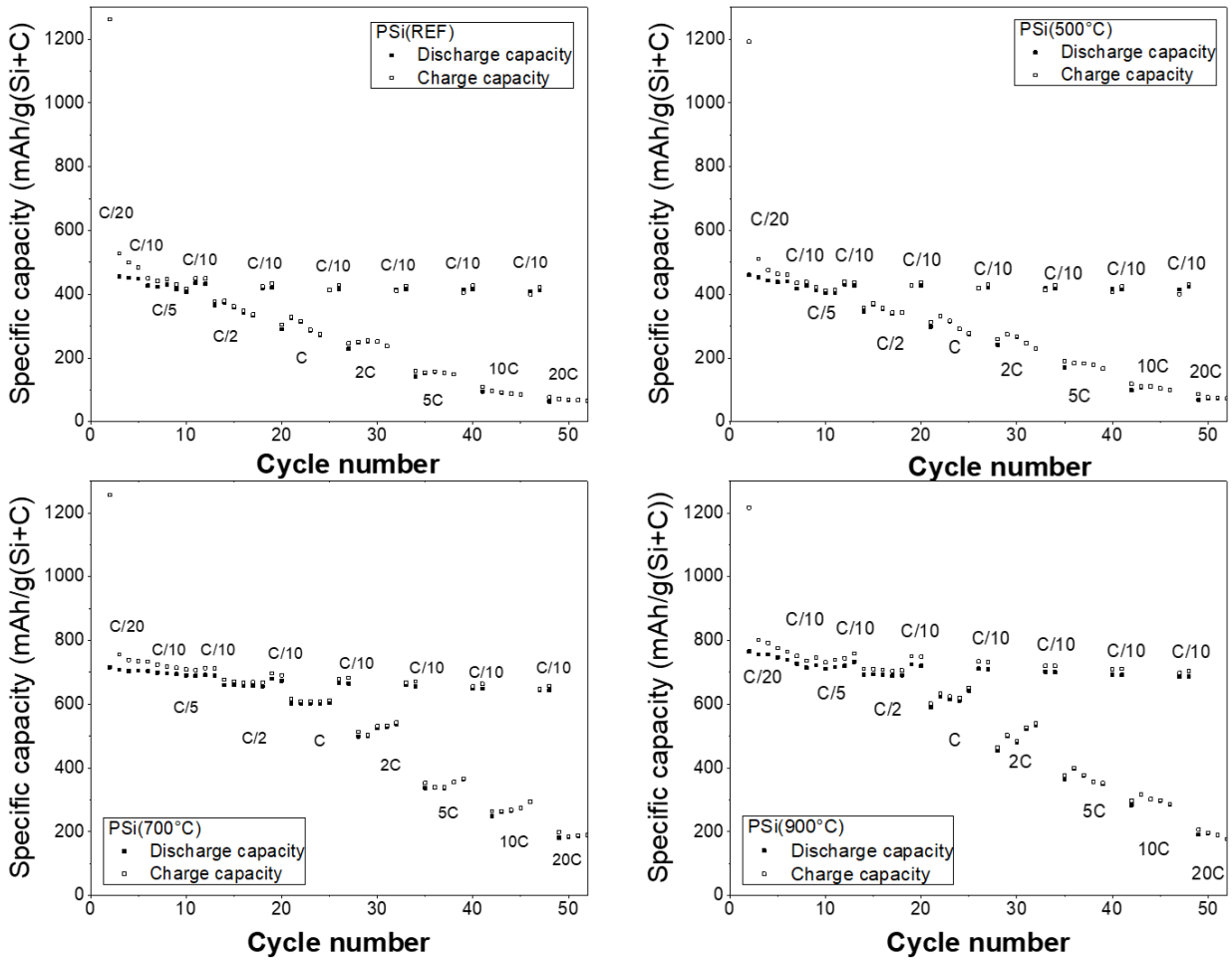

Figure 6 : Variable Current-rate measurements - 0.01-1.5V Vs Li^+/Li

IV. CONCLUSION

In this study, we successfully used rapid thermal annealing to modify porous membranes obtained by electrochemical etching of silicon wafer. Annealing led to the

modification of the porous silicon morphological properties: larger pores and bigger crystallites sizes (Fig.1) were observed with an increased annealing temperature. The modification of the morphological properties led to surface nature modification, with higher oxidized surface which seems to increase the wettability of the porous Si by the alkyl carbonate based electrolyte (as demonstrated through contact angle experiments). To optimize the porous silicon activity in negative electrode for LiB it was shown that a simple 700°C annealing treatment leads to i) a highly porous structure able to limit the pulverization which is a consequence of the volume changes during the alloying mechanism, ii) large pores with limited surface area, beneficial for the electrolyte penetration and which limit the SEI formation, and to iii) a limited crystallite size to avoid structural fragility with lithium insertion.

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