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Christoforos Theodorou, Gérard Ghibaudo. Noise and Fluctuations in Fully Depleted Silicon-On-Insulator MOSFETs. Noise in Nanoscale Semiconductor Devices, 2020. hal-03090062

HAL Id: hal-03090062

<https://hal.science/hal-03090062>

Submitted on 29 Dec 2020

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Noise and fluctuations In Fully Depleted Silicon-On-Insulator MOSFETs

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1. Introduction

The Semiconductor-On-Insulator (SOI) philosophy offers a great control over the transistor channel: the device body is isolated between two oxides: the gate oxide that all classical MOSFETs have and the so-called buried oxide (BOX) [1]. The first device parameter that was not at all controlled in classic Bulk MOSFETs was the channel thickness. Reducing the thickness of the silicon body provides a better subthreshold slope [2], a very efficient control of the short-channel effects (SCEs), as well as the drain-induced barrier level (DIBL). Furthermore, the SOI structure allows for application of back-bias to control the threshold voltage value. In addition, the threshold voltage variability can be dramatically reduced, since there is no need for strong doping in the channel. Actually, the film is so lightly doped that it is already partially depleted (PD) or fully depleted (FD) even before applying bias voltages. In this way, ultra-thin body (UTB) SOI MOSFETs can be designed and produced, with a silicon film thickness from around 7 to 14 nm. However, as we will later show, the reduction of the film thickness can lead to serious electrostatic coupling effects between the front and back gate. Finally, by reducing the BOX thickness from the typical 145-300 nm value down to 8-25 nm, the device is called ultra-thin body and buried-oxide (UTBB) FDSOI MOSFET [3] and offers an easier back-bias threshold voltage control.

FD-SOI technology is considered one of the best candidates for Short Channel Effect (SCE) control in future sub-28 nm CMOS generations, while it remains compatible with standard planar CMOS technology [3]–[7]. The use of a midgap/high-k metal gate stack with undoped SOI films allows for great improvement of variability as compared to bulk technology [4], [8], [9]. The use of ultra-thin body and buried oxide thickness (UTBB) also enables to enhance the technology scalability, providing an ideal subthreshold slope and better drain-induced barrier lowering (DIBL), as well as larger back-to-front gate coupling effect useful for threshold voltage V_{th} control.

Besides, low frequency noise and RTS fluctuations which scale with the reciprocal device area, become more important with technology scaling down. They are not only limiting the analog circuit operation, but they could also jeopardize the digital circuit functioning. They could even appear as an ultimate variability source due to dynamic carrier trapping in undoped channel devices. For these reasons, the study of LFN and RTN in UTBB FDSOI is a key issue for technology evaluation and evolution.

Furthermore, it has been repeatedly shown that the LF noise in FDSOI devices can be influenced by the coupling effect between the back and front interfaces [10]–[14]. Due to this coupling, it is difficult to predict precisely the contribution of each interface to the measured noise. Moreover, application of a positive or negative bias voltage to the buried oxide can possibly lead to the appearance of either Lorentzian-type noise [10],[15],[16], or a significant increase of the flicker noise level [11], [17]. Thus, the analytical study of the noise sources and their dependence on the bias conditions is crucial for both device characterization and noise modeling.

In this chapter, after a brief theoretical introduction on the fluctuation mechanisms in MOSFETs, we present the most important aspects of our recent research work concerning the noise characterization and modeling of FDSOI MOSFETs, as well as the development of circuit noise simulation methods. The aspects of front/back gate coupling effects on both flicker and generation-recombination noise, as well as the LFN variability phenomenon, are covered in detail.

2. Theoretical background

2.1. Origin of low-frequency noise in MOSFETs

a. Carrier number fluctuations and correlated mobility fluctuations (CNF/CMF)

Within the classical carrier number fluctuation approach, the fluctuations in the drain current arise from the fluctuations of the inversion charge located at the gate dielectric interface, and which stem from the variations of the interfacial charge due to trapping–detrapping of free carriers into slow dielectric traps. The interface charge variation δQ_{it} can be translated into a flat band voltage variation as $\delta V_{fb} = -\delta Q_{it} / (WLC_{ox})$, C_{ox} being the gate dielectric capacitance and WL the device area [18]. A rigorous detailed analysis should also account for the correlated mobility fluctuations $\delta \mu_{eff}$ due to the modulation of the Coulomb scattering rate by the interface charge fluctuations. The overall drain current fluctuations therefore become for the linear operation region [19], [20].

$$\delta I_d = -g_m \delta V_{fb} - \alpha I_d \mu_{eff} \delta Q_{it} \quad (1)$$

where g_m is the transconductance, μ_{eff} is the effective mobility, α is the Coulomb scattering coefficient ($\approx 10^4$ Vs/C for electrons and 10^5 Vs/C for holes [21], [22]).

This yields a normalized drain current noise given by [3]:

$$\frac{S_{Id}}{I_d^2} = S_{Vfb} \left(\frac{g_m}{I_d} \right)^2 \left(1 + \alpha \mu_{eff} C_{ox} I_d / g_m \right)^2 \quad (2)$$

and to an input-referred gate voltage noise S_{Vg} , at strong inversion as,

$$S_{Vg} = \frac{S_{Id}}{g_m^2} = S_{Vfb1} [1 + \alpha \mu_0 C_{ox} (V_g - V_t)]^2 \quad (3)$$

where μ_0 is the low field mobility, V_t the threshold voltage and

$$S_{Vfb} = \frac{S_{Qit}}{WLC_{ox}^2} \quad (4)$$

the flat band voltage power spectral density (PSD), with S_{Qit} being the PSD of the dynamic interface charge per unit area. Note that S_{Vg} is different from S_{Vfb} , especially at strong inversion where CMF prevail.

The PSD of the interface charge is intimately related to the physical trapping mechanism into the gate dielectric. For a tunnelling process (McWorther scheme [23]), the trapping probability decreases exponentially with dielectric depth, so that the PSD of the flat band voltage reads for a uniform trap depth profile [23], [24]:

$$S_{Vfb} = \frac{q^2 kT \lambda N_t}{WLC_{ox}^2 f} \quad (5)$$

where f is the frequency, λ is the tunnel attenuation distance (≈ 0.1 nm in SiO_2), kT is the thermal energy and N_t is the volumetric trap density ($/\text{eVcm}^3$). However, some experiments [25], [27] show that the time constants are either weakly or not at all correlated with depth. In that case, one has to

consider that the trapping probability decreases exponentially with the activation energy of the defect cross section E_a , as in thermally assisted trapping processes (Dutta scheme [28]). This is also consistent with Random Telegraph Noise data from [25], [27], [29]. Accounting for such a dependence of τ and E_a , the PSD of the flat band voltage takes the form [30]:

$$S_{V_{fb}} = \frac{q^2 k^2 T^2 N_{st}}{W L C_{ox}^2 f \Delta E_a} \quad (6)$$

where ΔE_a is the spread of the activation energy and N_{st} is the areal surface trap density ($/\text{eVcm}^2$).

The CNF-CMF derivation of Eq. (2) can be generalized within the gradual channel approximation to the non-linear MOSFET operation region after integration of the local sheet conductivity σ fluctuations along the channel, yielding [31]:

$$\frac{S_{I_d}}{I_d^2} = S_{V_{fb}} \cdot \frac{\int_0^{V_d} \left(\frac{1}{\sigma} \frac{\partial \sigma}{\partial V_{fb}} + \alpha \mu_{eff} C_{ox} \right)^2 \cdot \sigma \cdot dU_c}{\int_0^{V_d} \sigma dU_c} \quad (7)$$

where $\sigma = q \mu_{eff} \cdot Q_i$ with Q_i being the inversion charge and U_c is the channel potential.

As illustrated in Figure 1(a), the variation rate of the input gate voltage noise $S_{V_g}(V_d)$ strongly depends on the CMF amplitude factor (α) and shows clear presence of CMF in the experimental results as in Figure 1(b).

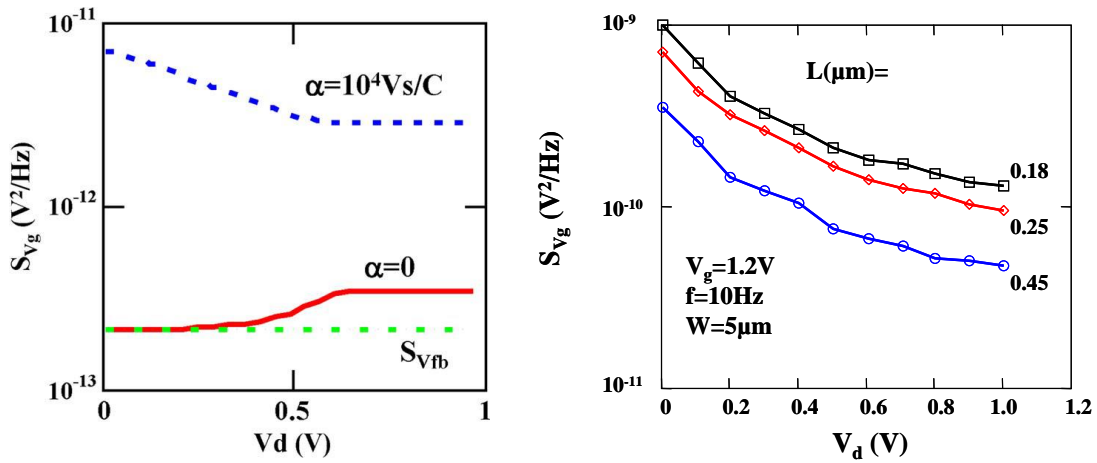


Figure 1. a) Theoretical $S_{V_g}(V_d)$ characteristics as obtained from CNF-CMF model of Eq. (7) and b) typical experimental $S_{V_g}(V_d)$ characteristics (after [31]).

b. Hooge Mobility fluctuations (HMF)

According to the Hooge mobility model [32], the drain current noise comes from the fluctuations of the carrier mobility stemming from variations in the scattering probability due to phonon number fluctuations [33], [34]. This results in a flicker noise with amplitude inversely proportional to the total number of carriers in the device. The normalized drain current noise in linear operation then reads [35]:

$$\frac{S_{Id}}{I_d^2} = \frac{q\alpha_H}{WLQ_i f} \quad (8)$$

where Q_i is the inversion charge and α_H is the Hooge parameter ($\approx 10^{-4}$ - 10^{-7}).

In the case of non-linear operation region, it can be shown that the normalized drain current noise becomes after integration along the channel [35]:

$$\frac{S_{Id}}{I_d^2} = \frac{q\alpha_H \langle \mu_{eff} \rangle V_d}{L^2 I_d f} \quad (9)$$

where $\langle \mu_{eff} \rangle$ stands for the average mobility along the channel.

As the Hooge mobility fluctuations depend only on the phonon scattering rate [36], the Hooge mobility parameter should be modulated by its contribution among other scattering mechanisms limiting the carrier mobility. Therefore, in the case of a MOSFET, the Hooge parameter should be written as:

$$\alpha_H = \alpha_{H0} \left(\frac{\frac{1}{\mu_{ph}}}{\frac{1}{\mu_{ph}} + \frac{1}{\mu_C} + \frac{1}{\mu_{SR}}} \right)^2 \quad (10)$$

where α_{H0} refers to the intrinsic Hooge parameter, μ_{ph} , μ_C and μ_{SR} are respectively the phonon, Coulomb and surface roughness scattering limited mobilities in the MOSFET inversion layer [37]. Accounting for the phonon, Coulomb and surface roughness scattering universal mobility law [37], [38] against effective electric field, the dependence of the Hooge parameter given by Eq. (10) can be evaluated theoretically with the MOSFET inversion charge from weak to strong inversion as illustrated in Figure 2. It clearly reveals that, in MOSFET, the Hooge parameter is far from being independent of inversion charge i.e. gate voltage while varying from subthreshold to strong inversion region. The Hooge parameter is maximized when the phonon scattering contribution prevails with respect to Coulomb and surface roughness scattering rates.

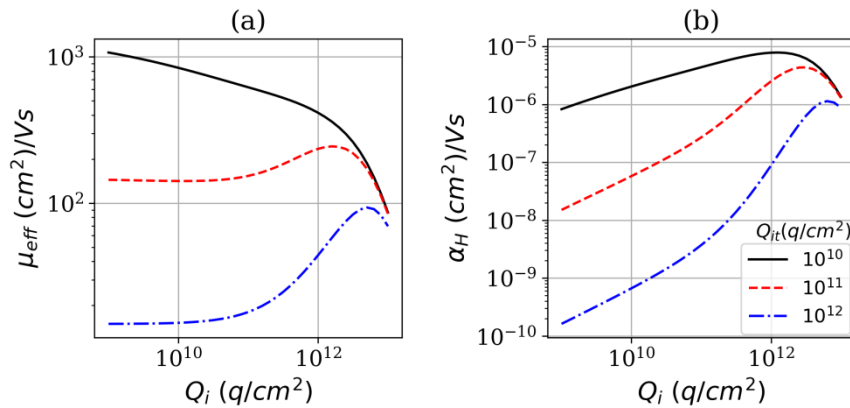


Figure 2. Theoretical variations of μ_{eff} (a) and Hooge parameter (b) with MOSFET inversion charge Q_i for various interface charge Q_{it} levels modulating the Coulomb scattering rate ($\alpha_{H0}=10^{-5}$).

Figure 3 shows the impact of the Hooge parameter dependence with inversion charge (Eq. (10)) on the associated normalized drain current noise. In this situation, S_{Id}/I_d^2 is no longer simply inversely

proportional to the inversion charge as it were the case for HMF model with constant mobility. Therefore, even if the Hooge model is empirical, the α_H parameter should not be considered constant with gate bias, due to its modulation by the interface charge Coulomb scattering.

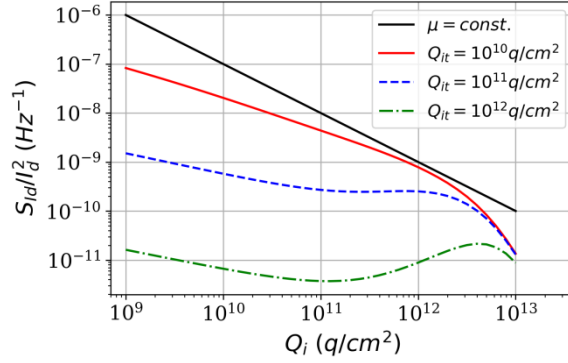


Figure 3. Variation of normalized drain current noise S_{Id}/I_d^2 with inversion charge for HMF model with Hooge parameter of Figure 2.

c. Impact of Access resistance

The impact of the access resistance R_{sd} on the LF noise can be obtained by adding to the channel drain current noise the LF noise component arising from the resistance of the source and drain access region. To this end, one should note that the sensitivity of the drain current to R_{sd} variation is simply given by,

$$\frac{\partial I_d}{\partial R_{sd}} = g_d + g_m/2 \quad (11)$$

where $g_d = dI_d/dV_d$ is the output conductance and assuming $R_{sd} = 2R_s = 2R_d$. Therefore, the extrinsic normalized drain current noise including the access region noise can be expressed as:

$$\frac{S_{Id}}{I_d^2} = \left(\frac{S_{Id}}{I_d^2} \right)_{channel} + (g_d + g_m/2)^2 S_{Rsd} \quad (12)$$

where S_{Rsd} is the PSD associated to the access resistance. In Eq. (12) the channel component is either calculated by the CNF/CMF (2)-(7) or by the HMF (9) model.

d. Random Telegraph Noise (RTN)

The observation of RTN in small area MOS devices in the 80s was attributed to elementary carrier trapping at the channel-gate dielectric interface [39], [40]. The drain current RTN was commonly interpreted as a conductance modulation due to the fluctuation in the carrier number with associated mobility fluctuations. The two-level RTN signal of a single trap is statistically characterized by three parameters: i) the average amplitude of the drain current jump ΔI_d between the low and high levels, ii) the average time passed on the high level normally associated to the capture time τ_c and iii) the average time passed on the low level normally related to the emission

time τ_e . In this case, the histogram of the drain current amplitude exhibits two peaks at a distance equal to ΔI_d . The histogram of the high and low level times are generally exponentially distributed due to the Poisson process governing the dynamic trapping events [41]. In the case where more than one traps are active under the same gate bias, the result is a multi-level RTN signal (not discussed here).

The drain current RTN amplitude can be evaluated by considering that the trapping of an elementary charge q from the channel into an oxide defect modulates the local conductivity [20], [41]. In a first order approximation, the relative drain RTN amplitude accounting for both CNF and CMF is given by [20], [42]:

$$\frac{\Delta I_d}{I_d} = \frac{g_m}{I_d} \frac{q}{WLC_{ox}} \left(1 - \frac{x_t}{t_{ox}}\right) \left(1 + \alpha \mu_{eff} C_{ox} I_d / g_m\right) \quad (13)$$

where x_t is trap depth in the gate dielectric and t_{ox} is the gate oxide thickness. Therefore, the drain current RTN relative amplitude is maximized in the subthreshold region where the transistor gain g_m/I_d is larger.

Furthermore, in order to account for abnormally high RTN amplitudes in dramatically scaled devices, a parameter η should be added to (13) [43]:

$$\frac{\Delta I_{ds}}{I_{ds}} = \eta \frac{g_m}{I_{ds}} \frac{q}{WLC_{ox}} \left(1 - \frac{x_t}{t_{ox}}\right) \left(1 + \Omega \frac{I_{ds}}{g_m}\right) \quad (14)$$

where η is unity for a homogeneous channel in the linear region and $\Omega = \alpha \mu_{eff} C_{ox}$ the CMF factor [44]. The large deviation of the parameter η from unity [45], [46]–[48] could be explained by the huge variability of the threshold voltage associated with single charge trapping, which exhibits an exponential distribution due to the impact of trap location within the gate dielectric and facing the channel [48], [49].

Regarding the trap kinetics, in general, the RTN capture and emission times are governed by the Shockley-Read-Hall statistics [41] and reads:

$$\tau_c = \frac{1}{\sigma n_s v_{th}} \quad (a) \quad \text{and} \quad \tau_e = \frac{1}{\sigma n_1 v_{th}} \quad (b) \quad (15)$$

where v_{th} is the thermal velocity, σ is the trap cross section, n_s is the surface carrier concentration and n_1 is the surface carrier concentration when the Fermi level E_f crosses the trap energy E_t . The trap cross section might depend on the trap depth into the oxide and on temperature as $\sigma = \sigma_0 \exp(-E_a/kT) \cdot \exp(-x_t/\lambda)$ [41].

However, when the trap is not located right at the oxide-channel interface, but at a depth x_t in the oxide, the apparent trap energy E_t depends on the band bending in the gate dielectric as [39], [41]:

$$E_t = E_{t0} - q \frac{x_t}{t_{ox}} (V_g - V_{fb} - V_s) \quad (16)$$

where V_s is the surface potential and V_g is the gate voltage. Another way to express this difference is through n_1 in Eq.(15)(b), if we replace it with:

$$n_1 = n_0 e^{\frac{\psi_{s1}}{kT}} = n_0 e^{\frac{\psi_{s1,0} - \Delta\psi_1}{kT}} \quad (17)$$

where ψ_{s1} is the surface potential for which E_t coincides with E_f , and $\Delta\psi_1 = x_t \cdot Q_i / \epsilon_{ox}$ corresponds to the potential drop across the oxide, from the interface to the trap depth.

It should also be noted that the capture and emission times of Eqs (15) are evaluated within the classical statistics i.e. using carrier volumetric concentration at the surface. They have to be updated when quantum mechanical effects become important in the MOSFET inversion layer, since n_s is cancelled out at the surface. Indeed, the capture probability is proportional to the escape frequency of the electrons in the quantized sub-band and to the barrier tunnelling transparency to reach the trap in the oxide. If in addition we take into consideration Eq. (17), the capture and emission time can be expressed in a way that accounts for the trap depth x_t and the single sub-band approximation:

$$\bar{\tau}_c = \frac{q}{\sigma \cdot f_e \cdot Q_i} \quad (a) \quad \text{and} \quad \bar{\tau}_e = \frac{q \cdot e^{\frac{x_t \cdot (Q_i + Q_d)}{kT \cdot \epsilon_{ox}}}}{\sigma \cdot f_e \cdot Q_{i1}} \quad (b) \quad (18)$$

where f_e is the escape frequency ($\approx 2 \cdot 10^{13}$ Hz), ϵ_{ox} is the oxide permittivity, Q_{i1} the inversion charge when the Fermi level E_f crosses the trap energy E_t and Q_d is the depletion charge. In Figure 4 are illustrated typical variations of the capture and emission times calculated with Eqs (18) as a function of gate voltage for a FDSOI structure and showing the usual huge decrease of τ_c and the slight increase of τ_e with V_g in strong inversion. It should be emphasized that this formulation (18) of the capture and emission times will also be of great interest for compact modelling applied to circuit simulation (see section 5).

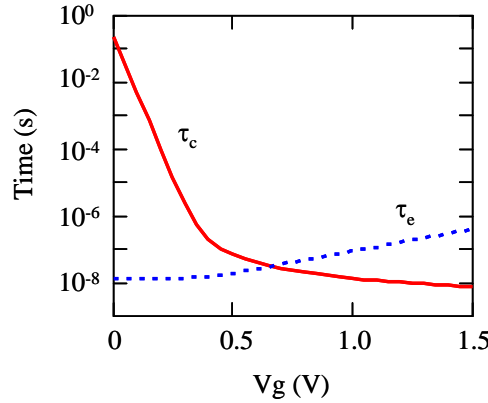


Figure 4. Typical variations of capture and emission with gate voltage for a FDSOI structure ($Q_d=0$) with parameters: $t_{ox}=2nm$, $x_t=0.05 \cdot t_{ox}$, $\sigma_0=10^{-18}/cm^2$, $E_g=0$.

Furthermore, in strong inversion we can consider $Q_i = C_{ox}(V_g - V_t)$, so Eqs. (18) becomes:

$$\bar{\tau}_c = \frac{q}{\sigma \cdot f_e \cdot C_{ox}(V_g - V_t)} \quad (a) \quad \text{and} \quad \bar{\tau}_e = \frac{q \cdot e^{\frac{x_t \cdot (V_g - V_t)}{kT \cdot t_{ox}}}}{\sigma \cdot f_e \cdot C_{ox}(V_{g,trap} - V_t)} \quad (b) \quad (19)$$

where $V_{g,trap}$ is the gate voltage bias for which $E_t = E_f$. Thus, it can be simply shown from Eq. (17)(b) that $d(\ln(\tau_e))/dV_g \approx qx_t/(t_{ox}kT)$ in strong inversion, giving access to the trap depth. Similarly, one has $d(\ln(\tau_c/\tau_e))/dV_g \approx qy_t/(LkT)$ in weak inversion, providing a way to estimate the trap position from source along the channel [50].

It should be also mentioned that more sophisticated capture and emission time models have been proposed for a better description of the trapping-detrapping dynamics using multi-state defects with multiphonon theory (see [51]).

Finally, it is worth recalling that the drain current power spectral density of a two-level RTN follows a Lorentzian spectrum given by [52]:

$$S_{Id} = 4.A.\Delta I_d^2 \frac{\tau}{1 + \omega^2 \tau^2} \quad (20)$$

where $\tau = (1/\tau_c + 1/\tau_e)^{-1}$ is the effective time constant, $A = \tau/(\tau_c + \tau_e) = f_t(1 - f_t)$ is the space mark ratio, $\omega = 2\pi f$ is the angular frequency and f_t is the trap occupancy factor, $f_t = 1/\{1 + \exp[(E_t - E_f)/kT]\}$.

The RTN phenomenon in MOSFETs and the various characterization methods are discussed in more detail in Chapters 4 [53], 7 [54], 14 [55] and 18 [56] of this book.

2.2. Noise model development and challenges

a. Multi-interface CNF approach

In multi-gate devices, trapping and de-trapping of carriers can occur at multiple channel/oxide interfaces. Therefore, if one applied the CNF model as described in 2.1 for this case, the normalized flicker drain current noise would be expressed as:

$$\frac{S_{Id}}{I_d^2 (multi-gate)} = \sum_{i=1}^n S_{Vfb_i} \left(\frac{g_{mi}}{I_d} \right)^2 \quad (21)$$

where the subscript i refers to each interface, n is the total number of interfaces, and S_{Vfb} is defined by (5). In SOI devices, there are only two flicker noise sources: the interfaces between silicon / front gate oxide (t_{ox}) and silicon / buried oxide (t_{BOX}), thus for SOI can be expressed as:

$$\frac{S_{Id}}{I_d^2 (SOI)} = S_{Vfb1} \left(\frac{g_{m1}}{I_d} \right)^2 + S_{Vfb2} \left(\frac{g_{m2}}{I_d} \right)^2 \quad (22)$$

where subscripts 1 and 2 refer to the top and back interface, respectively. It follows that $g_{m1} = dl_d/dV_{G1}$ and $g_{m2} = dl_d/dV_{G2}$ are the respective front and back gate transconductance. Then, taking into account that only the oxide capacitance and trap densities differ between S_{Vfb1} and S_{Vfb2} , the front input referred noise $S_{VG1} = S_{Id}/g_{m1}^2$ can be expressed through:

$$S_{Vg1(SOI)} = S_{Vfb1} \left[1 + C_{21}^2 \frac{N_{t2}}{N_{t1}} \left(\frac{C_{ox1}}{C_{ox2}} \right)^2 \right] \quad (23)$$

where $C_{21} = g_{m2}/g_{m1}$. If the two oxides are made from the same dielectric material and with the same process, then the approximation $N_{t1} = N_{t2}$ can be considered. However, the high-k dielectric used in the front gate to reduce the leakage current degrades the interface quality compared to buried thermal oxide, resulting in N_{t1} values typically one decade higher than N_{t2} [17]. Nevertheless, from (23), it becomes clear that the defining factor for the coupling effect between the two noise sources is the product $(C_{21})^2 \times (N_{t2}/N_{t1}) \times (C_{ox1}/C_{ox2})^2$, revealing that the contribution of the back interface to the total drain current noise is not just depending on the back/front trap density ratio, but also on the

back/front transconductance and oxide thickness ratios. From (23) we also conclude that in strong inversion, where $g_{m1} \approx g_{m2}$ [57], the front/back noise coupling only depends on the quality ratio of the two interfaces (N_{t2}/N_{t1}) and the ratio between the buried oxide and channel thicknesses.

To illustrate these effects, we run a series of TCAD simulations in FlexPDE (a fast and reliable partial differential equations solver), for FD-SOI MOSFETs with $t_{Si} = 7$ nm, $t_{ox1} = 1.5$ nm and $t_{ox2} = 25$ nm. Some results are shown in Figure 5, where we varied the trap density ratio and in Figure 6, where the simulations were repeated for different back-gate voltage V_{G2} . As can be seen in Figure 5, when the volumetric trap density values N_{t1} and N_{t2} are close to each other, both noise sources -front and bottom- contribute to the total noise level, while if one oxide has a much worse interface quality, its noise becomes dominant. This makes it very difficult to extract N_{t1} and N_{t2} from a single set of measurements in a reliable way. However, as shown in Figure 6, the noise intensity of the bottom interface can be controlled by V_{G2} , resulting in a different total noise level for each back-bias value. Thus, one can extract the characteristic parameter values of each interface combining simultaneously noise measurement data at various bias conditions: front-gate mode, back-gate mode, back-accumulation mode, constant current etc. [11], [58].

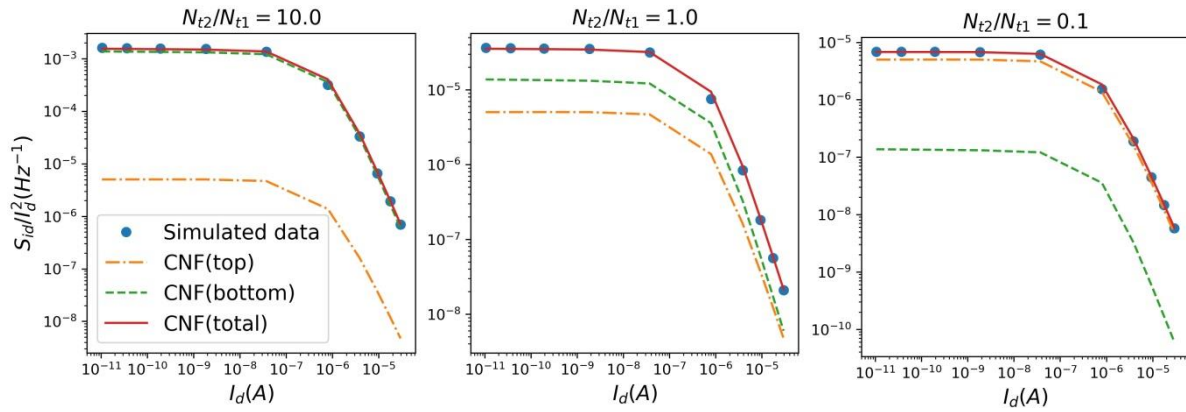


Figure 5. TCAD simulations results of normalized noise for different trap density ratio between top and bottom interface. The dashed lines correspond to the two terms of the model expressed in (22) and the continuous line to their sum.

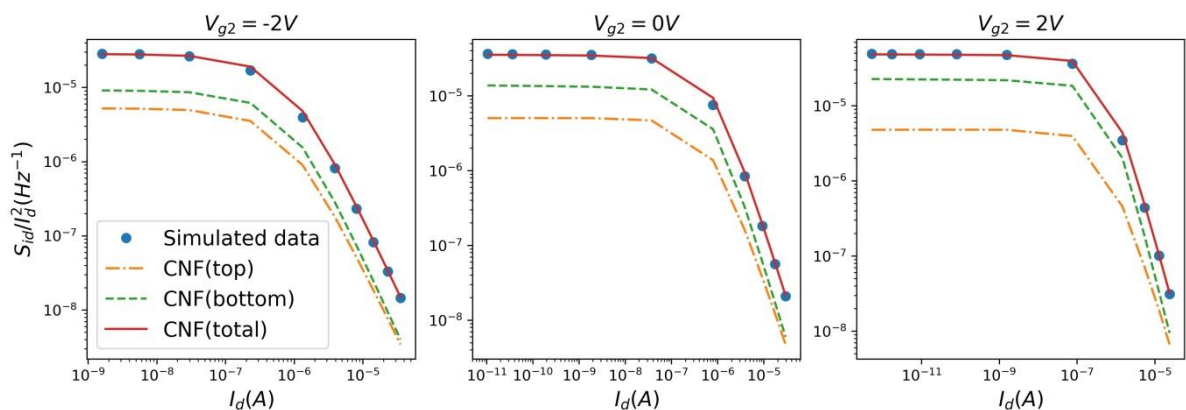


Figure 6. TCAD simulations results of normalized drain current noise for different back gate voltage values

b. Two-interface CNF/CMF modeling

Now, if we also take into account the contribution from remote Coulomb scattering, we can add the CMF terms in (22) and obtain:

$$\frac{S_{Id}}{I_d^2 (SOI)} = S_{Vfb1} \left(\frac{g_{m1}}{I_d} \right)^2 \left(1 + \Omega_1 \frac{I_d}{g_{m1}} \right)^2 + S_{Vfb2} \left(\frac{g_{m2}}{I_d} \right)^2 \left(1 + \Omega_2 \frac{I_d}{g_{m2}} \right)^2 \quad (24)$$

or, expressed as input-referred gate voltage power spectral density [57]:

$$S_{Vg1(SOI)} = S_{Vfb1} \left[\left(1 + \Omega_1 \frac{I_d}{g_{m1}} \right)^2 + C_{21}^2 \frac{N_{t2}}{N_{t1}} \left(\frac{C_{ox1}}{C_{ox2}} \right)^2 \left(1 + \Omega_2 \frac{I_d}{g_{m2}} \right)^2 \right] \quad (25)$$

It becomes clear from (25) that the last parameters determining the total drain current noise are the CMF factors $\Omega_1 = \alpha_{sc1} \mu_{eff} C_{ox1}$ and $\Omega_2 = \alpha_{sc2} \mu_{eff} C_{ox2}$. Regarding these two factors, a relation between them can be found using the dependence of α_{sc} on the carriers' position. According to [59] (Chapter 3), α_{sc} depends on the distance x between the inversion charge centroid and the interface through:

$$\alpha_{sc} = \frac{\alpha_0}{\left(1 + \frac{x}{\lambda_c} \right)^2} \quad (26)$$

where $\alpha_0 = 10^5$ Vs/C approximately in ultra-thin body SOI devices [17] and $\lambda_c = 1.2$ nm. As obtained by the numerical simulations shown in Figure 7 (after [17]) for a constant drain current, the strong dependence of the charge centroid / interface distance on the back-bias voltage V_{G2} results in a significant increase of the RCS coefficient α_{sc} -through (26)- for negative values of V_{G2} . This occurs because as the bottom interface goes towards accumulation region, for the same total charge, the centroid moves much closer to the front interface.

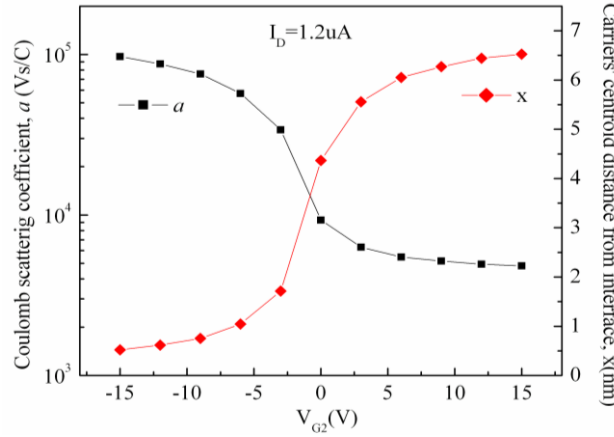


Figure 7. Calculation results for carriers distribution centroid-front interface distance x and coulomb scattering coefficient α versus bias voltage V_{G2} , keeping the drain current constant [17].

Considering a distance x from the front interface and $t_{Si} - x$ from the back interface, an expression for the ratio Ω_1/Ω_2 can be derived as [57]:

$$\frac{\Omega_1}{\Omega_2} = \frac{\frac{C_{ox1}}{\left(1 + \frac{x}{\lambda_c} \right)^2}}{\frac{C_{ox2}}{\left(1 + \frac{t_{Si} - x}{\lambda_c} \right)^2}} = \frac{\left(1 + \frac{t_{Si} - x}{\lambda_c} \right)^2}{\left(1 + \frac{x}{\lambda_c} \right)^2} \frac{t_{ox2} \epsilon_{ox}}{\epsilon_{ox} t_{ox1}} = \left(\frac{\lambda_c + t_{Si} - x}{\lambda_c + x} \right)^2 \frac{t_{ox2}}{t_{ox1}} \quad (27)$$

Figure 8 (after [1]) shows a calculation example of (27) for devices with $t_{Si} = 8.7$ nm, $t_{ox1} = 1.2$ nm and $t_{ox2} = 10$ nm. This figure gives a rough estimation of Ω_1 and Ω_2 , demonstrating that when the

charge is mainly concentrated near the front interface, then $\Omega_1 \gg \Omega_2$. Thus, Ω_2 can be considered as negligible when the device is biased in front-gate (FG) mode without any back-bias.

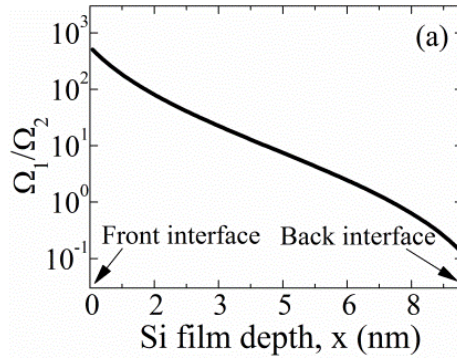


Figure 8. CMF factors ratio Ω_1/Ω_2 versus carriers distance from front interface [57]

Therefore, for the FG mode and $V_{G2} = 0$ V, (25) can be approximated as:

$$S_{Vg1(SOI)} = S_{Vfb1} \left[\left(1 + \Omega_1 \frac{I_d}{g_{m1}} \right)^2 + C_{21}^2 \frac{N_{t2}}{N_{t1}} \left(\frac{C_{ox1}}{C_{ox2}} \right)^2 \right] \quad (28)$$

which, for fully depleted channel (ultra-thin and lightly doped), reduces to the final CNF/CMF model approach for FD-SOI MOSFETs for the FG mode:

$$S_{Vg1(FD-SOI)} = S_{Vfb1} \left[\left(1 + \Omega_1 \frac{I_d}{g_{m1}} \right)^2 + \frac{N_{t2}}{N_{t1}} \left(\frac{1}{1 + C_{ox2}/C_{Si}} \right)^2 \right] \quad (29)$$

Conversely, for back-gate (BG) mode and $V_{G1} = 0$ V, we obtain:

$$S_{Vg2(FD-SOI)} = S_{Vfb2} \left[\left(1 + \Omega_2 \frac{I_d}{g_{m2}} \right)^2 + \frac{N_{t1}}{N_{t2}} \left(\frac{1}{1 + C_{ox1}/C_{Si}} \right)^2 \right] \quad (30)$$

The above equations (29) and (30) can be used to fit experimental data and extract the noise parameters N_{t1} , N_{t2} and Ω_1 and Ω_2 . The need of combining the results from both the FG and BG modes is demonstrated through TCAD simulations that illustrate the carrier concentration distribution in the silicon film channel [57]. As shown in Figure 9(a), while the total charge is exactly the same, one can observe a lack of symmetry in the distribution of the charge, depending on FG or BG operation mode. In FG mode it is almost uniformly distributed across the channel, whereas for BG mode most of the charge is concentrated near the bottom interface. This means that measuring in BG mode we have a better de-coupling, leading to an easier extraction of N_{t2} and Ω_2 , which then can be used in (29) to extract N_{t1} and Ω_1 using the FG mode results. An experimental confirmation of this effect is shown in Figure 9(b) [57], where a reduction of the coupling factor $(t_{ox1}g_{m1}/t_{ox2}g_{m2})^2$ was measured in BG mode, compared to FG mode.

For practical reasons and simplicity of use in SPICE simulation, it is very helpful to transfer all the noise sources to the front gate, including the bottom interface component, as it was implemented in [60]. To this end, one could define the normalized flicker noise using a classic CNF/CMF model equation as in Eq. (2), but with front gate input-referred effective bias-dependent values of $S_{Vfb,eff}$ and Ω_{eff} :

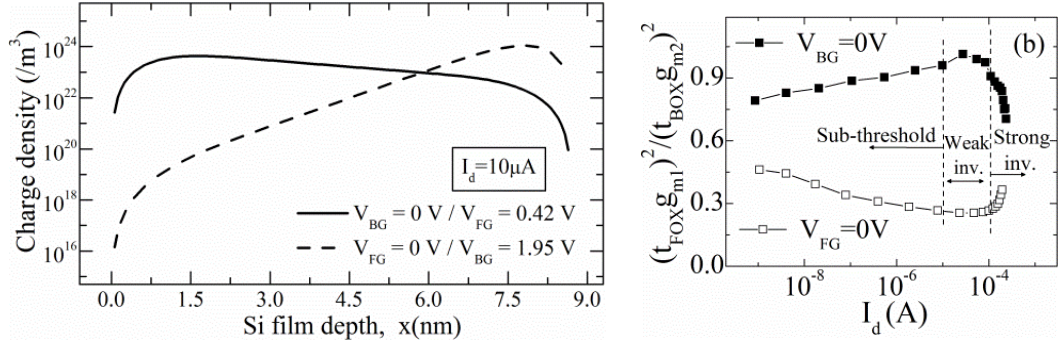


Figure 9. Electron density versus silicon film depth at $V_{BG} = 0$ V (solid line) and $V_{FG} = 0$ V (dotted line) for the same total drain current $I_d = 10 \mu\text{A}$ ($W = 10 \mu\text{m}$, $L = 87 \text{ nm}$). [57]

$$\frac{S_{Id}}{I_d^2} = S_{V_{fb,eff}} \cdot \left(\frac{g_{m1}}{I_d} \right)^2 \cdot (1 + \Omega_{eff} \cdot \frac{I_d}{g_{m1}})^2 \quad (31)$$

$S_{V_{fb,eff}}$ can be obtained from weak inversion region limits where CNF dominates as [60]:

$$S_{V_{fb,eff}} = \frac{q^2 \lambda k T N_{t,eff}}{f W L C_{ox,1}^2} \quad (32)$$

where $N_{t,eff}$ is the effective slow oxide trap volumetric density, related the front and back interface trap densities via the coupling factor as $N_{t,eff} = N_{t1} + C_{21}^2 N_{t2} \Omega_{eff}$ on the other hand can be obtained from strong inversion region limits where CMF prevails as [60]:

$$\Omega_{eff} \approx \sqrt{\left(\Omega_1^2 + \frac{S_{V_{fb2}}}{S_{V_{fb1}}} \Omega_2^2 \right) / \left(1 + C_{21}^2 \cdot \frac{S_{V_{fb2}}}{S_{V_{fb1}}} \right)} \quad (33)$$

where $S_{V_{fb2}}/S_{V_{fb1}} = (t_{ox2}^2 \cdot N_{t2} / t_{ox1}^2 \cdot N_{t1})$ revealing the effect of the front and back gate oxide thickness and volumetric trap density ratio on the total noise level. These equations indicate that the effective parameters $S_{V_{fb,eff}}$ and Ω_{eff} are univocally related to both front and back interface parameters and coupling factor.

The model in (31), combined with (32) and (33), can be easily used to fit drain current flicker noise data from various FD-SOI technology nodes, extract Ω_{eff} and $N_{t,eff}$, and use these parameters to perform accurate circuit noise simulations.

3. Noise characterization in FD-SOI MOSFETs

3.1. Flicker noise in FD-SOI MOSFETs

a. Front/back coupling effects

As explained in Section 2, a very important parameter for the flicker noise analysis is the squared transistor gain $(g_{m1,2}/I_D)^2$. In front gate mode, g_{m1} can be directly measured from the transfer characteristic at constant V_{G2} as $g_{m1} = di_d/dV_{G1}$, whereas a supplementary static measurement under a nearby back-gate bias (i.e. $\Delta V_{G2} = 50$ mV for 10 nm BOX) is needed to extract $g_{m2} = di_d/dV_{G2}$ at each value of V_{FG} . For the back-gate mode, the inverse procedure has to be followed. In Figure 10, $(g_{m1,2}/I_D)^2$ are plotted for various back-bias values as a function of drain current in 28 nm FD-SOI MOSFETs [17]. As usual, $(g_m/I_D)^2$ exhibits a plateau in weak inversion, before dropping above threshold in strong inversion. The top gate gain factor seems to be affected by V_{G2} only for high positive values, where the position of the inversion channel is modified. However, $(g_{m2}/I_D)^2$ depends strongly on V_{G2} , becoming negligible for very negative back-gate bias, where accumulation is achieved.

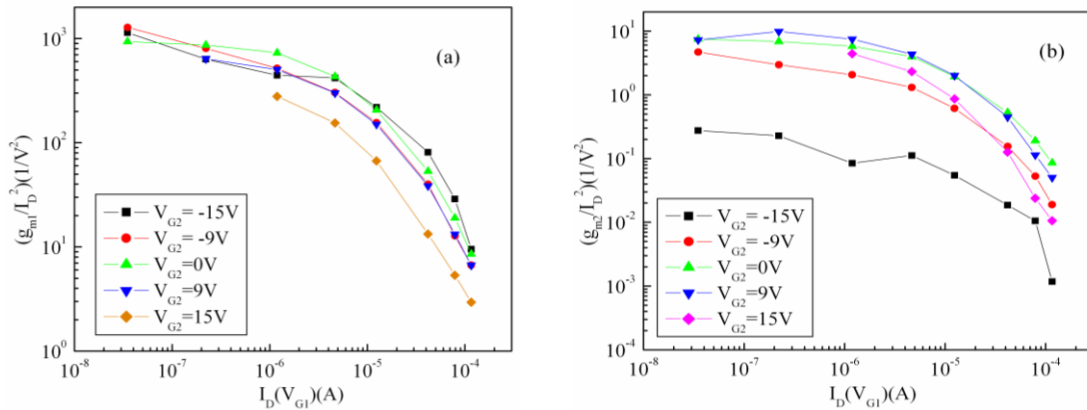


Figure 10. $(g_{m1}/I_D)^2$ (a) and $(g_{m2}/I_D)^2$ (b) versus drain current for various V_{G2} values (after [17]).

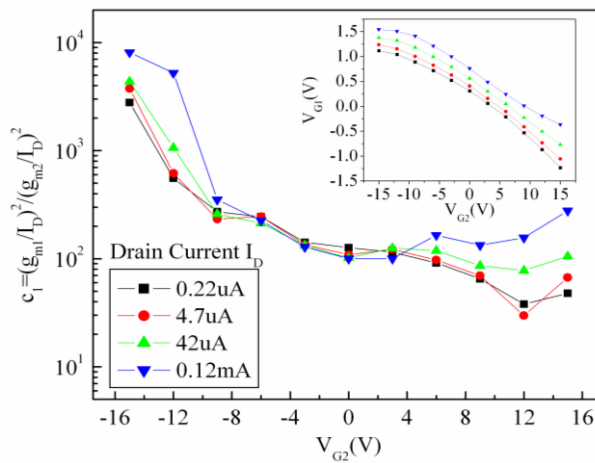


Figure 11. Coupling factor c_1 and V_{G1} dependence on V_{G2} (inset) for various drain current values (after [17]).

The ratio (coupling factor) between the two gain factors is plotted in Figure 11. As can be seen, it lies around ≈ 100 when the bottom interface is in depletion and weak inversion regimes ($V_{G2} > 0$ V), whereas it increases up to almost 10^4 for strong accumulation at the bottom ($V_{G2} \ll 0$ V). This feature indicates that the bottom interface LF noise contribution could be eliminated in the latter situation, allowing for an easier extraction of the front interface noise parameters. One can also notice that c_1 is almost independent of I_D in the depletion and weak inversion region. Nevertheless, when comparing the drain current PSD at different back-bias voltages (Figure 12), we conclude that a high negative V_{G2} value can cause an increase of the flicker noise level, whereas a positive one the opposite.

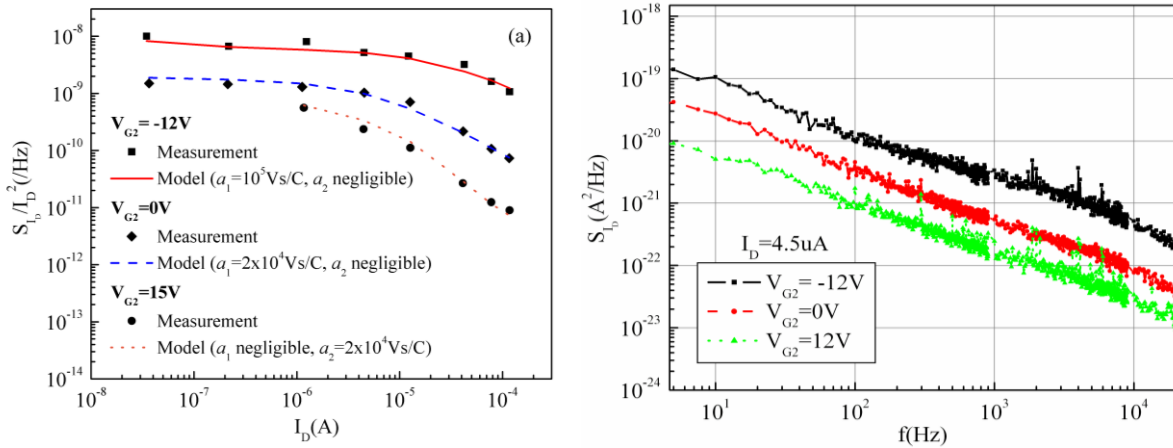


Figure 12. a) Normalized PSD at $f=10$ Hz versus drain current for different V_{G2} values with CNF/CMF model and b) Drain current PSD for $I_D = 4.5 \mu\text{A}$ measured at different V_{G2} (after [17]).

The influence of the back interface coupling effect on the front gate operation LF noise can be better analysed by plotting the normalized drain current noise, measured at a constant drain current, as a function of back gate voltage as shown in Figure 13(a). As can be seen, the normalized drain current noise is significantly higher when V_{G2} takes high negative value. It should also be noted, by comparing Figure 11 and Figure 13(a), that the normalized drain current noise has a similar behaviour with V_{G2} as that of the noise coupling factor c_1 . This type of noise dependence on the back-bias voltage was also confirmed in [61] for the 22 nm FD-SOI node (Figure 13(b)).

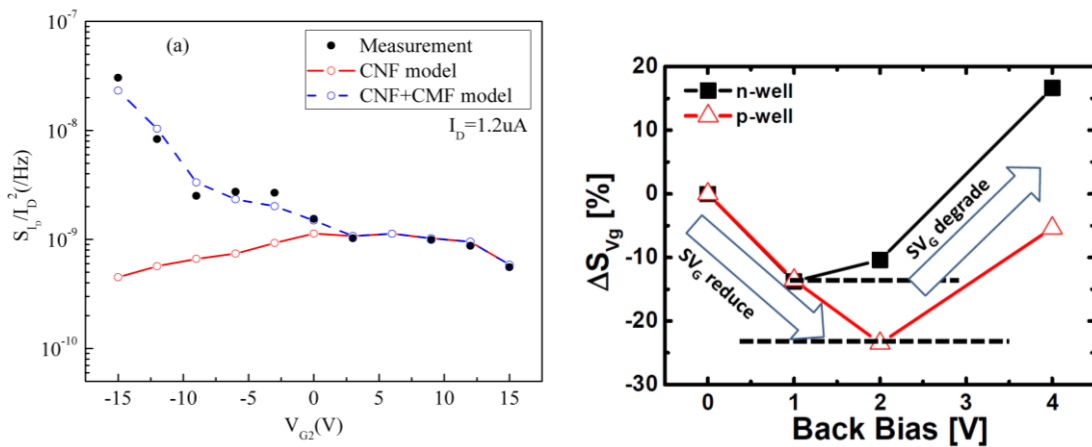


Figure 13. a) Comparison of experimental normalized drain current PSD versus V_{G2} results with the CNF and CNF/CMF model results, for samples from STMicroelectronics (after [17]), b) Percentage change of S_{Vg} median over 30 dies versus back-bias (after [61]).

If only the CNF model of Eq. (22) is taken into account without CMF, this behavior cannot be explained, because neither $(g_{m1}/I_D)^2$ nor $(g_{m2}/I_D)^2$ is increasing for negative V_{G2} . However, the CNF LF noise model applied in the positive V_{G2} range allows us to solve Eq. (22) considering negligible CMF contribution at low drain currents. By combining different bias conditions one can extract constant values for S_{Vfb1} and S_{Vfb2} , from which the front and back gate oxide trap densities can be determined using Eq. (5) ($N_{t1} = 9 \times 10^{17} \text{ cm}^{-3} \text{ eV}^{-1}$ and $N_{t2} = 2 \times 10^{17} \text{ cm}^{-3} \text{ eV}^{-1}$ for the 28 nm FDSOI in [17]). Note that the front interface shows higher oxide trap density as expected due to the high-k/metal gate stack, whereas the back interface trap density is lower due to the higher quality of a pure thermal oxide.

In order to interpret the abnormal LF noise behavior in the negative V_{G2} range, one has to account for the CMF dependence on the carriers position, through the influence of V_{G2} on the remote Coulomb scattering (RCS) parameter α_{sc} , as already explained through Eq. (26) and Figure 7 [17]. Using this RCS formulation and choosing values of α_{sc} that correspond to the dependence shown in Figure 7, the variation of noise with the back gate voltage can be well approached (see fitting lines in Figure 12(a) and Figure 13(a)).

This CMF dependence on back-bias has been also confirmed for 14 nm FDSOI node MOSFETs of STMicroelectronics [60]. As shown in Figure 14(a), it was found that Ω_{eff} (see Eq. (31)) increases for negative back gate bias and tends to very small values for positive ones. This behavior cannot be interpreted using constant RCS coefficients $\alpha_{sc1,2}$ occurring in Eq. (33). Based on the carrier centroid dependence of $\alpha_{sc1,2}$ (see Figure 7), it has been proposed to generalize the CMF coefficients under the symmetric forms [60]:

$$\Omega_1 = \alpha_{sc1} \cdot \mu_{eff} \cdot C_{ox1} \cdot X_{c1} + \alpha_{sc2} \cdot \mu_{eff} \cdot C_{ox2} \cdot (1 - X_{c1}) \quad (34)$$

and

$$\Omega_2 = \alpha_{sc1} \cdot \mu_{eff} \cdot C_{ox1} \cdot X_{c2} + \alpha_{sc2} \cdot \mu_{eff} \cdot C_{ox2} \cdot (1 - X_{c2}) \quad (35)$$

where $X_{c1,2}$ are the normalized carrier centroid positions for the front and back interface, respectively ($X_c=1$ at the front interface and $X_c=0$ at the back interface). Using these expressions in Eq. (33) and extracting the centroid position by solving Poisson's equation with TCAD simulations allows obtaining the simulated trend in Figure 14(a), justifying reasonably well the experimental data behavior.

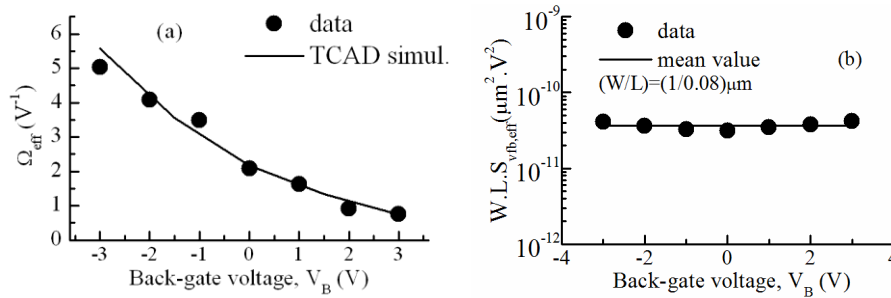


Figure 14. Ω_{eff} (a) and $W.L.S_{Vfb,eff}$ (b) dependence for various back gate biases for n-MOS 14 nm FDSOI node MOSFETs (after [60]).

As already explained in 2.2.b, the combination of front and back gate modes of operation can be very useful for achieving different coupling conditions in order to modify the noise contribution of each interface and help the parameter extraction procedure. Indeed, as shown in Figure 15(a) [58], in the sub-threshold region $(g_{m1}/I_D)^2$ decreases in changing from front-gate ($V_{BG} = 0$ V) to back-gate ($V_{FG} = 0$ V) mode of operation, whereas $(g_{m2}/I_D)^2$ shows a relative increase between FG and BG mode of operation as shown in Figure 15(b). The above behavior is typical for asymmetrical double-gate devices such as UTTB FDSOI MOSFETs [62], related to the different channel position in the silicon film under various bias conditions. A more direct way for an experimental representation of the carrier distribution at different bias conditions is the plot of the coupling factor $C = (g_{m1}/g_{m2})^2$ as a function of the drain current as described in the previous section. The dramatic reduction of C under the back-gate mode of operation (Figure 15 (c)) clearly shows that in that case the carriers have a higher concentration near the Si/BOX interface.

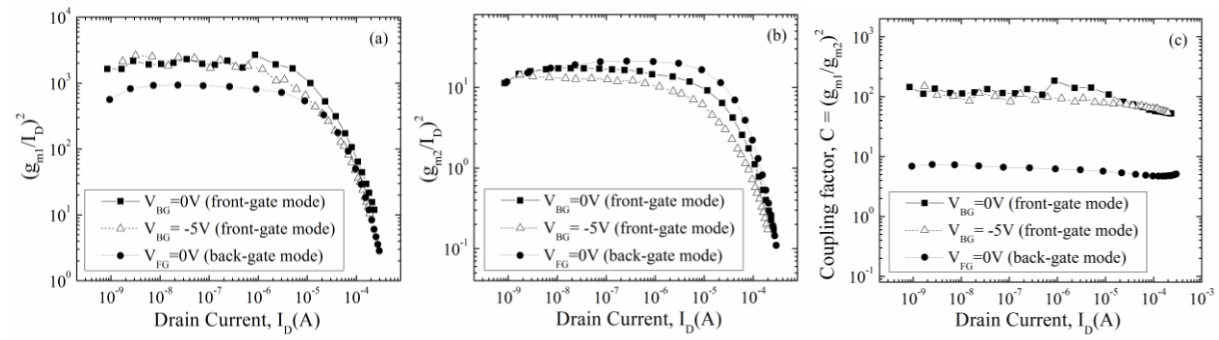


Figure 15. CNF factors $(g_{m1}/I_D)^2$ (a), $(g_{m2}/I_D)^2$ (b) and coupling factor (c) versus drain current for n-MOS transistors issued from 20 nm FDSOI CMOS technology with $W = 10 \mu\text{m}$ and $L = 87 \text{ nm}$, $t_{ox} = 1.2 \text{ nm}$, $t_{si} = 8.7 \text{ nm}$ and $t_{ox2} = 10 \text{ nm}$ (after [58]).

This can be taken advantage of and combine measurements from both front and back gate modes of operation to extract a unique set of parameters that fits all data. An example is shown in Figure 16, where the noise parameters $S_{V_{fb1}}$, $S_{V_{fb2}}$, Ω_1 and Ω_2 were obtained by fitting Eq. (24) simultaneously with all $1/f$ noise data for the front gate mode ($V_{G2} = 0$ V and -5 V) and back gate mode ($V_{G1} = 0$ V). Otherwise, fitting the noise data for a specific bias condition (for example $V_{G2} = 0$ V), may lead to a numerous number of model parameters. The difference between the ‘Measured ($f=10$ Hz)’ and ‘ $1/f$ component’ seen in Figure 16 means that around 10 Hz there is a strong presence of Lorentzian-like noise, which needs to be removed in order to extract the flicker noise contribution (more on that in 3.2).

Furthermore, one can observe the dependence on the bias conditions of the Si/BOX interface contribution to the total noise level. In front-gate mode, there is sufficient de-coupling of the two interfaces in the sub-threshold region, whereas in strong inversion the back interface affects the noise level significantly. In back-gate mode, as expected, there is a strong influence on the noise of both back and front interfaces.

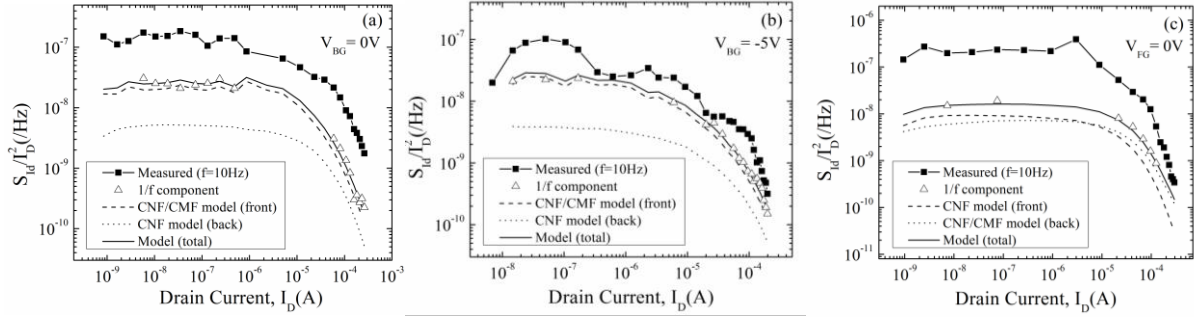


Figure 16. Normalized power spectral densities, flicker noise component values and CNF/CMF model fitting versus drain current for $V_{BG} = 0\text{ V}$ (a), $V_{BG} = -5\text{ V}$ (b) and $V_{FG} = 0\text{ V}$ (c) for n-MOS transistors issued from 20 nm FDSOI CMOS technology with $W = 10\text{ }\mu\text{m}$ and $L = 87\text{ nm}$, $t_{ox} = 1.2\text{ nm}$, $t_{Si} = 8.7\text{ nm}$ and $t_{ox2} = 10\text{ nm}$ (after [58]).

Moreover, the involvement of the correlated mobility fluctuation is also bias dependent. In front-gate mode, the CMF takes place only at the front interface. Respectively, when the back gate bias voltage V_{BG} is varying, the CMF appears only at the back interface. This behavior confirms the analysis regarding the Ω_1 and Ω_2 CMF factors, as already explained in Paragraph 11 through Eq. (27) and Figure 8. The same technique was also used successfully in [57] (see Figure 17), for both n- and p-channel FD-SOI MOSFETs.

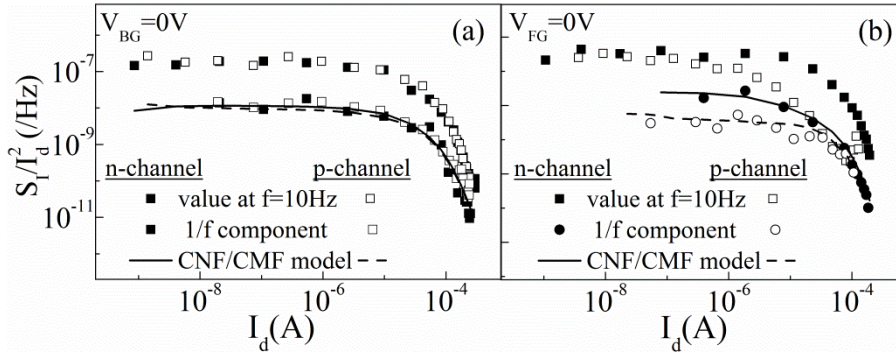
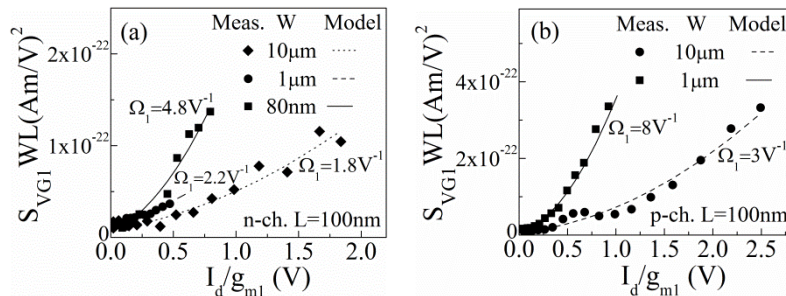


Figure 17. Measured normalized drain current S_d/I_d^2 at $f = 10\text{ Hz}$, extracted $1/f$ component and CNF/CMF model versus drain current for n (solid symbols) and p (open symbols) channel devices at front-gate (a) and back-gate mode (b) with $W = 10\text{ }\mu\text{m}$ and $L = 87\text{ nm}$ (after [57]).

b. Impact of channel geometry on RCS

In Figure 18(a)-(c) [57], the plotted model lines have been derived using (29) as a fitting function. It is clear from Figure 18(a)-(b) that for both 20 nm node n- and p-channel FDSOI devices of constant gate length and varying width, there is a strong dependence of Ω_1 on the gate width W . However, this does not seem to be the case for devices of constant gate width. As shown in Figure 18(c), in devices with constant gate width and different gate lengths, Ω_1 is independent on the gate length.



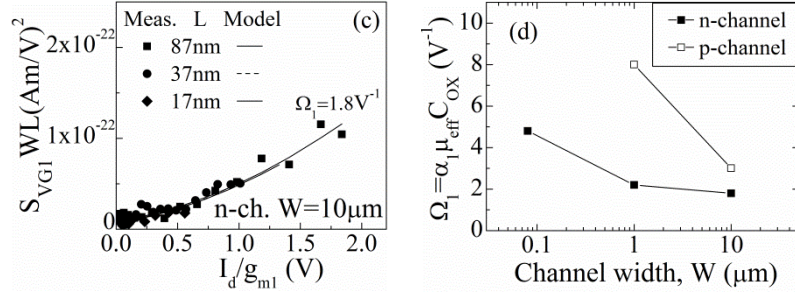


Figure 18. Normalized input-referred noise voltage $S_{VG1}WL$ and noise model fit versus I_d/g_{m1} for n-channel (a, c) and p-channel (b) devices, and extracted values of Ω_1 versus channel width W (d) for transistors issued from 20 nm FDSOI CMOS technology with $t_{\text{ox}} = 1.2$ nm, $t_{\text{si}} = 8.7$ nm and $t_{\text{ox}2} = 10$ nm (after [57]).

This behavior is summarized in Figure 18(d), where the extracted values of Ω_1 are plotted versus the gate width W . It is obvious that for both n- and p-channel devices, the CMF factor Ω_1 is increasing as W decreases. This effect can be attributed to the decrease of the channel cross-section, as W is reduced, which leads to a shorter average distance between carriers and interface. Furthermore, higher values of Ω_1 are clearly observed for the p-channel devices, which are related to the higher values of RCS coefficient α_{sc} observed for holes [22].

This lack of dependence of the CMF on the channel length was not, however, confirmed for the 14 nm FDSOI node MOSFETs of STMicroelectronics, studied in [60]. As shown in Figure 19(a), the Ω_{eff} parameter of Eq. (31) was found to increase in long channel devices. This trend is primarily related to the strong mobility dependence on channel length [63] that also follows a similar tendency, as shown in Figure 19(a). The small deviation can be attributed to the mobility degradation taking place in strong inversion, which was not taken into account. Nevertheless, contrary to the CMF dependence on channel geometry, no such impact was observed for the CNF factors $S_{\text{vfb}1}$ and $S_{\text{vfb}2}$, meaning that the oxide trap density can be considered constant with channel width and length, for both top and bottom interfaces. This is clear in Figure 18(a)-(c), where $S_{VG1}WL$ is constant with W and L in weak inversion, but also in Figure 14(b) and Figure 19(b), where the extracted $S_{\text{vfb,eff}}$, normalized by the surface, is proven to stay constant with W and L , respectively.

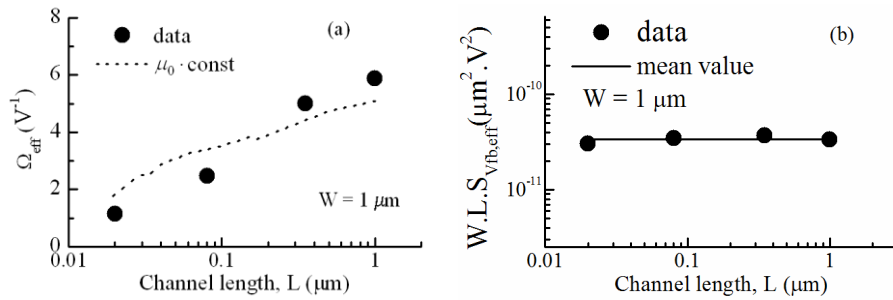


Figure 19. Ω_{eff} (a) and $W.L.S_{\text{vfb,eff}}$ (b) versus device length for n-MOS, respectively, for 14 nm FDSOI MOSFETs (after [60]).

For this effect of L on Ω_{eff} , as well as the impact of V_b (V_{G2}) a unified empirical equation that can fit to all data (as shown in Figure 20) was proposed [60]:

$$\Omega_{\text{eff}}(V_b, L) = \frac{\Omega_0 \cdot e^{-V_b/V_0}}{(1 + L_0/L)} \quad (36)$$

where $\Omega_0 = 6.5 \text{ V}^{-1}$, $V_0 = 3.42 \text{ V}^{-1}$ and $L_0 = 0.12 \mu\text{m}$ are some fitting parameters, with values that were extracted for the 14nm FDSOI technology node devices in [60].

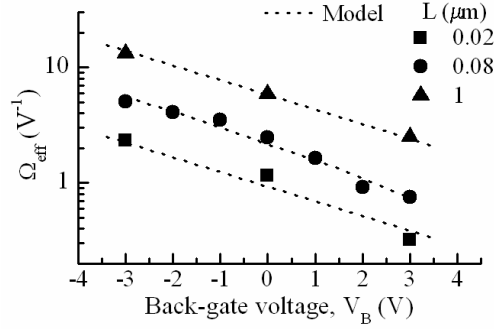


Figure 20. Ω_{eff} dependence on back gate bias for various channel lengths.

In another study [57], a comparative parameter extraction was done for three different FDSOI wafers. Table I presents the characteristic manufacturing details of the wafers, while Table II the extracted noise parameters. As shown, N_{t1} has almost the same value for all wafers, whereas N_{t2} depends slightly on t_{BOX} . In all wafers, the same front oxide high-k metal gate technology is used in terms of materials and thicknesses, explaining the constant N_{t1} values. However, the thickness and the quality of the buried oxide change from wafer to wafer, thus affecting the value of N_{t2} . Moreover, the CMF factor $\Omega_1 = \alpha_{sc1} \mu_{eff} C_{ox}$ was found to decrease with the thickness of the silicon body, due to the increase in the average distance between interface-inversion charge centroid, as explained in 2.2.b.

Wafer number	Technology node (nm)	BOX thickness t_{BOX} (nm)	Si body thickness t_{Si} (nm)	Gate oxide trap density N_{t1} ($\text{cm}^{-3} \text{eV}^{-1}$)	Buried oxide trap density N_{t2} ($\text{cm}^{-3} \text{eV}^{-1}$)	CMF factor Ω_1 (V^{-1})
1	14	10	8.7	8.7×10^{17}	3.5×10^{17}	1.8
2	28	25	6.7	9×10^{17}	2.7×10^{17}	12.2
3	28	145	10	8×10^{17}	8.5×10^{16}	0.8

Table 1. FDSOI wafer characteristics & Extracted Flicker Noise Parameters (after [57]).

3.2. Generation-recombination noise

The physical phenomenon that results in a Lorentzian type of spectrum is the carrier generation-recombination occurring when:

- a free electron and a free hole recombine, or
- a pair of a free electron and a free hole are generated, or
- a free electron is trapped at an empty trap, or
- a free hole is trapped at a filled trap.

The Random Telegraph Noise (explained in 2.1.d) is a case of g-r noise, for which there is only one discrete trap and not a group of defects.

In general, when the noise spectra are composed of $1/f$ and Lorentzian noise components due to several distinct and uncorrelated trap levels, the total current noise power spectral density S_{id} can be written as:

$$S_{I_d} = \frac{K_f}{f} + \sum_{i=1}^N \frac{A_i}{1+(f/f_{ci})^2} \quad (37)$$

where K_f is the amplitude of the flicker noise, A_i is the Lorentzian plateau value and f_{ci} is the corner frequency of each Lorentzian noise spectrum. Such an example can be seen in Figure 21, where F corresponds to K_f , L_i to A_i and $T+B$ to the sum of thermal and background noise.

The origin of the g-r noise can be clarified by determining the dependence of the Lorentzian time constant ($\tau = 1/2\pi f_c$) on the gate bias. When the time constant remains unchanged with gate voltage, the g-r centers are uniformly distributed within the depletion region of the silicon body, whereas when it passes through a maximum, the g-r noise centers are defects located at the interface [64] or inside the oxide region. A recent study has shown that in fully-depleted devices the g-r traps positioned in the Si film can have a misleading time constant behavior, due to its dependence on the carrier concentration above a gate voltage level [65]: the time constant maintains the same value as long as the Fermi level is below the trap energy level and τ starts decreasing with increasing gate voltage when the Fermi level exceeds the trap energy level.

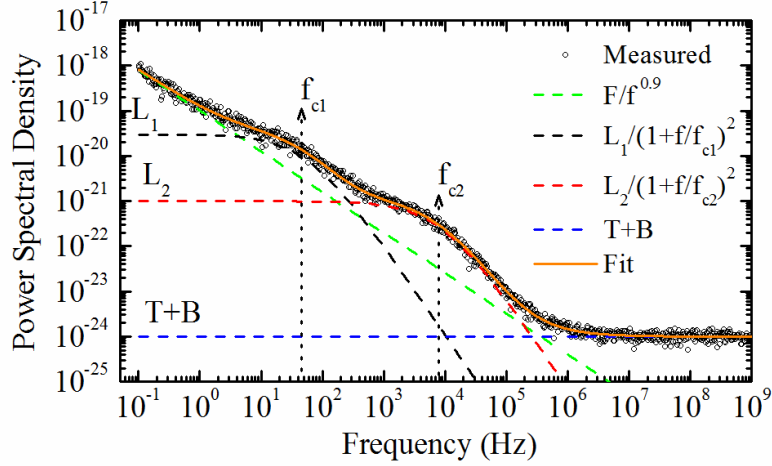


Figure 21. Example of spectrum decomposition for a MOSFET drain current PSD measurement

In Figure 22(a) [58], one can clearly notice that when $V_{BG} = 0$ V, the total noise is composed of a flicker noise and a Lorentzian component. A direct way to ascertain if the g-r component is current dependent is to plot noise spectra, obtained at a constant drain current under different bias conditions, as shown in Figure 22(b). It is evident that the g-r component is mainly dependent on the carriers' position and not on the total channel charge, whereas the flicker noise component seems to change slightly. In addition, from Figure 22(b) one can safely conclude that the specific Lorentzian-type noise is not related to the front gate interface.

After decomposing all spectra into their noise components, the Lorentzian noise parameters (time constants and plateau values) were extracted. In Figure 23 (after [58]) these parameters are plotted as a function of the front and back gate voltages under back and front gate modes of operation, respectively, adjusted to correspond to the same drain current range. One can notice the different trend of the two sets of data. The time constant is not drain current related, but it is defined by the applied bias voltages. This finding leads to the conclusion that the time constant is related to the distribution of the carriers in the channel and not with the total charge.

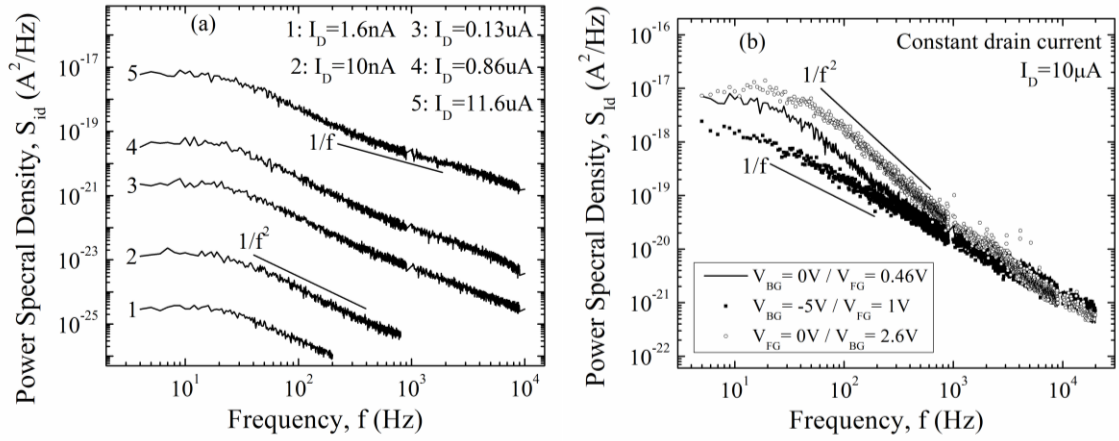


Figure 22. Power spectral density versus frequency for $V_{BG} = 0$ V (a) and for different bias voltages for a constant drain current $I_D = 10$ μ A (b) (after [58]).

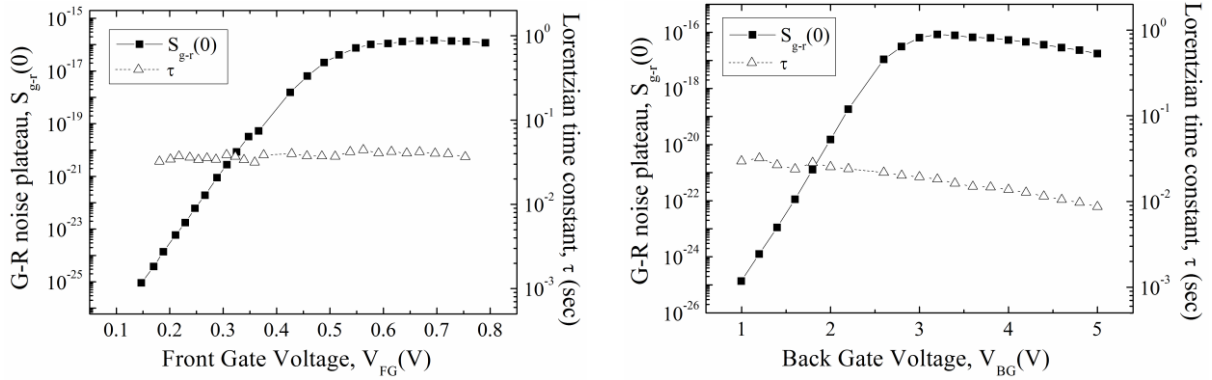


Figure 23. Extracted values of the Lorentzian plateau (squares) and time constant (triangles) versus V_{FG} for $V_{BG} = 0$ V (a) and versus V_{BG} for $V_{FG} = 0$ V (b), plotted at the same drain current region (after [58]).

As shown in Figure 23(a), for $V_{BG} = 0$ V there is no voltage dependence of the time constant and the g-r plateau reaches a constant value above threshold. However, in back-gate mode (Figure 23 (b)) and in the voltage range above the maximum value of $S_{g-r}(0)$, the time constant decreases exponentially with increasing V_{BG} . The results of Figure 23 can be explained considering that in FDSOI MOSFETs there is almost no depletion layer in the Si film when the inversion channel is created, as simulations have shown in [11], [65]. If the electron density n_1 (see Eq. (15)(b)) at the position where the Fermi level is coinciding with the trap energy level in the Si film is higher than the density n of carriers all across the channel, the time constant of the g-r noise is dependent only on n_1 [65], thus it remains unchanged as shown in Figure 23(a). When n becomes comparable or larger than n_t the time constant becomes inversely proportional to n , leading to the behavior of Figure 23(b). At low back gate voltages τ is almost constant, but when $S_{g-r}(0)$ reaches a maximum value the Fermi level approaches the trap energy level. After this point, the time constant decreases following the decrease of the g-r noise plateau. This observation leads to the conclusion that these defects are located inside the silicon channel, but near the bottom silicon/buried oxide interface. This explains why τ stays constant with the front gate voltage.

3.3. Noise variability

a. General properties of LFN variability

The reduction of the device area in advanced CMOS technologies, such as the FD-SOI structure, can lead to important issues regarding the device performance variability [66]. As far as the low frequency noise (LFN) is concerned, one of its main properties is the scaling with the reciprocal of the device area [23] (Figure 24), which has become a major concern for both analog and digital circuits operation, such as oscillators, RAM cells, inverters and other mixed signal circuits [49]. Furthermore, the nanoscale-induced uncertainty in number of traps, the random telegraph noise (RTN) presence, common in small-area MOSFETs ($<1\mu\text{m}^2$) [42], as well as generation-recombination (GR) noise centers in the Si film [67] directly lead to enormous levels of LFN variability (Figure 24) that further limit the device performance and reliability and introduce a high inaccuracy in the prediction of circuit noise levels. Thus, a detailed study of the advanced FD-SOI LFN variability is crucial in order to better understand its origin and by turn its prediction and/or reduction.

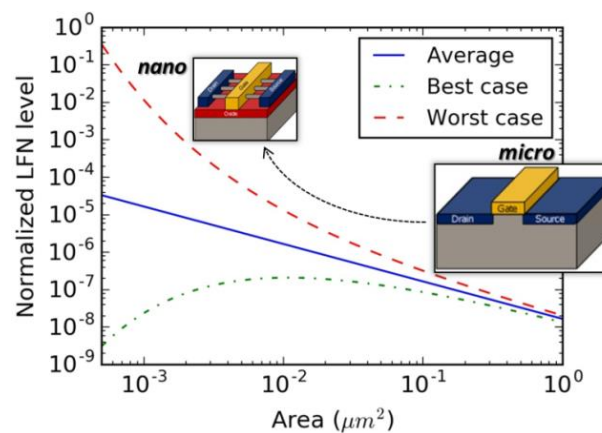


Figure 24. Both LFN level and LFN variability scale reciprocally with the device area.

An example of noise variability experimental results is shown in Figure 25 (after [68]), where S_{V_g} is plotted versus frequency for all measured devices across a 300 mm wafer biased under the same gate voltage bias $V_G = 0.4$ V. Notice that few spectra are $1/f$ -like, but there is also a significant number of Lorentzian-like spectra, commonly observed in such small area ($W.L = 0.0012 \mu\text{m}^2$) devices, due to Random Telegraph Noise (RTN), or due to generation-recombination (GR) centers located in the Si film [65],[69]. From Figure 25 (after [68]), it is clear that the noise variability is strongly enhanced when Lorentzian noise is present.

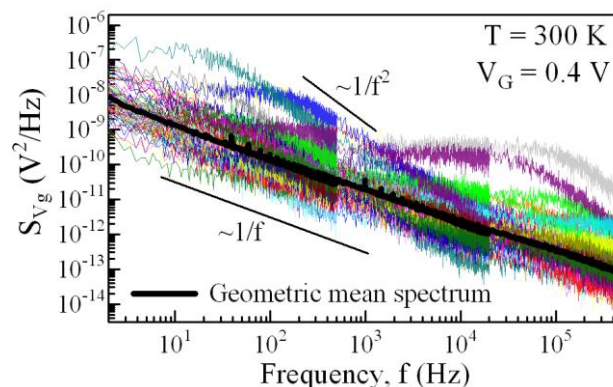


Figure 25. Input-referred gate voltage noise spectra at $V_G = 0.4$ V for 85 dies (colored lines) and geometric mean spectrum (black line) for 14 nm FD-SOI MOSFETs with $L = 20$ nm and $W = 60$ nm (after [68]).

Based on Eqs. (13) and (20), without taking into account the CMF component, this dispersion in the noise spectra can be expressed mathematically through [70],[71]:

$$S_{Vg,i} = \frac{q^2}{(WLC_{ox})^2} \sum_{k=1}^N \left(1 - \frac{x_{t,k}}{t_{ox}}\right) 4A_k \frac{\tau_k}{1 + \omega^2 \tau_k^2} \quad (38)$$

where τ refers to the effective trap time constant, $A=f_t(1-f_t)$ is the space mark ratio, x_t the trap depth and N is the number of traps in the gate oxide within the energy range swept by the Fermi level ($N=W \cdot L \cdot t_{ox} \cdot N_t \cdot \Delta E_f$, N_t being the volumetric oxide trap density and ΔE_f the Fermi level excursion). Therefore, since each device has a different number of traps N (i.e. RTN fluctuators) and each trap its own x_t , τ and A , an induced variability increase is expected as N decreases dramatically, which is the case in nano-scale devices. This effect is further demonstrated in Figure 26 (after [72]), where it is shown that the noise level dispersion is enhanced by 2-3 decades going from the large (Figure 26(a)) to the small (Figure 26(b)) area device. Furthermore, the shape of the spectrum is noticeably changing from $1/f$ to more Lorentzian like behavior, indicating the impact of RTN in LFN variability.

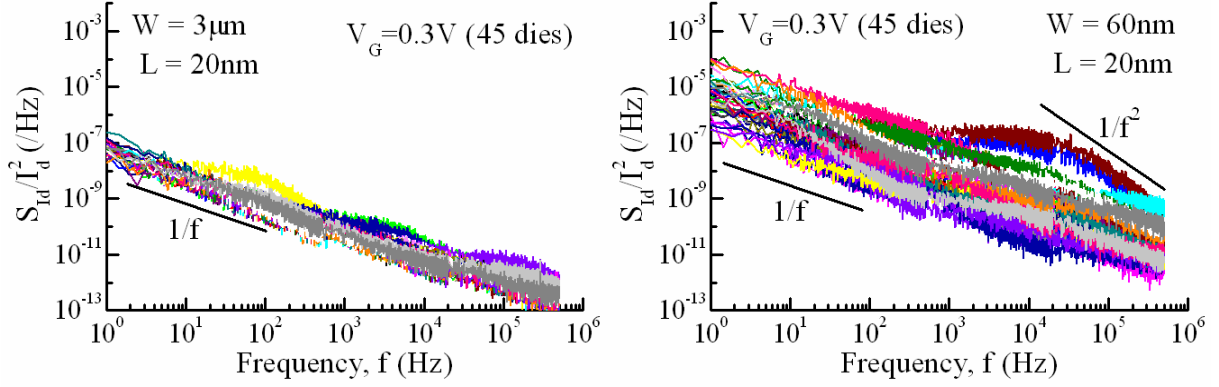


Figure 26. Normalized drain current spectral density S_{Id}/I_d^2 versus frequency for large (left) and small (right) area n -channel 14 nm FDSOI MOSFETs (after [72]).

Furthermore, as already shown in [73]-[74], the drain current noise data of ultra-scaled devices follow a log-normal distribution, thus the geometric mean (or, alternatively, the log-mean) spectrum can better represent the average noise:

$$\langle S \rangle_{geom.} = \sqrt[n]{S_1 S_2 S_3 \cdots S_n} \quad (39)$$

Indeed, as can be seen in Figure 25, the geometric mean spectrum has a clear $1/f$ behavior, that can be used for both interface characterization and noise modeling after the correction given in [73]. Thus, in this section we always consider a geometric mean average in the noise variability analysis.

Finally, in order to quantify the LFN variability effect and be able to make a variability parameter comparison between different technologies, one needs to calculate the standard deviation of the surface-normalized noise at a certain extraction frequency (usually at 10 Hz) [71]:

$$\text{Drain current LFN variability: } \sigma \left(\log \left(WL \frac{S_{Id}}{I_d^2} \right) \right) \quad (40)$$

or, even better, in order to eliminate the influence of the subthreshold swing or threshold voltage variability in the LFN variability estimation, one can use [68]:

$$\text{Input – referred gate voltage LFN variability: } \sigma \left(\log \left(WLS_{V_g} \right) \right) \quad (41)$$

where $S_{V_g} = S_{id} / g_m^2$ is the input-referred gate voltage noise.

b. Variability comparison between different technology nodes

Due to the fact that the trap number variation is a local effect, if the normalized LFN standard deviation (Eq. (40) or (41)) is plotted versus $1/\sqrt{WL}$, a Pelgrom's law [75] trend is observed, from which one can extract a noise matching parameter A. An example is presented in Figure 27 (after [71]), where the slope A seems to be changing, depending on the technology node.

Following this methodology, the noise variability in of the FDSOI technology [76] was found to be improved as compared to advanced bulk technology nodes, as shown in Figure 27 (after [71] and [72]). This was further verified in [72], where the 14nm-node FDSOI technology [76] was found to be improved as compared to both 20 nm Bulk and 28 nm FDSOI nodes, as shown in Figure 28 (after [72]). Interestingly, the noise matching parameter A is following the same trend as the product of the extracted oxide trap density and the squared equivalent oxide thickness, $N_t \times EOT^2$, indicating that the use of a thinner oxide and better quality interface are the main reasons for this noise variability improvement [77].

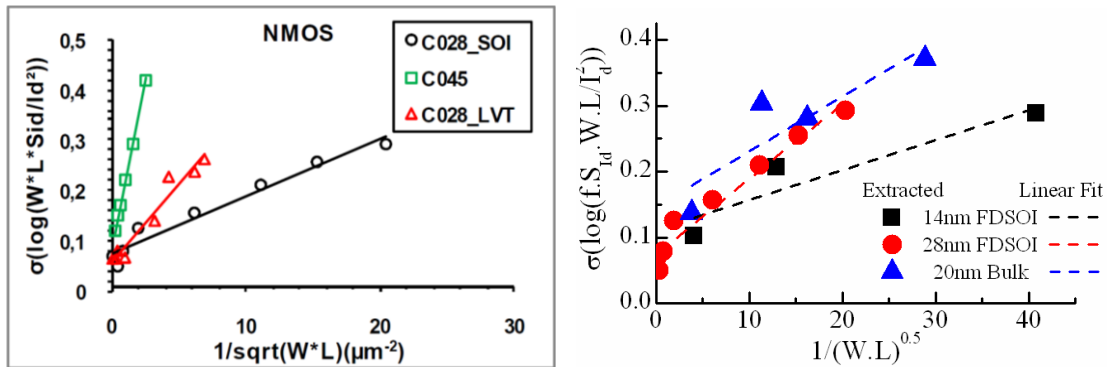


Figure 27. Comparison of the drain current noise variability as a function of the inverse square root of the area between 28nm SOI/Bulk and 45nm Bulk (after [71]) (a) and between 28nm/14nm FDSOI and 20nm bulk technology nodes (after [72]) (b).

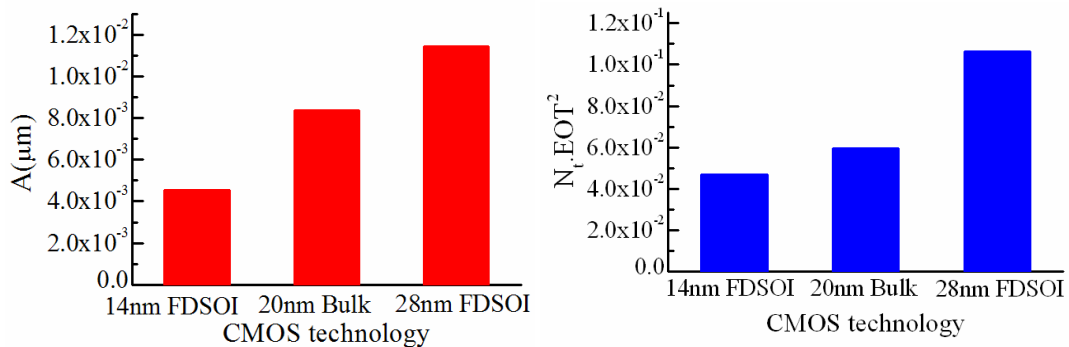


Figure 28. a) Comparison of the drain current noise matching parameter, b) Comparison of the product $N_t \cdot EOT^2$ for n-MOSFETs issued from 28nm & 14nm FDSOI and 20nm bulk technology nodes (after [72]).

c. Statistical LFN/RTN characterization methods

As shown in Figure 26, when going from large to smaller area devices, not only we induce an increase in noise variability, but there is a change in the spectral shape, from 1/f-like to more Lorentzian-like, because the average number of active traps is decreased. Thus, the CNF/CMF flicker noise model, needed for the extraction of N_t , is very difficult to be applied in nano-scale MOSFETs, due to the lack of uniformity in the oxide trap distribution, which results in non-flicker noise spectra. However, if the statistical sample is large enough, the average noise spectrum will be 1/f-like (see Figure 25) [29], [68], making it suitable for extracting the average trap density N_t [72]. Indeed, if we plot the extracted density values at 10 Hz from the spectra of Figure 26 versus the drain current (see Figure 29), the average LFN level follows the CNF model [72]. Therefore, with a sufficient number of measured dies, one can extract the average N_t for all gate oxide areas. An example of such an extraction is shown in Figure 30(a), where an almost constant state-of-the-art volumetric oxide trap density is extracted for both n- and p-channel 14 nm FDSOI MOSFETs for all measured device areas.

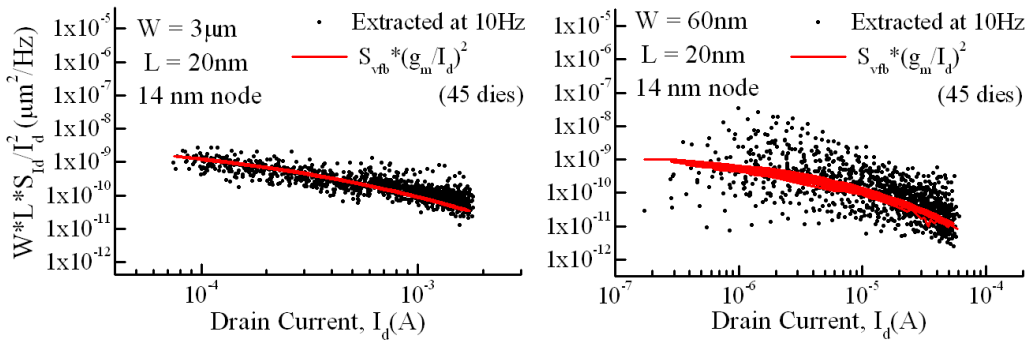


Figure 29. Normalized drain current noise (symbols) and CNF model (lines) at 10Hz for large (left) and small (right) area n-channel 14 nm FDSOI MOSFETs (after [72]).

Besides, Figure 30(b) shows the full wafer mean trap areal density D_{st} and corresponding average absolute number per device, $N_{st} = D_{st} \cdot (WL)$, values, as calculated using Eq. (42). The noise-induced threshold voltage standard deviation can be calculated using the spectra integrals (Eq. (43)). This way, a clear gate voltage dependence is revealed, due to specific trap-induced RTN.

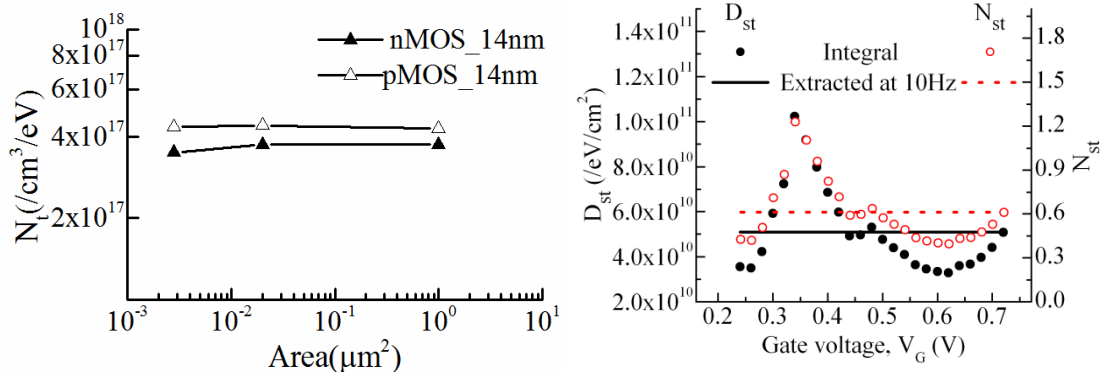


Figure 30. a) N_t versus device area for n- and p- MOS from 14nm technology node and b) Full wafer mean trap areal density D_{st} and average absolute number per device N_{st} ($W=60\text{nm}$, $L=20\text{ nm}$) (after [72]).

$$D_{st} = \frac{W.L.C_{ox}^2 \cdot \sigma_{Vt}^2}{q^2 kT} \quad (42)$$

where

$$\sigma_{Vt} = \sqrt{\int_{f=f_{min}}^{f_{max}} S_{Vg} df} \quad (43)$$

Therefore, following this method, one can obtain a more representative and realistic illustration of the oxide trap density in the full studied frequency range i.e. the whole time constant space, as compared to the standard analysis that extracts the volume trap density N_t from a pure flicker noise spectrum in a restricted frequency range e.g. around 10 Hz.

For certain studies, which want to examine the trap activity and to detect the presence of RTN signals, it is not mandatory to extract the exact parameters (ΔI_d , τ_c , τ_e) of every RTN-inducing trap for the whole wafer and every gate voltage bias, which would be also very time-consuming. Alternatively, in order to probe the RTN impact on the spectrum at each gate voltage and measured die, a new RTN strength indicator is proposed [72]: the standard deviation of $\log(S_{Vg}.f)$ vs frequency, where $S_{Vg} = S_{Id}/g_m^2$. As one can see in Figure 31, when a single RTN source is active, which occurs in a certain bias range, $\log(S_{Vg}.f)$ strongly deviates from the flat line that corresponds to $1/f$ -like noise, giving rise to $\sigma(\log(S_{Vg}.f))$.

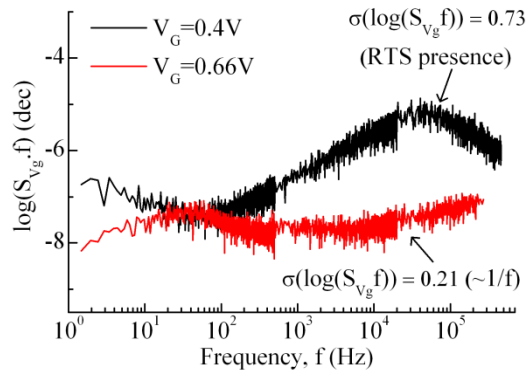


Figure 31. $\log(S_{Vg}.f)$ for $1/f$ -like (red) and Lorentzian-like (black) spectra (n-MOS 14 nm FD-SOI, $W=60\text{nm}$, $L=20\text{ nm}$) (after [72]).

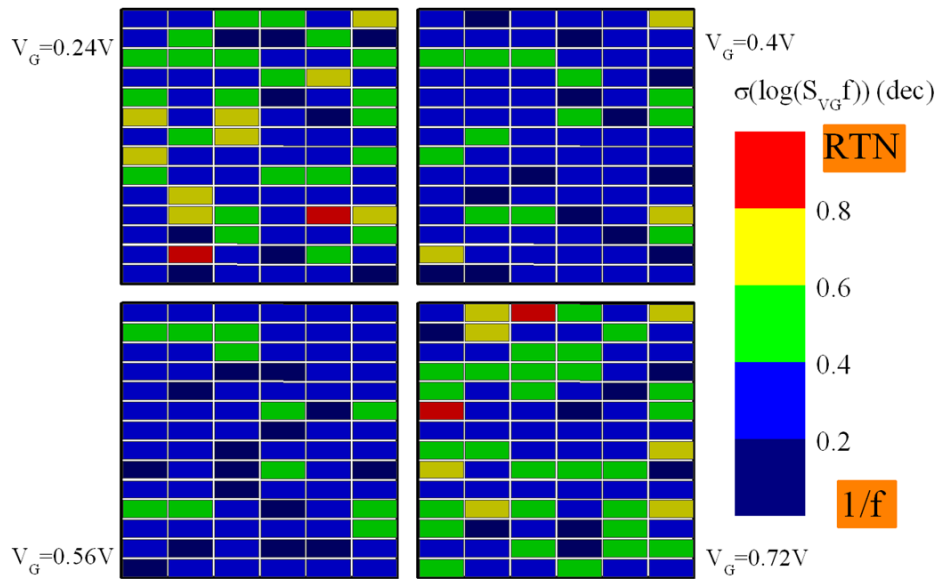


Figure 32. Colored wafer maps based on the values of $\sigma(\log(S_{V_G}, f))$ (dec) for various gate voltage values (*n*-MOS 14nm FD-SOI, $W=60\text{nm}$, $L=20\text{nm}$) (after [72]).

It can be seen from the full wafer cartography of Figure 32 that $\sigma(\log(S_{V_G}, f))$ is bias dependent, due to the RTN trap activity, and randomly distributed over the wafer map, revealing few RTN-dominated dies.

Considering the cumulative distribution function (CDF) for an arbitrarily selected gate voltage, Figure 33(a) shows that the statistical distribution of $\sigma(\log(S_{V_G}, f))$ can be easily modeled by a specific number (in this case 4) of randomly distributed additional RTN fluctuators over 6 frequency decades, superimposed to a $1/f$ background spectrum. Note also that $\sigma(\log(S_{V_G}, f))$ is very sensitive to the number of RTN per decade, demonstrating the RTN statistical probing capability of this quantity. Figure 33(b) shows the full wafer cartography of the mean values of $\sigma(\log(S_{V_G}, f))$ for all gate voltages. It is clear that they exhibit a smoother wafer distribution, meaning that $\sigma(\log(S_{V_G}, f))$ follows well the convergence of many RTN-like spectra to a $1/f$ -spectrum when averaged.

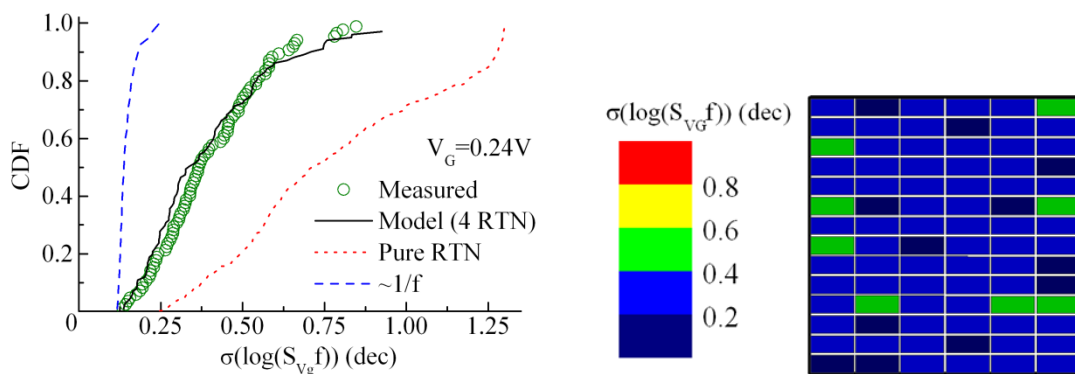


Figure 33. a) CDF of $\sigma(\log(S_{V_G}, f))$ (dec) (measurements and model) and b) Colored wafer maps based on the mean values of $\sigma(\log(S_{V_G}, f))$ (dec) (*n*-MOS 14 nm FD_SOI, $W=60\text{nm}$, $L=20\text{nm}$) (after [72]).

d. Dependence on frequency, gate bias and temperature

In Figure 25, a dispersion of up to 4 decades of magnitude can be observed at high frequencies, while almost 2 decades around $f = 1$ Hz, revealing a possible frequency dependence of the standard deviation. Indeed, as shown in Figure 34(a) (after [68]), where the measured spectra of 85 devices at $V_G = 0.4$ V are plotted along with the noise standard deviation, a clear dependence of LFN variability with frequency is visible. In fact, in the frequency regions where $\sigma(\log(S_{Vg}))$ is increased, there are Lorentzian-like spectra with significantly higher density levels than the remaining spectra. It becomes thus obvious that the dependence of the noise variability on frequency is directly related to the RTN or GR noise presence in many of the devices due to the random distribution of trap energy and trap position in the gate oxide or Si film for each device.

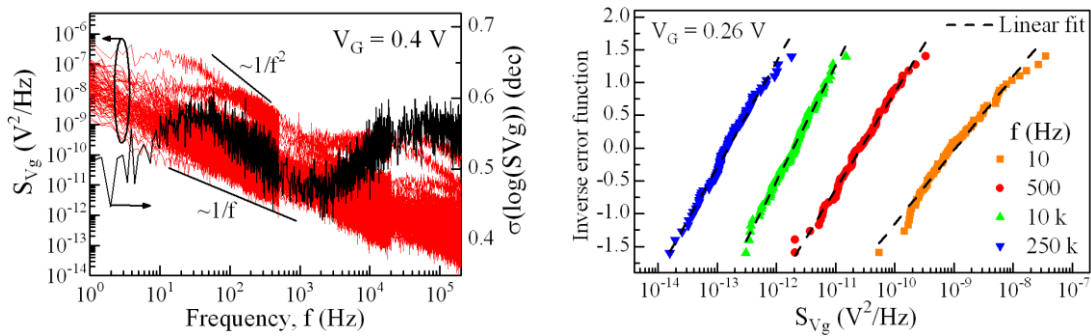


Figure 34. a) Input-referred gate voltage noise (left Y-axis) and standard deviation value (right Y-axis) at $V_G = 0.4$ V versus frequency, and b) Inverse error function versus input-referred gate voltage noise at $V_G = 0.26$ V for 4 different frequencies (after [68]).

A more representative method for validating and analyzing the log-normal distribution is the use of the inverse error function (InvErf) of $(2 \cdot \text{CDF} - 1)$, where CDF is the cumulative distribution function. If the data distribution is indeed log-normal, the $\text{InvErf}(2 \cdot \text{CDF} - 1)$ versus the logarithm of the data should follow a straight line, and the inverse of the slope can provide the standard deviation. So, in order to further demonstrate the frequency dependence of the noise variability, the $\text{InvErf}(2 \cdot \text{CDF} - 1)$ is shown versus S_{Vg} (in log-scale) at $V_G = 0.26$ V for 4 different extraction frequencies in Figure 34(b). The log-normal distribution in all extraction frequencies is evident from the linear fit of $\text{InvErf}(2 \cdot \text{CDF} - 1)$ with S_{Vg} in log-scale. Furthermore, from the difference observed between the linear fit slopes, it seems that at this specific gate voltage bias, the noise variability has its maximum value at low frequencies around 10 Hz, then it decreases with frequency reaching a minimum around 10 kHz, whereas it again increases at high frequencies around 250 kHz. This trend is different than the one shown in Figure 34(a) for $V_G = 0.4$ V, thus the way that the noise variability depends on the frequency changes with the device bias. Following the same data analysis methodology, a variability dependence on gate voltage and temperature was also found [68] (see Figure 35).

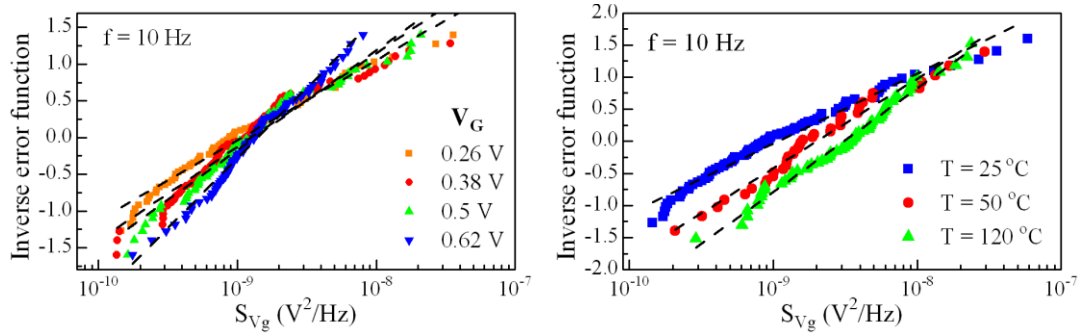


Figure 35. Inverse error function versus input-referred gate voltage noise at $f = 10$ Hz for a) 4 different gate voltage values under $T = 25^\circ\text{C}$ and b) for three different temperatures T under $V_G = 0.26\text{V}$ (after [68]).

To further probe the gate bias dependence of $\sigma(\log(S_{V_g}))$, a more intuitive plot is shown in Figure 36 (after [68]), where $\sigma(\log(S_{V_g}))$ is plotted versus frequency and V_G at the same time. For all bias conditions, a spectral peak of variability at a specific frequency is observed, the position of which is shifted to higher frequencies with increasing V_G . The noise variability dependence on V_G could be explained by the voltage dependence of the trap time constants (see Figure 4), as verified in Figure 37(a).

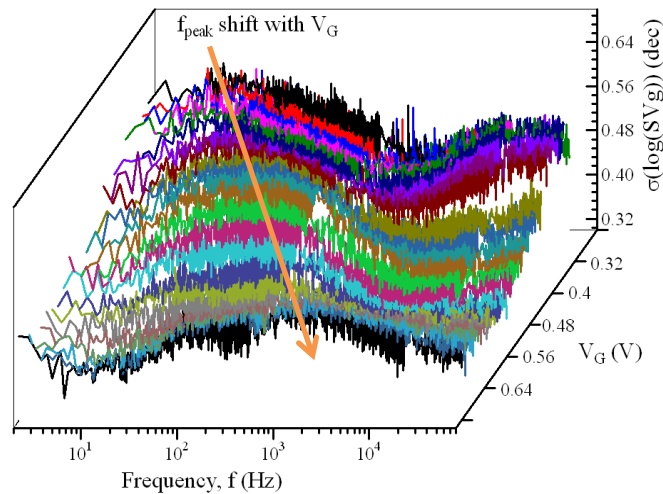


Figure 36. Input-referred gate voltage noise standard deviation versus frequency for all measured gate voltage values (after [68]).

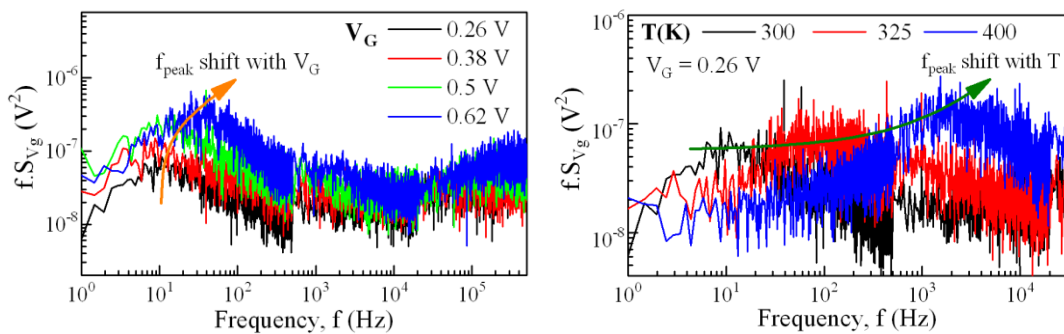


Figure 37. Frequency-normalized input-referred gate voltage noise versus frequency a) for 4 different gate voltage bias (1 die example) at $T = 300\text{K}$ and b) for three different temperatures T (1 die example) under $V_G = 0.26\text{V}$ (after [68]).

A similar time constant dependence is observed in Figure 37(b), where the frequency-normalized noise is plotted versus frequency at $V_G = 0.26$ V and different temperatures. The cut-off frequency of the Lorentzian spectrum corresponds to the maximum value of $f \cdot S_{Vg}$, which evidently increases with increasing the temperature. This behavior is well known in RTN analysis, where the trapping process is thermally activated, resulting in a decrease of the trap time constant with temperature [78]. This translates into an augmentation of the Lorentzian cut-off frequency as the temperature rises, since $f_c = 1/2\pi\tau$. Regarding the impact of temperature on the noise variability, we can relate the behavior shown in Figure 37(b) to the results of Figure 35(b). At $f = 10$ Hz, the noise is dominated by RTN at $T = 300$ K, whereas as the temperature increases the noise becomes more and more $1/f$ -like, resulting in a flat $f \cdot S_{Vg}$ around $f = 10$ Hz for $T = 400$ K. This can explain the reduction of $\sigma(\log(S_{Vg}))$ with increasing temperature at a given frequency for this particular wafer.

4. From noise modeling to circuit simulations

4.1. Noise model implementation

a. Using Verilog-A for noise modeling

Verilog-A [79] is a behavioral description language which is used by Cadence Spectre circuit simulator. It is a very powerful and useful tool, since it provides the potential for full description of a circuit netlist, as well as the behavior of a single device and its interface connections. In this section, two different ways to model a device behavior are presented. When the current-voltage characteristics are described by analytical and compact mathematical equations valid in all regions of operation, these equations can be written in the Verilog-A code and implemented as an analytical model. However, when the device behavior is known only through experimental measurements or TCAD simulations, one has to recall these data so that Spectre can predict all the in-between values through interpolation.

Provided that there is an analytical expression for the drain current as a function of both the gate and drain to source voltages, one can easily include a white or flicker noise source in the Verilog-A code. If the input-referred power spectral density S_{V_g} is constant, as in the case of the $1/f$ noise originating from carrier number fluctuations (CNF), then the device noise can be modeled by incorporating a voltage noise source at the transistor gate. This can be done by the following line of code, using the contributor symbol '<+' which adds a voltage signal on the declared node:

```
V(g) <+ flicker_noise(Svfb, 1, "Svg");
```

where Svfb is the flat-band voltage power spectral density, the number 1 represents the value of the exponent γ and "Svg" is the name of the noise source. This voltage source will result to a drain current noise density equal to $S_{V_g} * g_m^2$.

On the other hand, Verilog-A can also be used for time-dependent modules, since it gives access to the running time value of a transient simulation, as well as control over parameters such as permitted time-step etc. This is very useful for the simulation of RTN, but also LFN (through post-simulation FFT analysis) and BTI (time-dependent degradation) through defect-aware transient simulations, as will be shown in (c).

b. Implementing the two-interface CNF/CMF model

If the values of the drain current or transconductance are needed for the noise expression, as in the case of correlated mobility fluctuations or thermal noise, the transconductance has to be calculated first. If the analytical drain current model provides a simple expression for the I_d - V_g dependence, it is easy to obtain the derivative in the Verilog-A code as below:

```
gm = ddx (Ids, V(g));
```

where gm is the variable name for the transconductance, ddx is the operator used for non-transient derivatives and Ids is the variable name for the drain current. Thus, the improved $1/f$ noise model that takes into account the correlated mobility fluctuations can be described as:

```
V(g) <+ flicker_noise(Svfb*pow((1+alpha*ueff*Cox*Ids/gm),2), 1, "Svg");
```

where α , μ_{eff} and C_{ox} are the variable names of α , μ_{eff} and C_{ox} respectively. Using this method, a voltage noise source is being connected to the transistor gate, as illustrated in Figure 38. As can be seen, both S_{Vg} source and the calculation of g_m regard the interior of the module.

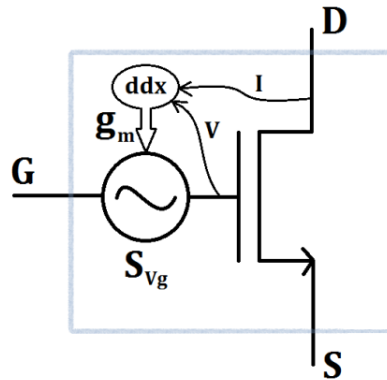


Figure 38. Schematic representation of the Verilog-A CNF/CMF noise model implementation (after [80]).

The FDSOI noise model presented in paragraph 2.2.b of this chapter takes into consideration the contribution of both front and back interfaces to the total noise level. Following the two-interface approach, the gate voltage noise sources can be declared as:

```
V(g) <+ flicker_noise(Svfb1*pow((1+Omega1*Ids/gm1),2), 1, "Sv1");
```

```
V(b) <+ flicker_noise(Svfb2*pow((1+Omega2*Ids/gm2),2), 1, "Sv2");
```

In this way, two noise sources are implemented in the module as illustrated in Figure 39:

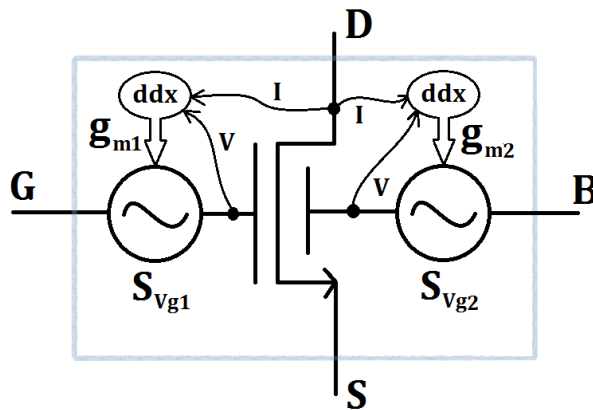


Figure 39. Schematic illustration of the FDSOI Verilog-A noise model implementation (after [80]).

Figure 40 shows a comparison between Spectre simulation and theoretical calculation of the normalized drain current noise S_{I_d}/I_d^2 values at 10 Hz versus drain current. The simulation data accurately follow the trend of the noise model, for both CNF and CNF/CMF cases.

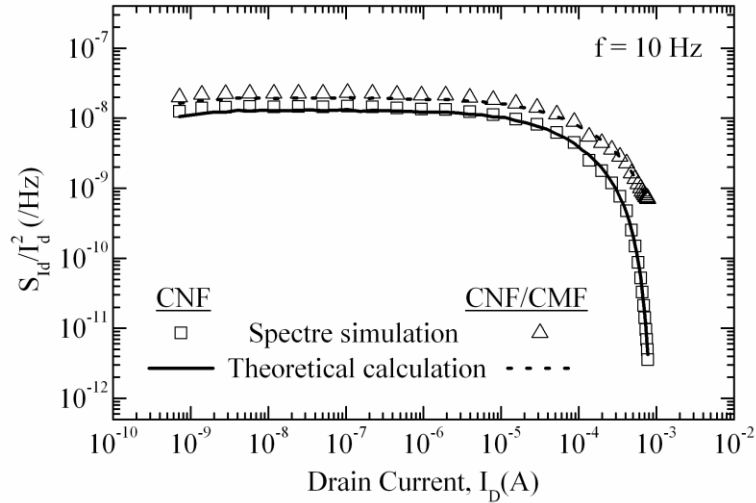


Figure 40. Normalized drain current noise S_{id}/I_d^2 simulated (symbols) and theoretically calculated (lines) values versus drain current for CNF with $N_{t1} = 5 \cdot 10^{17} \text{ cm}^{-3}$ and $N_{t2} = 10^{17} \text{ cm}^{-3}$ and CNF/CMF with $\Omega_1 = 5 \text{ V}^{-1}$ and $\Omega_2 = 0.5 \text{ V}^{-1}$ (after [80]).

The above method is very efficient for circuit simulations in the frequency domain accounting for 1/f noise. A good example of such case is the phase noise, because in frequencies close to the oscillation frequency it is directly proportional to the LFN amplitude [81]. In order to demonstrate the importance of accurate LFN modelling in FDSOI circuits, we took the example of a 3-stage ring oscillator circuit. Figure 41 shows three examples: one case where only the front interface noise is considered ($N_{t2}=0$), one where $N_{t2}=N_{t1}/2$ and finally a case with equally defective front and back oxides ($N_{t2} = N_{t1}$). From the figure becomes clear that if the N_{t2} contribution is not taken into account,

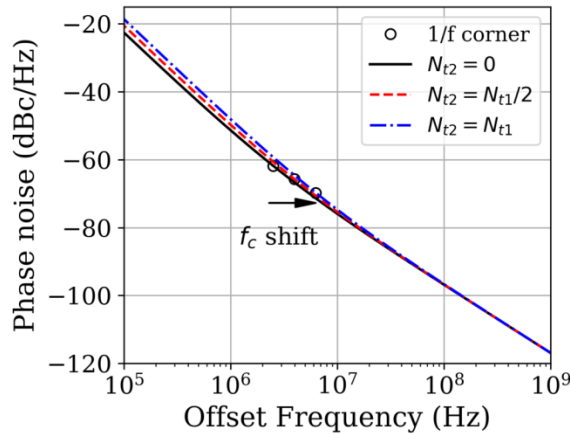


Figure 41. Simulated 3-stage oscillator ($W=10\mu\text{m}$, $L=30\text{nm}$) phase noise versus frequency for three different N_{t2}/N_{t1} ratios, using the model of (9). The flicker/thermal corner frequency points are noted with a circle.

both the phase noise level and the 1/f corner frequency are underestimated by 2-3 times, which may lead to false design decisions.

c. Defect-aware time-domain module

Following the RTN modeling approach described in 2.1.d, one can build a self-contained defect-aware Verilog-A module for time-domain simulations [82],[83]. For the device static response, we can use the model presented in [84], because it is threshold-voltage-based, allowing for a much more straightforward electrostatic trap impact declaration through an approximate relation:

$$\Delta V_t = \frac{q \left(1 - \frac{x_t}{t_{ox}} \right)}{WLC_{ox}} \quad (44)$$

For simplification purposes, the CMF impact on the RTN amplitude was neglected, focusing on the feasibility of the module. The flowcharts for the initialization and the transient processes are shown in Figure 42(a) and (b) respectively, while the module parameters are shown in Table I.

W	gate width	V_{to}	V _t for 0 active traps
L	gate length	Q_{iyt}	surface charge at trap position
t_{ox}	gate oxide EOT	Q_{iyt0}	value of Q _{iyt} when E _T = E _F
N_t	trap density (/cm ³ /eV)	τ_c	capture time
N_{T, Avg}	average # of traps	τ_e	emission time
x_t	trap depth in oxide	t_{up}	time on capture event
y_t	trap position across channel	t_{down}	time on emission event
V_{gtrap}	V _{gt} for which E _T = E _F	state	0 when empty, 1 when occupied

Table 2. Module parameters (after [82]).

As can be seen in Figure 42(a), right before the transient simulation starts, the number of active traps, is chosen from a Poisson distribution with an average value $N_T = WLt_{ox}N_t\Delta E_f$ based on the inputs (W,L,C_{ox} and N_t). In [83], Kaczer et al. approached the $\bar{\tau}_c$ and $\bar{\tau}_e$ estimation picking values for $\bar{\tau}_{e,H}$ (high bias state of a digital circuit) uniformly distributed on the log scale between 10⁻⁹ and 10⁹ and $\bar{\tau}_{e,L}$, $\bar{\tau}_{c,H}$, $\bar{\tau}_{c,L}$ calculated accordingly through different correlation levels. Regarding the intermediate voltages conditions, $\bar{\tau}_c$ and $\bar{\tau}_e$ were interpolated. In our work [82], a random vertical and lateral position is chosen for each trap assuming a uniform distribution in the oxide. Moreover, for the module to be functional under both stationary and non-stationary conditions, $\bar{\tau}_c$ and $\bar{\tau}_e$ are initialized and then re-calculated at every change of voltage bias or temperature (see Figure 42(b)), using Equations (18) and the local inversion charge density Q_{iyt} calculated by the model [84]. This way, this module can be also used for simulating the recoverable part of the Bias Temperature Instabilities (BTI) degradation (as shown in [82]).

A similar Verilog-A based implementation approach is also presented in Chapter 4 [53] of this book.

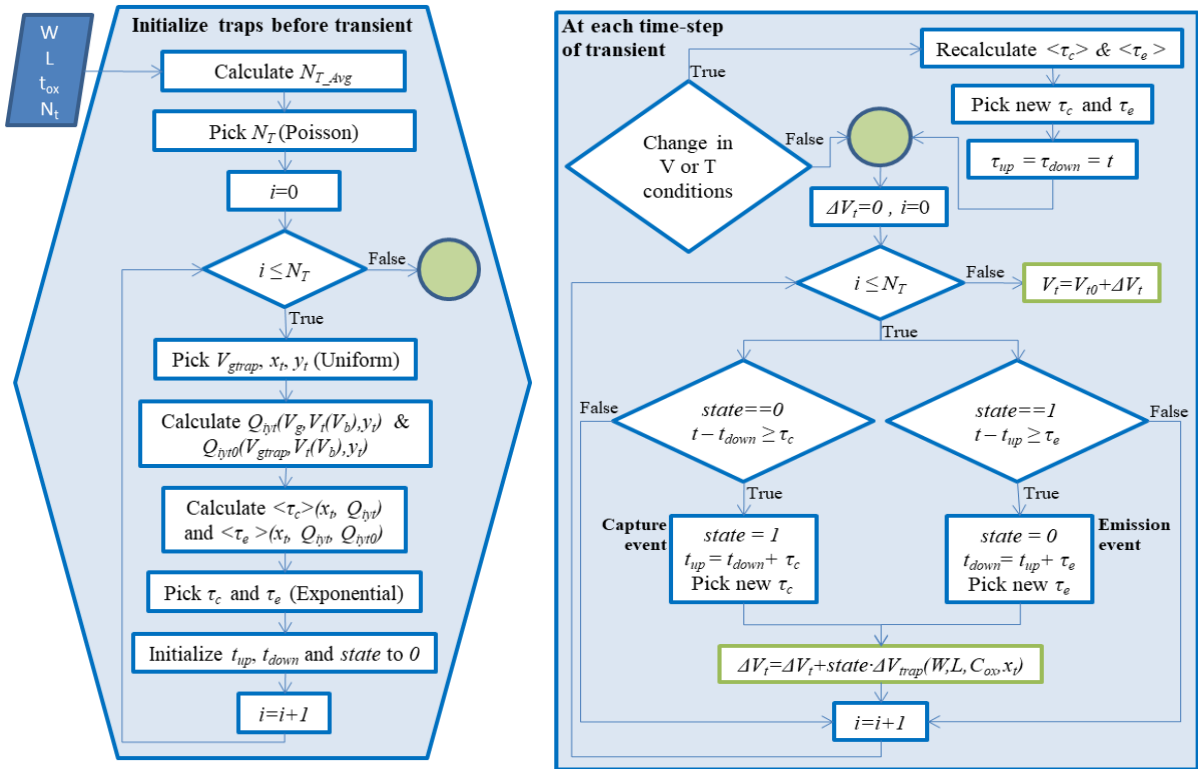


Figure 42. Flowcharts of a) trap initialization process and b) trap activation process during transient simulation (after [82]).

In order to verify that our module can generate an RTN signal with a behavior analogous to the number of active traps N_T , we simulated three different cases (see Figure 43). When only 1 trap is active, we obtain the typical two-level RTN pulse, whereas when $N_T = 2$ it becomes four-level and for $N_T = 10$ the number of levels is 2^{10} , thus becoming indistinguishable. In the frequency domain, these cases translate into one Lorentzian-like LFN spectrum per trap or a $1/f$ -like spectrum for $N_T = 10$, exactly as expected and calculated using the traps input parameters.

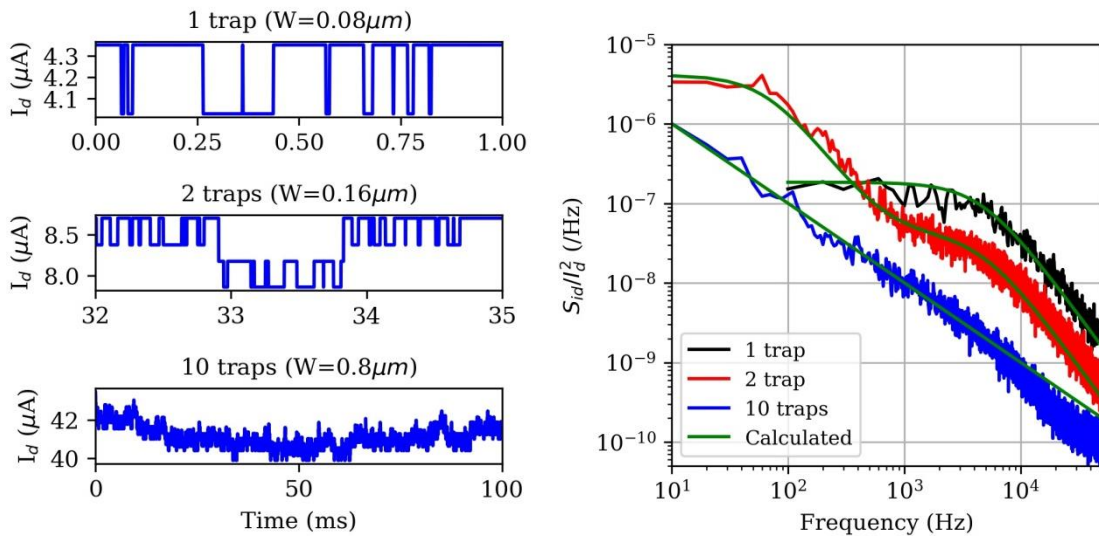


Figure 43. a) Simulated RTN signal examples for $N_T = 1, 2$ and 10 and b) corresponding normalized spectra through FFT (after [82]).

In order to make the use of our module completely generic and current model independent, we have to make it suitable to be used aside already existing PDK device instances. To do so, the simplest way would be to create a sub-circuit instance that contains the PDK transistor, together with a RTN voltage source in series with the transistor gate, as shown in Figure 44(a), in order that $V_g' = V_g + \Delta V_g$, where $\Delta V_g = -\Delta V_{t_RTN}$. However, since the industrial PDK device models usually do not provide access to the inversion charge values, we need to obtain the drain current, I_d , values during a transient so that we can calculate τ_c and τ_e for each trap. If we neglect, for simplicity reasons, the mobility degradation effects, one can express the inversion charge as a function of I_d as following [85]:

$$Q_i(t) = \frac{L}{W} \frac{I_d(t)}{\mu_0 V_d} \quad (a) \quad , \quad Q_{it} = \frac{L}{W} \frac{I_{dt}}{\mu_0 V_d} \quad (b) \quad (45)$$

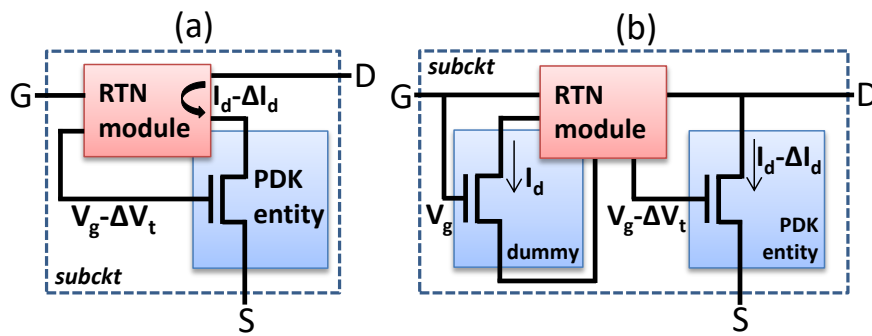


Figure 44. Module implementation methods in existing PDKs: without (a) and with (b) noise-less dummy transistor (after [85]).

There is a serious issue, however, with the above implementation approach: $I_d(t)$ is the device current containing the defect activity through the RTN-induced ΔV_t that by turn causes a ΔI_d shift. Therefore, the capture time calculation during a transient simulation is affected by the trap occupancy itself, creating continuity errors. The solution we proposed in [85] is to utilize an ideal “dummy” transistor with no RTN inside the sub-circuit. Its role is to always provide the theoretical $I_d(t)$ values, when no traps are occupied, in all moments of the transient simulation. This method is illustrated schematically in Figure 44(b). Finally, regarding the energy levels, since we cannot express a charge-voltage relation as done in [82], they can be declared through a characteristic I_{dt} , for which E_t coincides with E_f and calculate Q_{it} through (45)(b), to use it in Eq. (18)(b) for the calculation of τ_e .

4.2. Impact of LFN/RTN on circuit operation

a. Phase noise in FD-SOI ring oscillator circuits

The frequency domain implementation of noise models, such as the one described in paragraph 4.1.b of this chapter, can be very useful when it comes to performing circuit simulations in the frequency domain accounting for $1/f$ noise. A good example for the latter is the phase noise, because the $1/f$ noise is up-converted to phase noise around the oscillation frequency [81]. In order to demonstrate the importance of accounting for both interfaces contributions in FD-SOI circuits, we took the example of a 3-stage ring oscillator circuit (schematic shown in Figure 45). Here we present three cases: one where only the front interface noise is taken into account ($N_{t2}=0$), one where $N_{t2}=N_{t1}/2$ and finally an example where the front and back oxide are equally defective ($N_{t2} = N_{t1}$). One

can clearly observe in Figure 45 that if the bottom interface contribution (N_{t2}) is not taken into account, both the phase noise level and the $1/f$ corner frequency are underestimated by 2-3 times [85]. This might cause wrong noise yield estimations or/and lead to false design decisions.

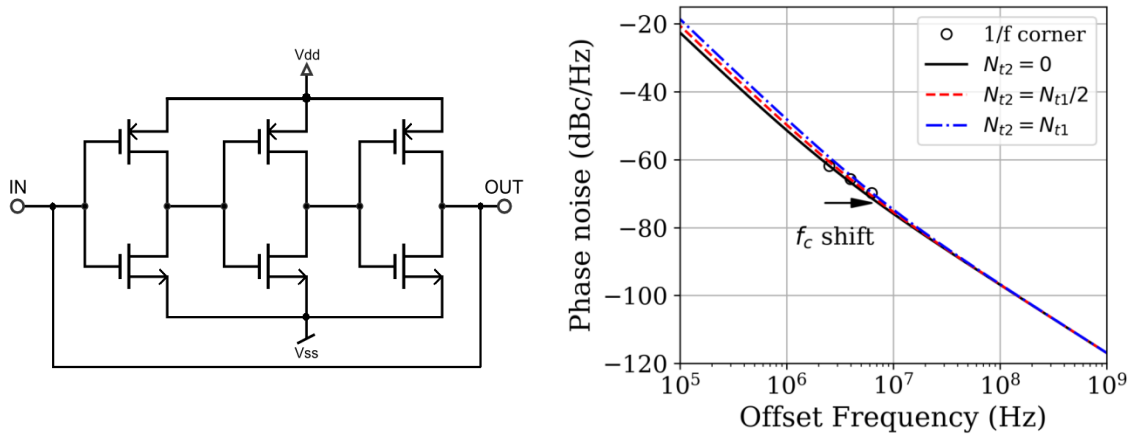


Figure 45. Simulated 3-stage oscillator ($W=10\mu\text{m}$, $L=30\text{nm}$) schematic (left) and phase noise versus frequency for three different N_{t2}/N_{t1} ratios (right) (after [85]), using the model of (9). The flicker/thermal corner frequency points are noted with a circle.

b. The SRAM cell as a circuit reference

In order to examine the impact of LFN or RTN (or both) on a circuit operation, or verify any model approaches, we need a circuit that has wide application, a well-known standard operation and a noise-sensitive dynamic behavior. The typical 6T SRAM cell (Figure 46) has all these characteristics and is very easy to design and simulate. The letters L and R refer to the left and right symmetrical sides, while BL stands for Bit-Line, PG for Pass-Gate, PD for Pull-Down and PU for Pull-Up. The two bit versions (0 and 1) are written using the Write-Line (WL) and stored at the nodes CH and CL.

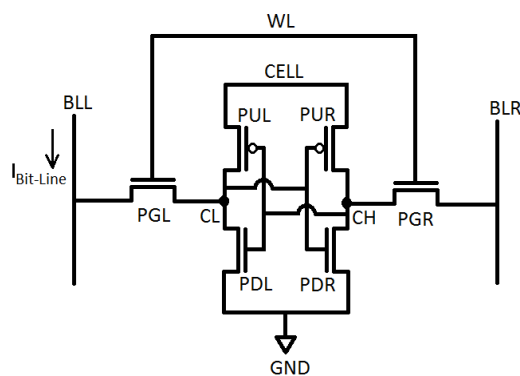


Figure 46. Typical SRAM cell schematic: R stands for Right, L for left, PU for pull-up, PD for pull-down, PG for pass-gate, BL for bit-line and WL for word-line.

The SRAM cell's dynamic limitations can be measured through what we call "stability metrics". Some of the most common SRAM stability metrics are: the Read and Write Static Noise Margin (RSNM & WSNM) and the Supply and Wordline Read Retention Voltage (SRRV & WRRV) [86]. Here, we will focus on the SRRV and RSNM metrics that can provide a representative overview of the SRAM cell dynamic stability.

The SRRV is defined as the maximum allowed reduction of cell supply voltage for which the read stability is not affected. Figure 47(a) and (b) show the time-domain bias setup for properly monitoring the SRRV. During the measurement (or simulation), the word-line (WL) and the right bit-line (BLR) are biased at $V_{WL} = V_{BL(R)} = 1$ V. An initial time is needed for the pre-charge of 0, for example, at the left bit node (CL), and then V_{BL} is constant at 1 V while V_{CELL} is ramped down in order to read the bit-line current I_{BL} . As shown in Figure 47(c), at a certain point the stored bit is flipped and I_{BL} drops suddenly, becoming significantly lower and equal to the Pass-Gate (PG) current. The V_{CELL} value at that point is called V_{flip} and SRRV is extracted as the difference between the power supply V_{DD} and V_{flip} .

The RSNM is an equally important stability metric for SRAM cells [86]. It represents the maximum tolerable DC noise voltage at each storage node before causing a read upset. Regarding its measurement, it requires a more difficult procedure, compared to the simple SRRV measurement setup, because it needs a high-speed voltage monitoring, as well as access to the internal nodes and it has to be performed in two steps. The RSNM simulation, nevertheless, is far more easy to perform than the SRRV and it can be also used to study the SRAM dynamic variability behavior.

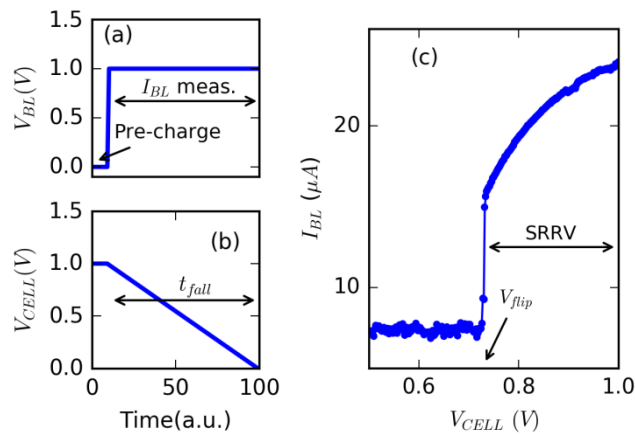


Figure 47. Setup for measuring the Supply Read Retention Voltage: (a) Bit-line voltage and (b) Cell supply voltage versus time. (c) Measured bit-line current versus cell supply voltage (after [87])

Many RTN simulation studies have used these metrics to explore how the RTN amplitude and trap kinetics can affect the SRAM cell stability or even cause read/write errors, arguing this way on the importance of understanding and properly modeling the RTN behavior [49], [88]–[91]. Here, we will present some novel approaches, regarding the aspects of the periodic transient noise and the defect-aware time-domain circuit simulations.

c. “Periodic Transient Noise” approach

Cadence Spectre incorporates a transient simulation option called “Transient Noise” (TN). When activated, this method generates time-domain current fluctuations that correspond to the noise power spectral density that has been declared in the model. Details of this simulation process can be found elsewhere [92], [93]. As a result, when a transient I_d - V_g simulation with a ramp gate voltage as an input is run repeatedly, it produces a set of curves as in Figure 48(a) (after [94]), where we show an example of 100 multiple runs. The disadvantage of this simulation approach is that the noise bandwidth $\Delta f = f_{max} - f_{min}$ taken into account by the TN is limited by the rise time, i.e. the duration of each run, because $f_{min} = 1/t_r$, and by the timestep Δt through $f_{max} = 1 / 2.\Delta t$. This leads to a constant

threshold voltage variation $\sigma_{V_{th}}$ for all rise time values (see Figure 48(b)), because the low-frequency part of the spectrum is not considered.

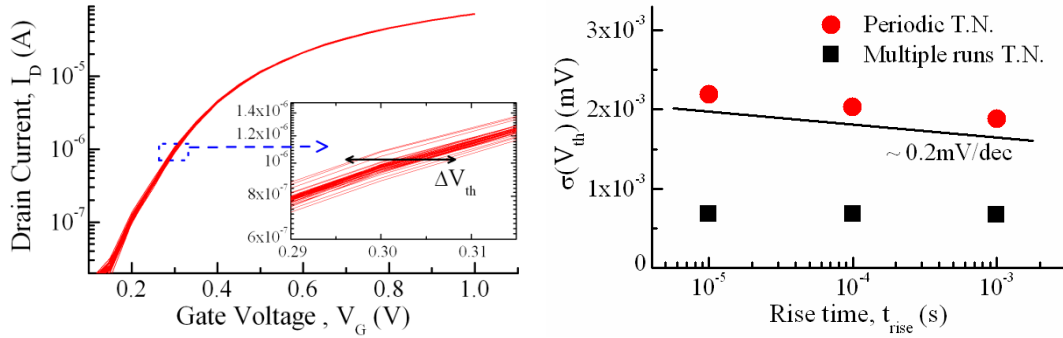


Figure 48. a) Transient noise simulation (100 multiple runs) example . b) Dynamic standard deviation of V_{th} versus rise time for periodic and multiple runs transient noise simulation ($W = 80$ nm, $L = 30$ nm, $S_{Vg}=A/f$ with $A=1.8 \times 10^{-8}$ V^2/Hz) (from [94]).

To resolve this issue, one can use the Periodic Transient Noise (PTN) approach [94], which means running a periodic transient simulation instead of multiple runs, with the TN module activated. This can enlarge the simulation duration and thus increase the noise bandwidth to lower frequencies as much as necessary. This way, the noise-induced threshold voltage variations are both speed- and duration-sensitive, as expressed in 3.3.c through Eq. (43). Also, using the PTN method, the simulation stop time can approach the real duration of operation, obtaining more realistic results.

Using the PTN method, we can easily simulate the noise-induced degradation of the SRRV metric [87] through a series of I_{BL} - V_{CELL} simulations (setup in Figure 47), with the transistors LFN level being controlled by the flat band voltage fluctuations power spectral density $S_{V_{fb}}$ (Eq. (5)) declared in the flicker noise model (4.1.b). A reference simulation with $S_{V_{fb}} = 10^{-8}$ V^2/Hz , stop time $t_{stop} = 10$ ms and cell supply voltage fall time $t_{fall} = 0.1$ ms is shown in Figure 49(a) (after [87]), where a small but not significant noise-induced variability of SRRV can be observed.

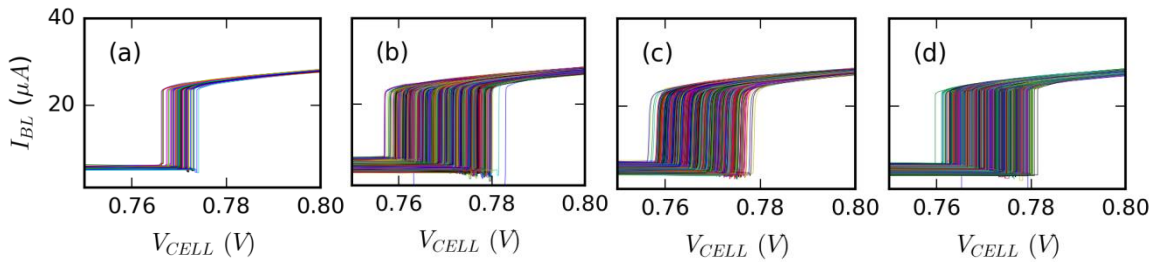


Figure 49. Periodic transient noise simulation results of the bit-line current versus cell supply voltage for four different configurations: (a) Reference simulation, (b) $S_{V_{fb}} \cdot 100$, (c) $t_{fall}/1000$, (d) $t_{stop} \cdot 100$ (after [87]).

In the simulations of Figure 49(b), (c) and (d), one of these three parameters was changed while keeping the rest constant, to examine the impact of each one separately. In Figure 49(b), the noise level was increased to $S_{V_{fb}} = 10^{-6}$ V^2/Hz , in accordance with the worst case LFN level of nano-scale FDSOI MOSFETs [72]. In Figure 49(c) the V_{CELL} fall time was reduced down to $t_{fall} = 1$ μs to increase the speed of operation, and in Figure 49(d) the simulation stop time was increased to $t_{stop} = 1$ s to include the noise contribution from the lower part of the frequency bandwidth. In all three cases, compared to the reference, a significant increase of the SRRV dynamic variability is observed, concluding that the noise-induced FDSOI SRAM dynamic variability is increasing with the transistor LFN level, the

circuit operation speed, and the duration of operation. These results also verify the measured behavior of SRRV shown in Figure 50, further underlining the validity of the PTN simulation method.

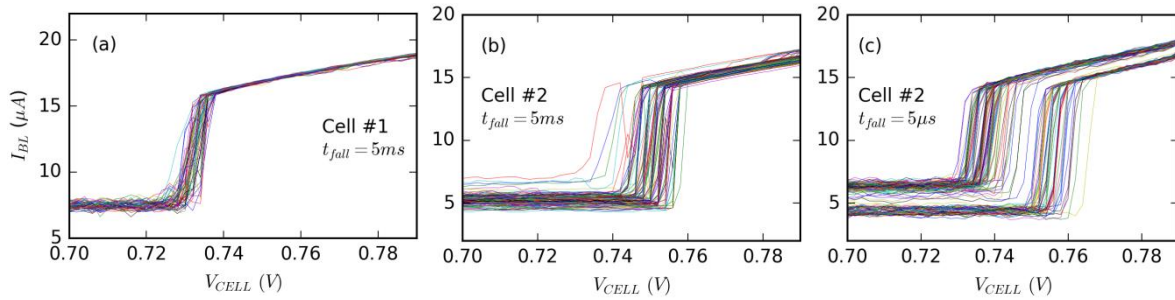


Figure 50. Measured SRAM cell bit-line current versus cell supply voltage for three different cases: (a) Cell #1 with $t_{fall} = 5$ ms, (b) Cell #2 with $t_{fall} = 5$ ms, (c) Cell #2 with $t_{fall} = 5$ μ s (after [87]).

Regarding the PTN simulation of the LFN impact on the RSNM, some representative results are shown in Figure 51 (after [87]). In order to capture both local and time-domain RSNM variations, Figure 51(a) shows local variability results through mismatch-related Monte Carlo simulations. One can notice how the RSNM can be reduced by more than 50% from cell to cell, due to the threshold voltage static mismatch. The noise-induced dynamic variability of a single FDSOI SRAM cell, on the other hand, as shown in Figure 51 (b), can lead to a RSNM reduction of up to 20%. For the latter simulation, the device noise level was boosted by two orders of magnitude ($S_{vfb} = 10^{-6}$ V²/Hz), in order to consider the worst case scenario, which is to have either huge LFN variability or the presence of high amplitude RTN. This alarming finding means that in FDSOI circuits consisting of nano-scale transistors, the LFN/RTN-induced variations can be comparable to the mismatch variations. Considering that these two sources of variations (topological and temporal) will in reality be added together and result to a variability level significantly higher than what is often taken into account in simulations (only process variations), we conclude that the accurate simulation of LFN and RTN becomes more and more important in circuit design.

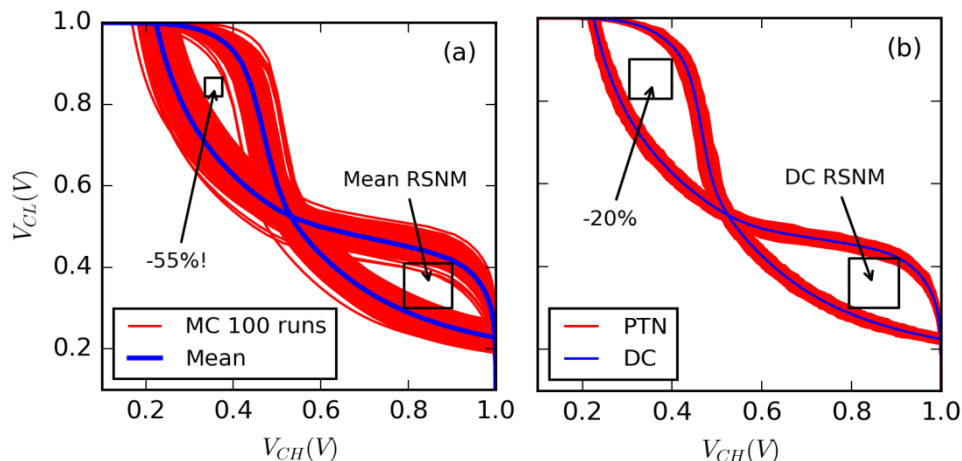


Figure 51. a) Impact of V_t mismatch on RSNM, (MC: Monte Carlo), b) Impact of LFN on RSNM (PTN: Periodic Transient Noise) (after [87]).

d. Defect-aware time-domain simulations

Using the defect-aware module described in 4.1.c, the impact of RTN-TDV on the Read Static to Noise Margin (RSNM) of a SRAM cell was simulated. Figure 52(a) presents the 6T-cell that was used

in our simulations, as well as the number of traps that was chosen by the simulator, considering a uniform trap distribution. The transistor width and length was fixed at $W = 80$ nm and $L = 30$ nm, respectively. In order to simulate the phenomenon, a periodic ramp voltage was applied first on the left node (L) and then on the right one (R), while monitoring the voltage at the opposite node.

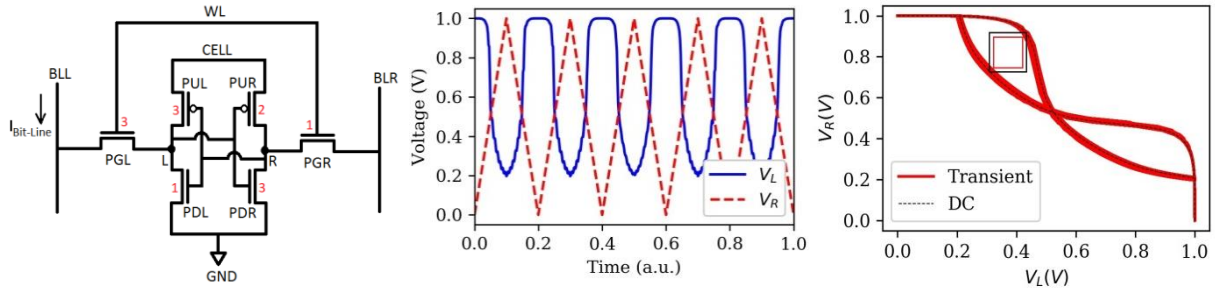


Figure 52. a) SRAM cell circuit used in the simulations. The numbers in red show the total number of traps per device, b) Voltage bias setup during transient simulation with RTN and c) Right-node vs left-node voltage for the extraction of RSNM (after [82]).

A zoomed-in result is shown in Figure 52(b), where one can also note the presence of RTN-related fluctuations in the output voltage. A number of 1000 ramp cycles was chosen, with $t_{\text{rise}} = t_{\text{fall}} = 100$ μs , in order to have a good statistical sample concerning the trap activity.

The final results are shown in Figure 52(c), where V_R is plotted versus V_L for both DC and transient simulations. The impact of the trap activity on the reduction of RSNM is visible: $\text{RSNM} \approx 0.13\text{V}$ in the DC simulation, while it drops at around 0.1 V in the case of the defect-aware transient, revealing a more than 20% reduction of RSNM, only by trapping/de-trapping events in a very low number of traps, in line with the transient noise results presented in (c), where the same reduction was found by using a high level $1/f$ noise spectrum with the Transient Noise module in Spectre.

5. Conclusion

In this chapter, we presented a review of the most important aspects of our research work regarding the low frequency noise behavior of Fully Depleted Silicon-On-Insulator MOSFETs.

First, we found it necessary to give a brief explanation of important terms and concepts regarding the fluctuations mechanisms in MOSFETs, providing some fresh points of view regarding RTN and the Hooge mobility fluctuations. Next, we presented the methodology we followed in order to derive the FDSOI LFN models, which were used on the one hand to extract the noise-related parameters for various FDSOI wafers and on the other hand to perform accurate simulations of noise-induced limitations of a circuit's performance. It was shown that neglecting the impact of the bottom interface on the total noise level or the latter's dependence on back-bias can lead to serious errors in the extraction of trap densities etc.

Regarding the noise characterization of FDSOI MOSFETs, we analyzed the impact of front-back gate coupling on both carrier number and correlated mobility fluctuations, the impact of channel geometry (thickness, width and length) on the strength of the remote Coulomb scattering, and the presence of generation-recombination noise centers in the semiconductor region of such ultra-thin channels. We demonstrated that reducing the channel cross-section (width*thickness) or applying negative back-bias to increase the threshold voltage can lead to enhanced CMF levels.

Afterwards, we presented a thorough study of the LFN variability phenomenon and its properties. A comparison was shown between many different technology nodes, revealing a superiority of the FDSOI technology with respect to the LFN device-to-device variations. Moreover, some new methods of statistical LFN/RTN characterization were demonstrated, as well as the LFN variability dependences on gate bias, frequency and temperature.

Finally, our methodology regarding the noise model implementation for circuit simulations was presented in detail. The "Periodic Transient Noise" simulation method was also explained thoroughly, demonstrating its ability to produce realistic LFN-aware time-domain simulations. Also, after showing in which way both frequency and time-domain noise model approaches can be implemented through Verilog-A, we showed how the LFN and RTN of a nano-scale device can affect the stability and thus the performance limitations of a SRAM cell.

We hope that the content of this chapter will contribute to the clarification of any misconceptions regarding the fluctuation mechanisms in FDSOI MOSFETs and help towards a better understanding of the LFN and RTN phenomena in general, as well as the adoption of the noise characterization, modeling and simulation methods presented.

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Abbreviations

CMF	Correlated mobility fluctuations
CNF	Carrier number fluctuations
C_{ox}	Gate oxide capacitance per area
C_{si}	Silicon capacitance per area
FD	Fully depleted
freq	Escape frequency
g_d	Drain voltage transconductance
g_m	Gate voltage transconductance
HMF	Hooge mobility fluctuations
n_1	Carrier density near trap when $E_T=E_F$
n_s	Carrier density near trap
PD	Partially depleted
PSD	Power spectral density
Q_i	Inversion charge density
Q_{i1}	Inversion charge density near trap when $E_T=E_F$
RCS	Remote Coulomb scattering
R_{sd}	Source/drain series resistance
S_{Id}	Drain current power spectral density
SOI	Semiconductor On Insulator
S_{Vfb}	Flat-band voltage power spectral density
S_{Vg}	Input-referred gate voltage power spectral density
t_{ox2} / t_{box}	Back gate oxide
$V_{BG} / V_{G2} / V_B$	Back gate voltage
V_t	Threshold voltage
x_t	Trap depth in oxide
α / α_{sc}	RCS coefficient
v_{th}	Thermal velocity
σ	Trap cross section
σ_0	Trap cross section for interface trap
τ	Trap time constant
τ_c	Capture time
τ_e	Emission time
Ω	CMF factor