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P. Sideris, L. Brunet, L. Ciampolini, G. Sicard, P. Batude, et al.. Inter-tier electrostatic coupling effects in 3D sequential integration devices and circuits. Solid-State Electronics, 2020, 168, pp.107715. ⟨10.1016/j.sse.2019.107715⟩. ⟨hal-03089143⟩

HAL Id: hal-03089143

https://hal.science/hal-03089143v1

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Inter-Tier Electrostatic Coupling Effects in 3D Sequential Integration Devices and Circuits

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Abstract

This work presents for the first time an analytical study of the electrostatic coupling between bottom and top layer of 3D sequential integration devices, regarding its impact on both static and noise behavior. The effect is demonstrated experimentally through statistical measurements, and TCAD simulations are used to further examine its properties and propose ways for the limitation of inter-tier coupling. It is demonstrated that regarding digital applications, the coupling-induced fluctuations are well within the mismatch variation level.

Keywords

SOI; CMOS; Fully Depleted; M3D; Monolithic 3D; 3D Sequential Integration; stacked; coupling; SRAM;

1. Introduction

3D sequential integration, also named 3D monolithic integration or 3D VLSI, refers to a 3D integration scheme where the stacked devices are fabricated sequentially above each other. This process leads to outstanding high-density-contacts between the tiers (up to 10^8 3D via/mm^2) thanks to the high alignment precision obtained with lithography steppers [1], [2], compared to packaging integration schemes (TSV, Copper to Copper bonding etc.). However, the ultra-thin Inter-layer dielectric (ILD) separating the sequential tiers can act as a back gate oxide of the top transistor, becoming a pathway of electrical interference for the stacked devices. Consequently, the top device is an asymmetric double-gated FDSOI MOSFET sensitive to the electrode voltage variations of the bottom device. The experiments and TCAD simulations presented in this work prove that the stacked device exhibits a shift in its electrical characteristics due to this effect. Although the electrostatic coupling effect in M3D has been already presented in principle [3], [4], [5], [6], and experimentally verified [7], this is the first analytical study examining the coupling between the top and bottom tiers of 3D sequential technology stacking 28 nm FDSOI MOSFETs, under normal circuit operation (V_{DD} = ±0.9V) and its impact on low frequency noise (LFN) performance of the stacked device.

2. Experimental details

The devices under study were top n-channel FDSOI MOSFETs, with EOT = 1.2 nm, t_{Si} = 7 nm and ILD thickness t_{ILD} = 130 nm

(shown in Fig. 1) stacked above standard high temperature FDSOI CMOS devices. More details about the low thermal budget process used for top FET fabrication and the CoolCube^{TM} process integration scheme can be found in [2]. The gate width of the measured devices is W = 2 µm for both tiers, whereas two different gate lengths were measured (L = 1 µm and L = 0.1 µm). The static measurements were performed with the Agilent B1500A device parameter analyzer and the low-frequency noise measurements with the NOISYS7 equipment by Synergie Concept [8].

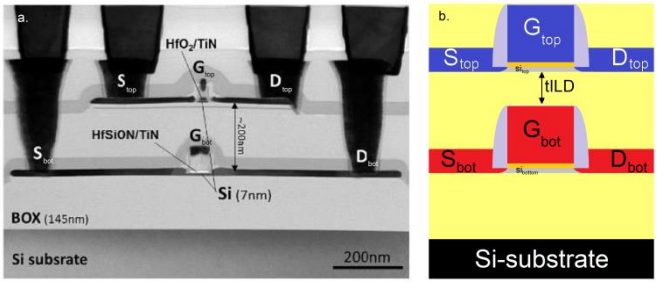

Fig. 1. a) TEM picture of two stacked transistors fabricated in M3D technology. The top device channel is separated from the bottom device gate by 130nm dielectrics. b) Schematic of the experimental configuration studied in this work. The applied gate voltages are shown in Table I along with V_{Dtop}=30mV and V_{Sbot},V_{Dbot} floating.

3. Results and discussion

In order to estimate the electrostatic coupling effect from the bottom to the top tier NMOS devices, a large set of experimental data was examined using different gate bias of the bottom transistor, i.e. V_{Gbot} = 0 V (bottom device OFF), 0.9 V (upper voltage limit) and -0.9 V (lower voltage limit), as shown in Table I. The gate voltage of the top tier devices was varied from V_{Gtop} = 0 V to 0.9 V in linear region of operation with the application of a 30 mV drain voltage, V_D.

TABLE I. CASES OF BOTTOM TRANSISTOR GATE BIAS

	Bottom OFF	**Bottom ON**	
		Upper limit	Lower limit
V_{Gbot}	0 V	0.9 V	-0.9 V
V_{Gtop}	0 → 0.9 V		

The opposite case, i.e. an electrostatic coupling effect from the top to the bottom device does not exist, because when the bottom transistor is in operation, its gate metal layer is biased and therefore it is shielding the bottom channel from any electric field penetration from the top transistor gate bias.

A. Impact on electrical parameters of top tier device

For the purpose of this study, we selected 126 dies for the top tier device that demonstrated good input characteristics. Fig. 2a shows the I_{Dtop}-V_{Gtop} characteristics results of NMOS devices with L = 1 μm. An example of electrostatic coupling is shown in Fig. 2(b), where a visible coupling-induced threshold voltage shift, ΔV_t, can be seen in both linear and log plots of I_{Dtop}-V_{Gtop}, whereas a slight change in the sub-threshold swing is observed in Fig. 2(c) (log-scale plot).

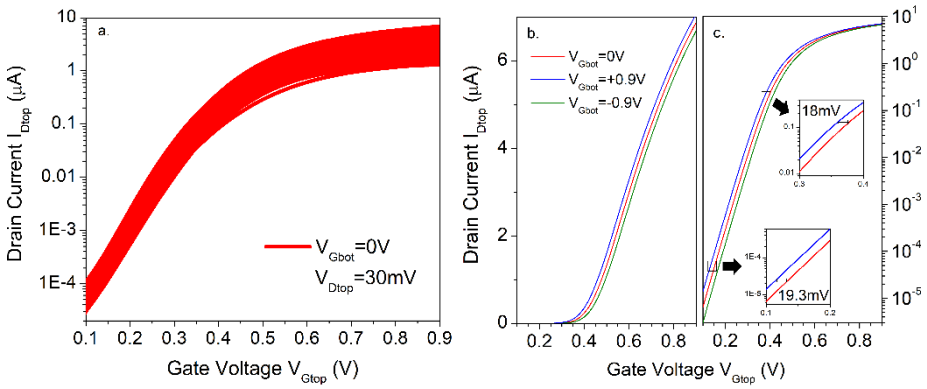

Fig. 2. (a) Drain current versus gate voltage for NMOS devices stacked on top of another NMOS, both with 2 μm^2 area (total of 126 dies). (b) Drain current versus gate voltage for an n-MOSFET (W = 2 μm, L = 1 μm) in linear scale and (c) in log scale, for all cases shown in Table I.

An automatic modified Y-function method [9] was applied to extract the threshold voltage, V_t, values for all 126 dies. As shown in Fig. 3, the coupling-induced V_t shift, ΔV_t, was found to be equal to -15.6mV ± 2.87 mV and 14.7mV ± 2.38mV for a positive and a negative V_{Gbot} bias respectively. The small difference between their mean values can be attributed to the weak bottom interface accumulation for negative V_{Gbot}, while the ~15% variation is attributed to the variability in t_{ILD} (estimated ±20nm for the wafer under study), that in turn affects the ΔV_t variability through the SOI coupling relation, given by (1) [10]:

$$\frac{\Delta V_t}{V_{Gbot}} = -\frac{C_{si(top)}C_{ILD}}{C_{ox(top)}\left(C_{ILD}+C_{si(top)}\right)} \qquad (1)$$

where $C_{si(top)}$, $C_{ox(top)}$, C_{ILD} are the top channel, the top oxide, and the ILD capacitances per unit area.

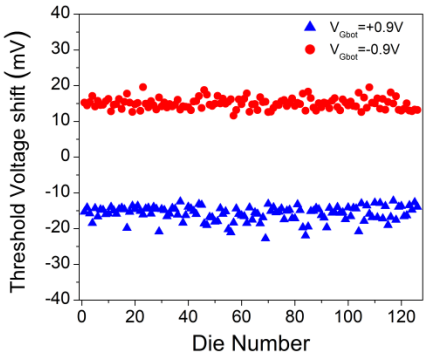

Fig. 3. Threshold voltage shift of top tier NMOS devices for linear regime (V_{Dtop} = 30 mV).

The extracted average ΔV_t of around 15 mV may seem significant, but it is well within the local variability limits (mismatch) of 28nm FDSOI technology [9], as can be seen in Fig. 4(a), for digital applications. Furthermore, the crossing point between mismatch and coupling reveals that even with an ILD thickness of 130nm, the maximum gate area for which the coupling-induced ΔV_t does not exceed the mismatch variations is much higher than the typical gate areas used in digital circuits. Similarly to ΔV_t, through Fig. 4(b) is demonstrated that both on- and off-current coupling-induced shifts ΔI_{off} and ΔI_{on}, are negligible compared to the calculated normalized mismatch variations of I_{off} and I_{on} in 28 nm FDSOI technology, for a typical range of gate areas in digital design.

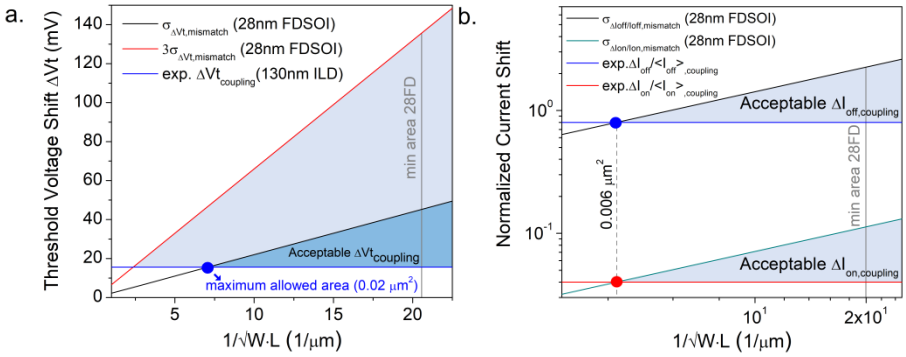

Fig. 4. a) Coupling-induced shift and mismatch-related variations (28 nm FDSOI versus reciprocal of gate area square root) for a) threshold voltage and b) I_{off} and I_{on} current shift. The vertical marker in figure 4(a) indicates the mismatch standard deviation for the minimal transistor surface in 28 nm FDSOI (W = 80nm, L = 30 nm).

B. Impact on LFN of top tier device

To study the electrostatic coupling impact on the top device LFN level, the drain current noise spectral density was measured from weak to strong inversion for all cases shown in Table I. In order to neglect the shift in the DC value of I_{Dtop}, the measured noise was normalized by I_{Dtop}^2. Fig. 5 illustrates the corresponding spectra for three selected V_{Gtop} values. Contrary to the impact on the static behavior, no noticeable coupling-induced change is observed in the LFN spectra behavior.

To further verify that the bottom-to-top coupling impact on LFN is negligible, we plotted the normalized Power Spectral Density (PSD) value extracted at f = 10 Hz versus drain current for all bias cases shown in Table I. As Fig. 6(a) shows, the LFN level for L = 1 μm can be considered unchanged whatever the bottom transistor gate bias, from subthreshold to strong inversion region. The same is true for the top devices with L = 0.1 μm, however, as shown in Fig. 6(b), the general LFN dependence on top gate bias is not the same. The latter is a typical behavior for sub-μm MOSFETs, where the noise spectra are not 1/f-like in most cases, but dominated by Lorentzian noise, responsible for the observed humps [12].

In previous studies, it has been shown that the bottom gate bias of an FDSOI MOSFET can strongly affect the remote Coulomb scattering between carriers and trapped charge [13], [14], leading to a change in the Correlated Mobility Fluctuations (CMF) factor Ω in the 1/f noise model expressed through (2) [15]:

$$\sqrt{S_{Vg}} = \sqrt{S_{Vfb}}\left(1 + \Omega\frac{I_d}{g_m}\right) \qquad (2)$$

where S_{Vg} is the input-referred gate voltage noise PSD, S_{Vfb} the flat-band voltage noise PSD and g_m the transconductance.

Therefore, in order to verify if the bottom transistor gate bias under normal operation can affect the CMF factor Ω, we plotted the square root of the input-referred gate voltage noise, S_{Vg}, versus I_d/g_m. As one can observe in Fig. 7, in all three cases (Table I), there is the same linear dependence, and the extracted Ω factor (inset) can be considered constant with V_{Gbot}.

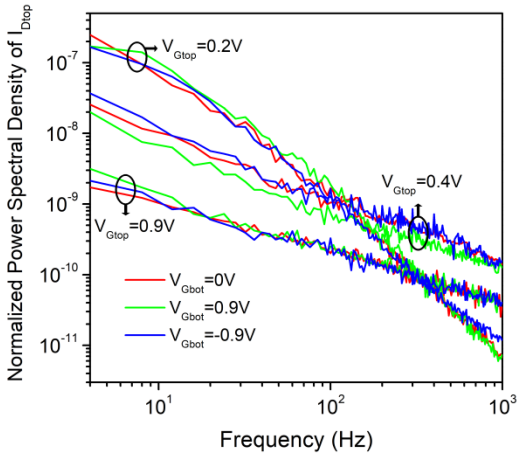

Fig. 5. Normalized drain current power spectral density vs frequency for a top NMOS with W = 2µm, L = 1µm in three different bias conditions of the bottom.

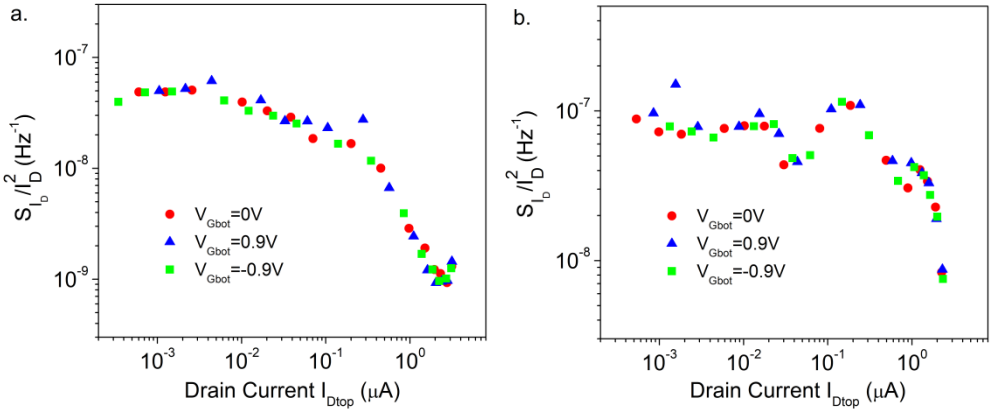

Fig. 6. Normalized power spectral density at f = 10 Hz vs drain current for a top NMOS with W = 2 µm, L = 1 µm (a) L = 0.1µm (b) and all bias cases of Table I.

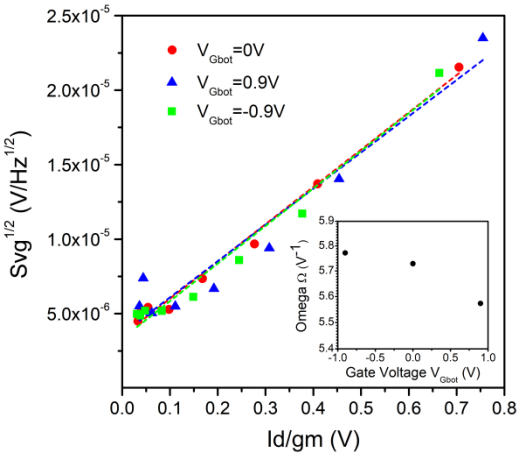

Fig. 7. Square root of input-referred gate voltage PSD S_{Vg} versus I_d/g_m (b) for a top NMOS with W=2μm, L=1μm and all bias cases of Table I.

C. Comparison with numerical simulations and proposed solutions for improvement

TCAD simulations were performed using the ATLAS Silvaco software, applying the same bias conditions as for the measurements (see Table I), as well as the same channel and gate oxide thickness values.

Fig. 8(a) shows the dependence of ΔV_t with t_{ILD} revealing a good agreement with the experimental results for a t_{ILD} of 130nm. From the same diagram we can conclude that decreasing tILD (for example up to 75 nm) the coupling-to-mismatch margin is maintained in an adequate level while the 3D contact aspect ratio is improved. In addition, the inter-tier coupling impact may be efficiently reduced when there is a misalignment between top and bottom device positions. Indeed, as shown in Fig. 8(b), our simulations revealed that in cases where the bottom-to-top overlapping area ratio is lower than 0.5, the coupling-induced ΔVt can be decreased by a factor of 3. This observation may function as a guideline for 3D design rules in the near future.

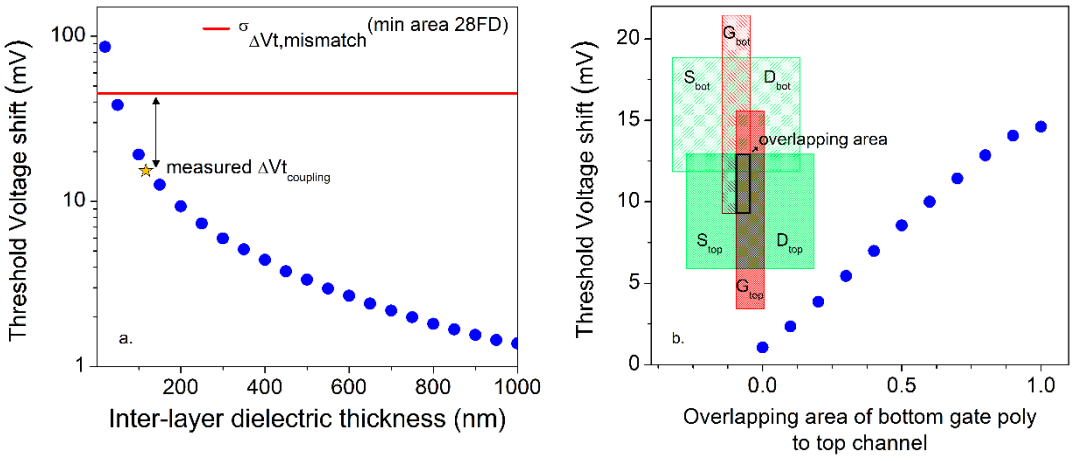

Fig. 8. (a) Coupling-induced threshold voltage shift vs ILD thickness for drain bias 30mV and ΔV_{Gbot}=-0.9V, compared with threshold voltage mismatch level for 28 nm FDSOI technology. (b) Threshold voltage shift vs overlapping gate area of bottom gate poly to top channel ($\frac{\text{Overlapping area}}{\text{Total top channel area}}$).

4. Monolithic 3D SRAM Analysis

Within the More than Moore context, 3D sequentially fabricated SRAM cells are framed as an extremely appealing architecture as they can provide denser and faster memory blocks, being co-integrated among various components (heterogeneous integration). Related work [14]–[19] clearly demonstrates the virtues of this option. Therefore, in order to study the possible impact of the coupling-induced V_t shift on a circuit's operation, we chose the 6T SRAM cell as a reference. In particular, we examined the configuration of a monolithic 3D (M3D) 2- bitcell SRAM, i.e. two stacked SRAM cells that are identical in layout design, so that the inter-tier coupling effects are maximized. Fig.1 shows the stacked M3D SRAM structure under consideration.

A. Methodology

As shown before, the inter-tier coupling is sensitive to both the ILD thickness and the layout design of the top/bottom cell with respect to each other. Except for using coupling advantageously [20], previous work considering undesirable coupling impact [21] has been carried out only for a single M3D SRAM bitcell having half of the transistors in each tier. Fig. 9 shows a schematic layout representation of the M3D 2-bitcell SRAM under study. Because the top transistors have an asymmetric double-gate SOI structure, one can consider that the Interlayer dielectric functions as their buried oxide and therefore their back gate terminalis indeed the front gate terminal of the respective bottom tier transistors.

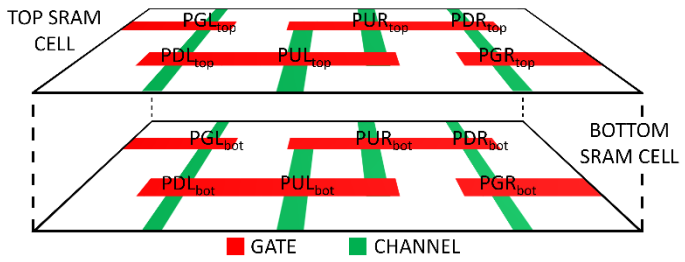

Fig. 9. Schematic layout representation of the M3D 2-bitcell SRAM under study.

In order to assess whether the bottom SRAM cell operation can significantly alter the top SRAM cell performance some of the most common stability metrics were investigated: the Read and Write Static Noise Margin (RSNM & WSNM) and the Supply Read Retention Voltage (SRRV), that can provide a profound overview of the top SRAM cell dynamic stability [22], [23]. The impact of coupling was studied in conjunction with the mismatch induced variations, using SPICE implementation of the equivalent circuit. The model chosen to describe the behavior of the top tier transistors is the LETI-UTSOI MOSFET model (version 2.11) that accurately captures the device characteristics. Furthermore, an appropriate parametrization was done to match the experimental coupling-induced behavior, analyzed in the previous sections.

The results (Fig. 10) show very good fitting between measurements and model for the static characteristics for the required

transistor biasing. In detail both linear and saturation behavior as well as the 15.6mV shift of the top transistor's threshold voltage due to bottom gate coupling, are accurately captured.

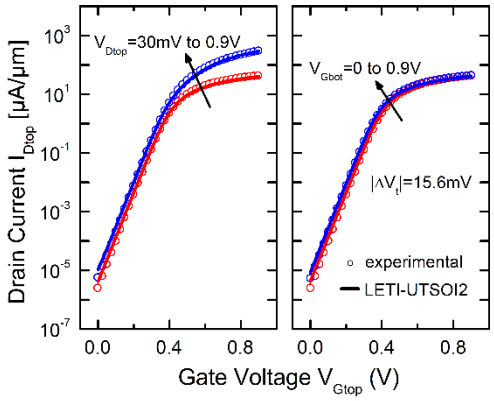

Fig. 10. Drain current versus gate voltage for the top tier NMOS device (L=100nm). Circles and lines denote experimental and simulation results respectively.

For the bottom SRAM cell operation we can distinguish 3 cases: 1) no operation (zero power supply), 2) a stored '0' (V_{CLbot}=0V, V_{CHbot}=1V), 3) a stored '1' (V_{CLbot}=1V, V_{CHbot}=0V). Table II summarizes the bottom transistor gate bias for each ~~one~~ of the 3 cases. These conditions were applied in the back gates of the respective top transistors to emulate the inter-tier coupling effect.

TABLE II. CASES OF BOTTOM TRANSISTOR GATE BIAS

	Bottom SRAM OFF	**Bottom SRAM ON**	
		Stored '0'	**Stored '1'**
V_{PULbot}	0 V	1 V	0 V
V_{PURbot}	0 V	0 V	1 V
V_{PDLbot}	0 V	1 V	0 V
V_{PDRbot}	0 V	0 V	1 V

B. SRAM stability metrics analysis

The RSNM represents the maximum tolerable DC noise voltage at each storage node before causing a read upset. The extraction of the RSNM was performed by applying mismatch-related Monte Carlo simulations to capture the impact of the mismatch variations. The SRAM cell can be repeated over 1 million times in memory circuits resulting in 6σ of mismatch variations. However, the 3σ limit is critical enough to compare it with the coupling induced shift and requires 1000 runs rather than over 1 million in the case of the 6σ limit. From the obtained butterfly curves (Fig. 11a), the mean represents the typical behavior while the blue curve shows the worst case of mismatch among the 1000 runs. The largest square was fit for the worst set to estimate the mismatch related RSNM degradation. Additionally, the mean RSNM was extracted and comparing the two values, the impact of the V_t mismatch is a RSNM reduction of 27%.

The same steps were followed after the addition of the coupling due to the operation of the bottom SRAM, the RSNM was extracted. As shown in Fig. 11b, the coupling-induced V_t shift can further reduce the RSNM by 1% more.

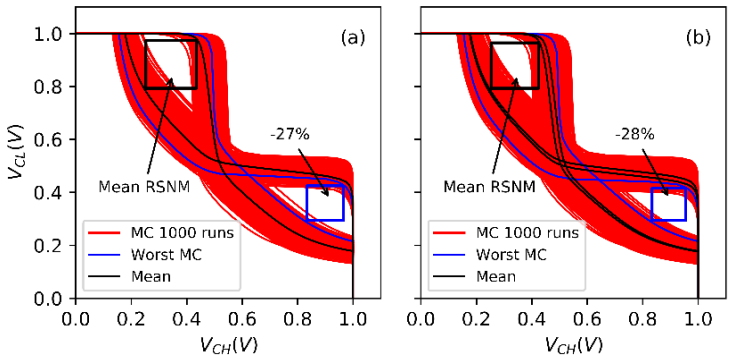

Fig. 11. (a) Impact of Vt mismatch on RSNM of top tier SRAM, (b) Addition of the static coupling because of the bottom tier SRAM operation

Following the same methodology as for the RSNM, we also extracted the WSNM that characterizes the write-ability of the SRAM bitcell (Fig. 12). Once again the reduction of the WSNM window due to the addition of the inter-tier coupling is 1% more.

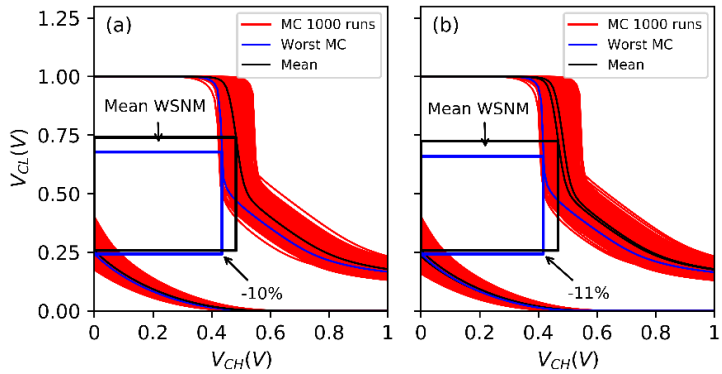

Fig. 12. (a) Impact of Vt mismatch on WSNM of top tier SRAM, (b) Addition of the static coupling because of the bottom tier SRAM operation

Regarding the SRRV, it is defined as the maximum allowed reduction of cell supply voltage for which the read stability is not affected. It is an equally important stability metric for SRAM cells [22]. It can be estimated measuring the bitline current I_{BL} while the power supply of the cell (V_{CELL}) is ramped down. At a specific value of the V_{CELL} (called V_{flip}), the stored bit is flipped and I_{BL} drops suddenly. Then the SRRV is extracted as

$$SRRV = V_{DD} - V_{flip} = 1 - V_{flip}$$

Fig.13 (a) shows the simulation results for a typical cell with the 3 cases of the bottom operation. It is apparent that the most critical case is when a '1' is stored at the bottom cell. By further adding for this case the mismatch variations with 1000 Monte-Carlo runs, we obtain is an additional SRRV reduction of 3.5%.

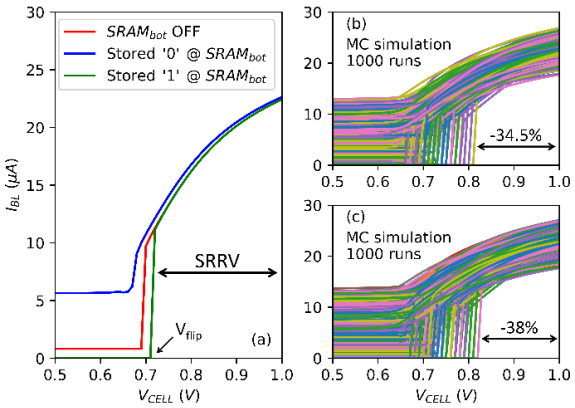

Fig. 13. Bit-line current versus cell supply voltage for (a) the three cased of the bottom SRAM operation and (b) Monte Carlo simulation with mismatch variations only or (c) adding also the static coupling induced shift.

CONCLUSIONS

A study of coupling-induced effects in the static and noise behavior of 3D sequential top tier transistors has been presented. Through both measurements and simulations, it was shown that the coupling-induced ΔV_t, ΔI_{off} and ΔI_{on} have high values considering analog applications, however they are well within the local variability limits of 28nm FDSOI technology for digital circuits, where sub-µm devices are used. Concerning the low frequency noise performance of the top tier transistor, no coupling-induced impact was observed regardless the transistor area. In addition, it was demonstrated that the coupling effect can be limited either by increasing the ILD thickness or through a top/bottom transistor misalignment. Finally, a circuit example of a M3D 2-bitcell SRAM proved the validity of our analysis as all of the metrics were altered negligibly (1 to 3.5%) by the inter-tier coupling compared to the mismatch-induced variations.

Acknowledgement

This work was partially supported by the LabEx Minos ANR-10-LABX-55-01 program.

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