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$f_{\max} = 800$ GHz with 75 nm gate length and asymmetric gate recess for InGaAs/InAlAs PHEMT

Samnoui, N.Wichmann, X.Wallart, C.Coinion, S.Lepilliet, S.Bollaert.

IEMN, University of Lille, CNRS, Centrale Lille, ISEN, Univ. Valenciennes, UMR 8520 - IEMN
UMR 8520 - IEMN 59000 Lille, France

mohammed.samnoui@univ-lille.fr & sylvain.bollaert@univ-lille.fr

Abstract— In This paper, we present a high maximum frequency of oscillation (f_{\max}) and a current-gain cutoff frequency (f_T) of 800 GHz and 260 GHz respectively with pseudomorphic high-electron mobility transistor (PHEMT), using a composite, InGaAs/InAs/InGaAs channel and an asymmetric gate recess. This result was achieved with long gate length $L_G = 75$ nm. The noise performance has been explored until 110 GHz, and gives a minimum noise figure $NF_{\min} = 0.8$ dB (1.8 dB) with associated gain $G_{\text{ass}} = 16$ dB (11.6 dB) at 40 GHz (94 GHz). Moreover extending the drain recess length to 225 nm and reducing the gate to source distance by 200 nm allows a $f_{\max} = 1.2$ THz.

I. INTRODUCTION

HElectron-Mobility Transistors (HEMTs) technology is the best candidate for low noise amplifier and Terahertz applications. Due to their superior high-frequency characteristics InP-based HEMTs are very promising for millimeter-wave applications and image sensor systems [1]. Currently, the record for f_{\max} is 1.5 THz ($f_T = 610$ GHz) [2] with pseudomorphic-HEMTs (PHEMTs) on InP substrate. In fact, for the last 10 years, the strategy used to improve electrical performance of HEMT was to reduce the gate length below 50 nm combined with epilayer engineering. This approach allows high cutoff frequencies and excellent transconductance with a record g_m of 3.1 mS/ μm [2], recently published papers report high f_{\max} while keeping longer gate length $L_G = 75$ nm [3].

II. FABRICATION

InAlAs/InAs/InGaAs Pseudomorphic HEMT (PHEMT) epitaxial layers were grown on semi-insulating InP substrate by gas source molecular beam epitaxy (MBE). The layer structure (figure 1), from bottom to top, consists of an $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ buffer layer, a bottom silicon-delta doped plane, an $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ first spacer, an $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InAs}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ composite channel, an $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ second spacer, a top silicon-delta doped plane, an $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ barrier, an InP etch-stop layer, and finally a thick $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ cap layer. The epilayer structure was optimized for high electron density and mobility in the channel. To achieve high channel mobility, strained pure InAs layer was inserted in InGaAs channel. Room temperature mobility of $\mu_{\text{Hall}} = 12000$ $\text{cm}^2/\text{V}\cdot\text{s}$ and a $N_{\text{Hall}} = 2.65 \times 10^{12}$ cm^{-2} are obtained by Hall measurement. For PHEMT fabrication, electron beam lithography was used. The first step of the fabrication was mesa isolation by wet chemical etching down to the InAlAs buffer layer. Next, Ohmic contact was realized as follow: after defining the Drain-Source with 1.5 μm distance by e-beam lithography, Ti/Pt/Au metals was evaporated.

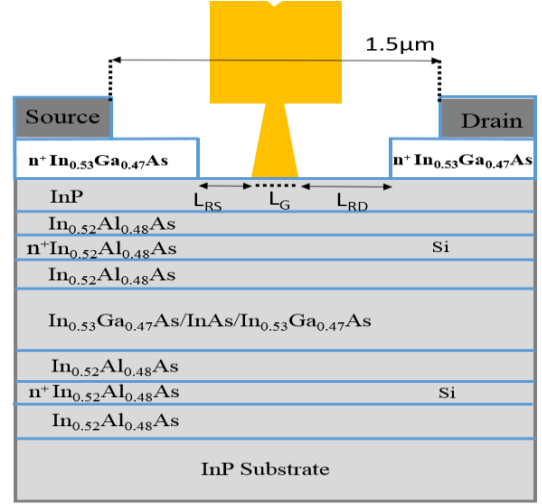


Fig. 1. Cross-section schematic of epitaxial layer structure.

The last process step concerns the asymmetric recess. The use of asymmetric recess will be motivated in the third part of this paper. For the recess, we need first to remove the InGaAs cap layer. Shinohara et al. [4] reported one of the fabrication technique for an asymmetric gate recess. This technique based on three-layers resist. The difficulty of this technique is observed during the opening of the slits that requires several precisions for the sizing, wet and dry etching. Furthermore, the recessed area is not passivated. Takahashi et al. [5] also reported a simple technique for an asymmetric gate recess, the process used based on one resist layer. After removing, the InGaAs cap layer the surface is passivated by Si_3N_4 film. Next, the gate electrode was deposited after definition of the gate footprint in Si_3N_4 by reactive ion etching RIE using SF_6 gas. However, the etching of Si_3N_4 using SF_6 have an effect on the electrical characteristics of the channel.

To verify the impact of the plasma etching, Hall measurements were performed after removing the Si_3N_4 . The mobility and the electron density were degraded by 10% and 25% from 12000 $\text{cm}^2/\text{V}\cdot\text{s}$ to 11000 $\text{cm}^2/\text{V}\cdot\text{s}$ and from $N_{\text{Hall}} = 2.65 \times 10^{12}$ cm^{-2} to $N_{\text{Hall}} = 1.97 \times 10^{12}$ cm^{-2} respectively. Then, we used a different technique. After e-beam lithography defining the recess zone, the cap layer was removed by wet chemical etching. The second e-beam lithography was performed in bilayers resists to define the shape of the T-gate. Ti/Pt/Au metals was evaporated. Finally, the sample was loaded into PECVD chamber where 30 nm-thick Si_3N_4 were deposited to form a passivation layer and decreasing the sheet resistance in recessed zones. This technique allows the asymmetry of the recess.

III. RESULTS

In this part, we will focus on the RF characterization. Concerning the DC measurements, the drain current is around $I_D = 800$ mA/mm and $I_D = 1000$ mA/mm for the reference and optimized PHEMT respectively. In both HEMTs, the recess length on the source side L_{RS} is 65 nm. The difference was in the recess on the drain side L_{RD} (figure 1). L_{RD} is 175 nm and 225 nm for the referenced and optimized transistor respectively. The gate to source distance was reduced by 200 nm for the optimized transistor. The extrinsic peak transconductance g_m of 1400 mS/mm was obtained at $V_{DS} = 0.8$ V for both transistors. S-Parameters were measured up to 110 GHz. The extrapolation by (20 dB/decade) of the unilateral Mason's gain U gives $f_{max} = 800$ GHz for the reference PHEMT and $f_{max} = 1.2$ THz for the optimized PHEMT at $V_{DS} = 1$ V (figure 2).

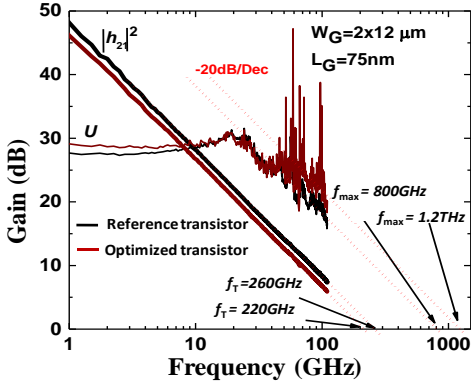


Fig. 2. Measured $U/|h_{21}|^2$ for reference and optimized PHEMT ($L_G = 75$ nm and $W = 2 \times 12 \mu\text{m}$)

To understand the impact of increasing the drain side recess on f_{max} , four devices were characterized up to 110 GHz. The source side recess was fixed at ~ 65 nm and L_{RD} varies from 70 nm to ~ 195 nm. The results are shown in figure 3. The symmetric devices, with $L_{RD} = L_{RS} \approx 65$ nm had a $f_{max} = 520$ GHz. As L_{RD} increased, the gain becomes more and more important thanks to the improvement of intrinsic parameters of the transistor also shown in figure 4. This indicates that the coupling between drain and gate is lower comparing to the gate source coupling [6]. In order to extract the four noise parameters of the reference PHEMT, NF_{50} method [7] has been used. The results achieved at 94 GHz were NF_{min} of 1.8 dB (with associated gain of 11.6 dB) for an optimal gate voltage $V_{GS_{Opt}} = -0.3$ V are shown in table 1.

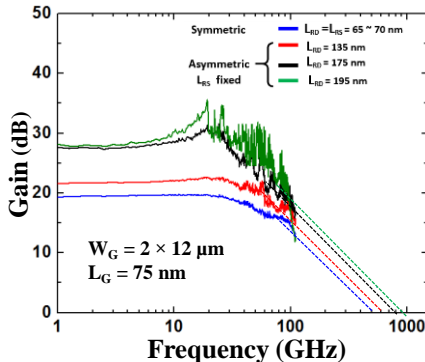


Fig. 3. Impact of drain side recess (L_{RD}) on f_{max}

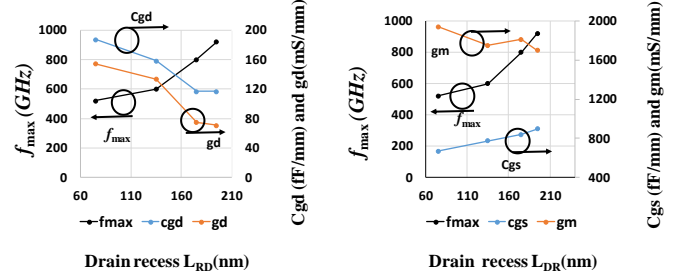


Fig. 4. Impact of drain side recess (L_{RD}) on intrinsic parameters

TABLE I
FOUR NOISE PARAMETERS VALUES OF REFERENCE PHEMT

Parameters	At 40 GHz	At 94 GHz
NF_{min} (dB)	0.82	1.8
G_{ass} (dB)	16	11.6
R_n (Ω)	45.1	41.6
Mag (Γ_{Opt})	0.8	0.64
$Phase$ (Γ_{Opt}) deg	19.7	48.3

IV. CONCLUSION

In conclusion, we have fabricated PHEMT operating above 800 GHz using an asymmetric gate recess with large gate length of 75 nm. This performance was obtained thanks to improvement of the epilayer structure with mobility channel of $\mu_{Hall} = 12000$ $\text{cm}^2/\text{V}\cdot\text{s}$. The use of an asymmetric recess improve the intrinsic parameters such as C_{gs} and C_{gd} capacitances. The output conductance g_d was also improved when L_{RD} increasing.

REFERENCES

- [1] M. Sato *et al.*, "Compact receiver module for a 94 GHz band passive millimetre-wave imager," *Antennas Propag. IET Microw.*, vol. 2, no. 8, pp. 848–853, Dec. 2008.
- [2] X. Mei *et al.*, "First Demonstration of Amplification at 1 THz Using 25-nm InP High Electron Mobility Transistor Process," *IEEE Electron Device Lett.*, vol. 36, no. 4, pp. 327–329, Apr. 2015.
- [3] T. Takahashi *et al.*, "Maximum frequency of oscillation of 1.3 THz obtained by using an extended drain-side recess structure in 75-nm-gate InAlAs/InGaAs high-electron-mobility transistors," *Appl. Phys. Express*, vol. 10, no. 2, p. 024102, Jan. 2017.
- [4] "Simple and high-precision asymmetric gate-recess process for ultrafast InP-based high electron mobility transistors," *J. Vac. Sci. Technol. B Microelectron. Nanometer Struct. Process. Meas. Phenom.*, vol. 20, no. 5, pp. 2096–2100, Sep. 2002.
- [5] T. Takahashi *et al.*, "Enhancement of f_{max} to 910 GHz by Adopting Asymmetric Gate Recess and Double-Side-Doped Structure in 75-nm-Gate InAlAs/InGaAs HEMTs," *IEEE Trans. Electron Devices*, vol. 64, no. 1, pp. 89–95, Jan. 2017.
- [6] D. G. Ballegeer, I. Adesida, C. Caneau, and R. Bhat, "Physics and behavior of asymmetrically recessed InP-based MODFET's fabricated with an electron beam resist process," in *Proceedings of 1994 IEEE 6th International Conference on Indium Phosphide and Related Materials (IPRM)*, 1994, pp. 331–334.
- [7] G. Dambrine, H. Happy, F. Danneville, and A. Cappy, "A new method for on wafer noise measurement," *IEEE Trans. Microw. Theory Tech.*, vol. 41, no. 3, pp. 375–381, Mar. 1993.