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# Linearity and robustness evaluation of 150-nm AlN/GaN HEMTs

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## Abstract

We report on linearity and robustness of AlN/GaN HEMTs with ultra-thin 4nm AlN barrier for millimeter wave range applications. Static and dynamic I-V characteristics feature high peak transconductance ( $g_{\text{mpeak}}$ ) of 385 mS/mm, and the transconductance exhibits small changes with gate bias. Semi on-state step stress and 24 h stress tests have been carried out on representative AlN/GaN HEMTs on SiC substrate. No catastrophic failure was identified after semi on-state step stress at  $V_{\text{GS}} = -1.5$  V up to  $V_{\text{DS}} = 100$  V, whereas a  $g_{\text{mpeak}}$  drop of 26 % was observed in these conditions. Moreover, 24 h stress carried out at different bias voltage along a load line show good robustness of these devices up to  $V_{\text{DS}} = 25$  V. In addition, an abrupt gate leakage current increase was identified to be field dependent, and associated with hot spots identified by electroluminescence measurements. Even in presence of a simple SiN passivation without air bridges or field plates, these devices exhibit high power added efficiency up to 40 GHz, thus demonstrating the great potential of AlN/GaN heterostructures.

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## 1. Introduction

GaN based High Electron Mobility Transistors (HEMTs) hold tremendous interest for millimeter wave applications especially with the emergence of the fifth generation (5G) communications technology, this is thanks to their high electron mobility and breakdown voltage [1]. For high power amplifiers (HPA) operating beyond 30 GHz, innovative device downscaling with ultra-short gate length ( $L_G < 200$  nm) and ultra-thin barrier layer are needed whilst maintaining high power added efficiency (PAE) combined with high output power in millimeter wave range. Recently, AlN/GaN HEMTs with sub-10nm AlN barrier layer demonstrated promising performance with PAE exceeding 40 % at 40 GHz [2]. AlN/GaN HEMTs with a maximum output current density of 2.3 A/mm and a peak extrinsic transconductance of 480 mS/mm [3] have also been reported.

The transconductance of GaN based HEMTs exhibits significant changes with the gate bias, and this is considered as a critical issue for the linearity performance of the device [4] [5] [6]. This limits large signal operation at high frequencies as well as power linearity, since the gain of a HEMT is critically dependent on the transconductance. The devices used in multichannel transmissions tend to produce intermodulation distortion, which leads to

the degradation of the system signal-to-noise ratio. The third-order intermodulation distortion (IM3) is considered as the most important parameter for the linearity performance of the devices. In order to reduce IM3, the transconductance needs to remain constant during a wide operating range of the gate bias [7].

In this paper, we evaluate for the first time the linearity and robustness of 150-nm AlN/GaN HEMTs on SiC substrate with C-doped GaN buffer and 4-nm AlN barrier. In addition to their outstanding RF performance in terms of high output power combined with high power added efficiency at 40 GHz, AlN/GaN HEMTs show good robustness after 24 hours stress test.

## 2. Samples details

The AlN/GaN heterostructures were grown by metal organic chemical vapor deposition (MOCVD) on 4 inch SiC substrates [8]. The HEMT structure consists of transition layers to GaN, a 1  $\mu\text{m}$ -thick C-doped GaN buffer layer followed by an undoped GaN channel, a 4.0 nm ultrathin AlN barrier layer and a 10-nm-thick in situ Si<sub>3</sub>N<sub>4</sub> cap layer. The in-situ SiN layer is used both as early passivation as well as to prevent strain relaxation. Ohmic contacts were formed directly on the top of the AlN barrier by etching the in-situ SiN cap layer. A Ti/Al/Ni/Au metal stack was used for ohmic contacts followed by

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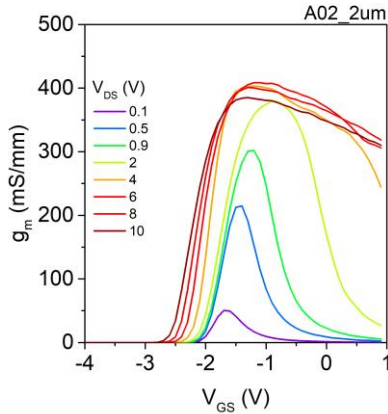


Fig - 1.  $g_m$  versus  $V_{GS}$  characteristics of a representative AlN/GaN HEMT

a rapid thermal annealing at 875°C. T-shaped Ni/Au Schottky contacts with 150-nm footprint and a top gate length of 400 nm were defined by e-beam lithography. The in-situ SiN underneath the gate pattern was fully removed using a low-power SF6 plasma etching. Device isolation was achieved by nitrogen implantation. A 200-nm thick Ex-situ SiN film was deposited by Plasma-Enhanced Chemical Vapor Deposition (PECVD). Room-temperature Hall measurements showed high electron sheet concentrations of  $1.8 \times 10^{13}$  and  $1.6 \times 10^{13} \text{ cm}^{-2}$  with an electron mobility about  $1100 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ .

### 1. DC and double pulse characterization

Fig - 1 shows transconductance ( $g_m$ ) versus  $V_{GS}$  characteristics of a representative AlN/GaN HEMT. The extrinsic transconductance peaks at 385 mS/mm at  $V_{DS} = 10 \text{ V}$  and  $V_{GS} = -1.3 \text{ V}$ . The presented devices are indeed still limited by the access resistances. Typical contact resistances are as high as 0.5 ohm.mm severely reducing the extrinsic transconductance. Intrinsic transconductance is in the range of 600 mS/mm for this device design. This high value results from the short gate-to-channel distance [9]. Interestingly, the transconductance of AlN/GaN HEMTs exhibits small changes with the gate bias for  $V_{DS} > 4 \text{ V}$ , unlike for AlGaIn/GaN HEMTs. This is owing to the ultra-thin AlN barrier with high Al content, and to the less negative threshold voltage [10][11]. Fig - 2 shows the double pulse  $g_m$  versus  $V_{GS}$  characteristics at  $V_{DS} = 8 \text{ V}$  at quiescent bias (QB) conditions (0 V, 0 V), (-5 V, 0 V), (-5 V, 5 V) and (-5 V, 10 V) of a representative AlN/GaN HEMT. The pulse width was set to 1  $\mu\text{s}$  with a duty cycle of 1 %. The current collapse rate corresponding to the gate-lag is 16.5 %. Moreover, the drain lag rate between (-5 V, 0 V) and (-5 V, 10 V) corresponds to 13.3 %.

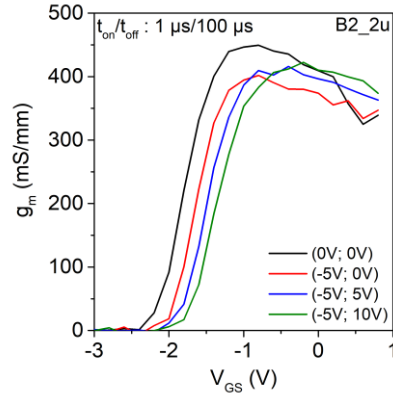


Fig - 2. Double pulse  $g_m$ - $V_{GS}$  characteristics at different QB conditions of a representative AlN/GaN HEMT.

A positive shift of threshold voltage, that is correlated with current collapse, is identified at QB (-5 V, 0 V) that increases by increasing drain source QB. Moreover, the transconductance versus  $V_{GS}$  remains high at positive  $V_{GS}$  under the different QB conditions

### 2. Semi on-state step stress

Before starting short or long term reliability tests at the bias targeted for the final application for these devices (in this case high power amplifiers (HPA) in class AB operation), it is mandatory to evaluate the limits and the safe operating area (SOA) of the process. DC step stress test is submitted at semi on-state ( $V_{GS} > V_{TH}$ ) condition. For this bias point, the gate is biased at  $V_{GS\text{Stress}} = -1.5 \text{ V}$  and the drain voltage is increased from 0 V to device failure by a step of 5 V during 2 min each step [12]. In this case, the drain voltage compliance was limited to 100 V. During the step stress test, drain and gate currents are monitored, electroluminescence is used after each step in on-state (peak of EL bell versus  $V_{GS}$ ) and off-state conditions, to check the distribution of the electroluminescence emission on the gate fingers during stress, if there are hot spots induced by the stress showing the creation of leakage paths or for the onset of the device failure. Fig - 3 shows  $g_m$ - $V_{GS}$  characteristics, at  $V_{DS} = 0.1$  and 10 V, after each step of semi on-state step stress at  $V_{GS\text{Stress}} = -1.5 \text{ V}$ . As illustrated in Fig - 4, the transconductance peak as well as the threshold voltage remain constant until  $V_{DS\text{Stress}} = 25 \text{ V}$ . Moreover,  $g_{m\text{peak}}$  decreases almost linearly for  $V_{DS\text{Stress}} > 25 \text{ V}$  to drop by 26% at  $V_{DS\text{Stress}} = 100 \text{ V}$ . Furthermore, the threshold voltage shifts positively for  $V_{DS\text{Stress}} > 25 \text{ V}$  to shift by 46 mV at  $V_{DS\text{Stress}} = 100 \text{ V}$ . Moreover, an abrupt decrease of forward and reverse gate voltage, in addition to an

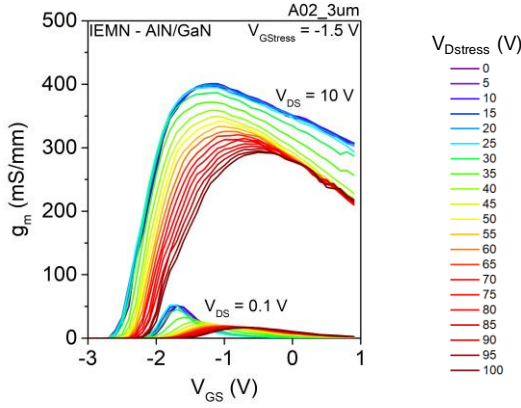


Fig - 3.  $g_m$ - $V_{GS}$  characteristics after each of semi on-state step stress at  $V_{GS_{Stress}} = -1.5$  V

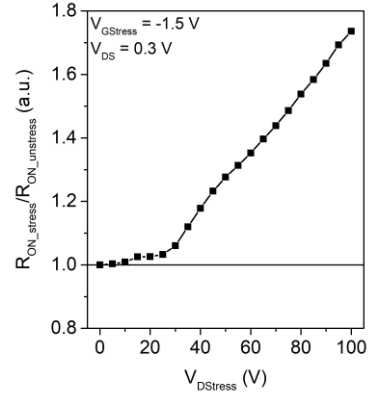


Fig - 6.  $R_{ON}$  variation during semi on-state step stress at  $V_{GS_{Stress}} = -1.5$  V of AlN/GaN HEMT

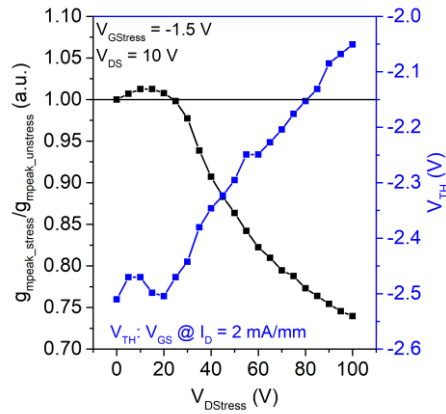


Fig - 4.  $G_{m_{peak}}$  and  $V_{TH}$  at  $V_{DS} = 10$  V variation during semi on-state step stress at  $V_{GS_{Stress}} = -1.5$  V of AlN/GaN HEMT

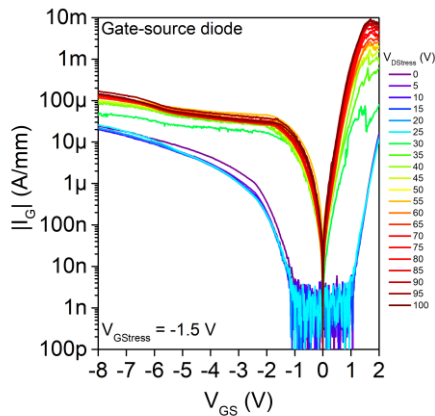


Fig - 5.  $I_G$ - $V_G$  characteristics after each step of semi on-state step stress at  $V_{GS_{Stress}} = -1.5$  V of AlN/GaN HEMT

increase of gate leakage current are identified at  $V_{DS} > 25$  V as shown in Fig - 5.

The on-state resistance ( $R_{ON}$ ) shows no degradation up to  $V_{DS} = 25$  V, whereas it linearly increases for  $V_{DS} > 25$  V to degrade by about 74% at  $V_{DS} = 100$  V, as shown in Fig - 6. By considering the different parameters variation with semi on-state step stress, it is suggested that the non-reversible degradation occurs at the critical voltage  $V_{DS} = 25$  V, due to degradation in the access regions ( $R_{ON}$  variation) and below the gate contact ( $V_{TH}$  variation) to be related to degradation of Schottky/AlN and SiN/AlN interfaces that field driven.

### 3. DC 24h robustness stress

This part focuses on the robustness of AlN/GaN HEMTs, by using 24 hours DC stress test, to assess the root cause for degradation mechanisms under stress limiting the electrical performance by considering semi on-state condition with  $V_{DS_{Stress}} \leq 25$  V. In this part, we discuss the robustness of AlN/GaN HEMTs at the bias conditions:  $(V_{GS_{Stress}}, V_{DS_{Stress}}) = (-1.2$  V, 10 V),  $(-1.5$  V, 15 V),  $(-2$  V, 20 V) and  $(-2.5$  V, 25 V). Different electrical parameters are recorded after interrupting the stress at 1h, 2h, 4h, 8h, 16h and 24h. Fig - 7 illustrates  $I_D$ - $V_{DS}$  characteristics of a representative AlN/GaN HEMT with  $V_{GS}$  from -3 V to 0 V with a pronounced kink effect. Circular dots are  $I_D$ - $V_{DS}$  bias-points adopted for 24-hours tests. The bias conditions at  $V_{DS} = 20$  V with  $I_D = 150$  mA/mm and  $V_{DS} = 25$  V with  $I_D = 100$  mA/mm were chosen according to the bias targeted for the final application for these devices (i.e. high power amplifiers in AB class operation).

1.1.  $(V_{GS_{Stress}}; V_{DS_{Stress}}) = (-1.2$  V, 10 V)

Fig - 8 shows the variation of gate current during

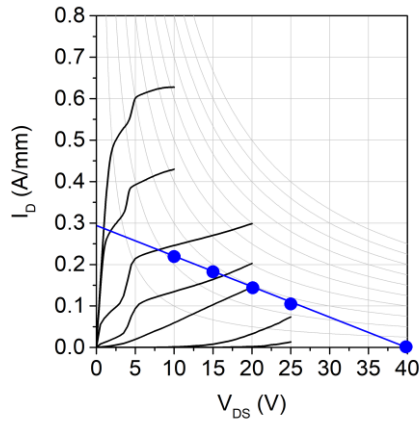


Fig - 7.  $I_D$  vs  $V_{DS}$  output characteristics of representative AlN/GaN HEMT, with  $V_{GS}$  from -3 V to +1 V in 0.5 V steps. Circular dots are  $I_D$ - $V_{DS}$  bias-points adopted for 24-hours tests

24h stress test at different steps: 1h, 2h, 4h, 8h, 16h and 24h, carried out at  $(V_{GStress}, V_{DStress}) = (-1.2$  V, 10 V).

Although the gate current is slightly noisy during the stress, it remains stable at a steady level around 1  $\mu$ A/mm. Moreover, electroluminescence (EL) emission intensity is uniformly distributed along the gate fingers during the stress, highlighting the good distribution of carriers in the channel, as shown in Fig - 9. Moreover, no hot spots are identified during stress. The microscopy image of the stressed device after 24h stress shows no damage in the device structure.

Fig - 10 shows  $g_{mpeak}$  at  $V_{DS} = 10$  V monitored during the different steps of the 24h stress at  $(V_{GStress}, V_{DStress}) = (-1.2$  V, 10 V) compared to their initial values before stress.

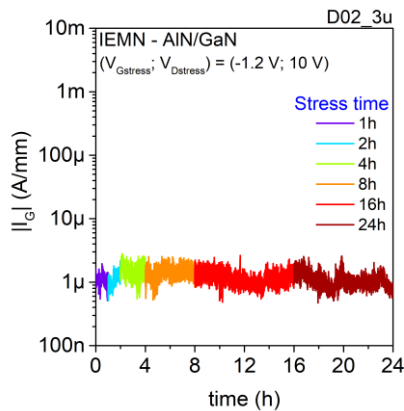


Fig - 8. Variation of gate current during 24h step-stress experiment carried out at  $(V_{GStress}, V_{DStress}) = (-1.2$  V, 10 V) with the electrical parameters monitored at 1h, 2h, 4h, 8h, 16h and 24h of AlN/GaN HEMT

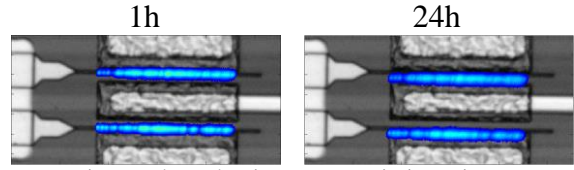


Fig - 9. Electroluminescence emission microscopy images during 24h stress test at two steps: 1h and 24h at  $(V_{GStress}, V_{DStress}) = (-1.2$  V, 10 V) of AlN/GaN HEMT.

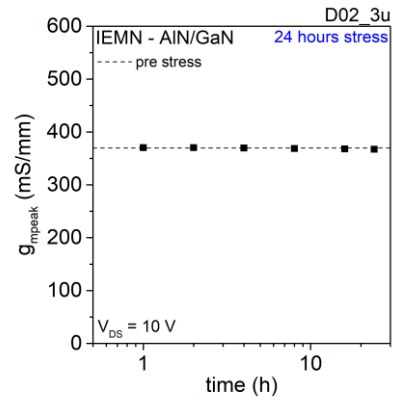


Fig - 10.  $g_{mpeak}$  at  $V_{DS} = 10$  V monitoring during 24h stress carried out at  $(V_{GStress}, V_{DStress}) = (-1.2$  V, 10 V) of AlN/GaN HEMT

The  $g_{mpeak}$  values after the different steps of the 24h stress are superimposed with their initial values before stress. Thus, no abrupt leakage currents increase or device degradation are identified after 24h stress at  $(V_{GStress}, V_{DStress}) = (-1.2$  V, 10 V).

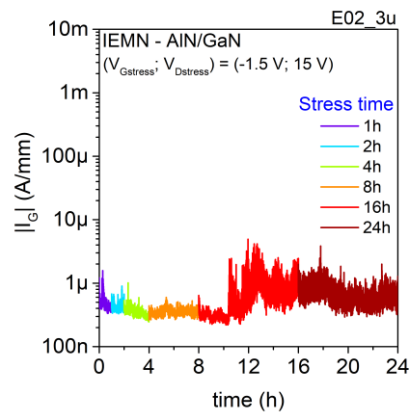


Fig - 11. Variation of gate current during 24h step-stress experiment carried out at  $(V_{GStress}, V_{DStress}) = (-1.5$  V, 15 V) with the electrical parameters monitored at 1h, 2h, 4h, 8h, 16h and 24h of AlN/GaN HEMT

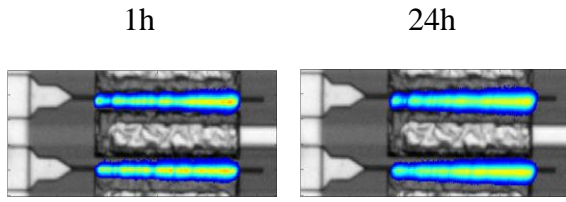


Fig - 12. Electroluminescence emission microscopy images during 24h stress test at two steps: 1h and 24h at  $(V_{GStress}, V_{DStress}) = (-1.5 \text{ V}, 15 \text{ V})$  of AlN/GaN HEMT.

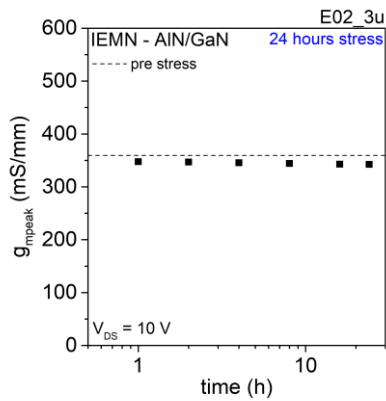


Fig - 13.  $g_{mpeak}$  at  $V_{DS} = 10 \text{ V}$  monitoring during 24h stress carried out at  $(V_{GStress}, V_{DStress}) = (-1.5 \text{ V}, 15 \text{ V})$  of AlN/GaN HEMT

### 1.2. $(V_{GStress}; V_{DStress}) = (-1.5 \text{ V}, 15 \text{ V})$

Fig - 11 shows the variation of gate current during 24h stress test at different steps: 1h, 2h, 4h, 8h, 16h and 24h, carried out at  $(V_{GStress}, V_{DStress}) = (-1.5 \text{ V}, 15 \text{ V})$  of AlN/GaN HEMT.

The gate current, during the stress, becomes more noisy starting from 10h stress, however it remains stable with no apparent abrupt increase with  $|I_G| \leq 1 \mu\text{A}/\text{mm}$ .

EL intensity after 1h and 24h stress at  $(V_{GStress}, V_{DStress}) = (-1.5 \text{ V}, 15 \text{ V})$  is higher on the edge of gate fingers, as shown in Fig - 12. Furthermore,  $g_{mpeak}$  values after the different steps of the 24h stress are lower by less than 5 % with their initial values before stress as illustrated in Fig - 13.

Thus, no abrupt leakage currents increase or device degradation are identified after 24h stress at  $(V_{GStress}, V_{DStress}) = (-1.5 \text{ V}, 15 \text{ V})$ .

### 1.3. $(V_{GStress}; V_{DStress}) = (-2 \text{ V}, 20 \text{ V})$

Fig - 14 shows gate current variation during 24h stress test at different steps: 1h, 2h, 4h, 8h, 16h and 24h, at  $(V_{GStress}, V_{DStress}) = (-2 \text{ V}, 20 \text{ V})$ .

The gate current, during the stress, becomes more noisy starting from 12h stress, with an abrupt increase from  $4 \mu\text{A}/\text{mm}$  to  $100 \mu\text{A}/\text{mm}$ . This result suggests that the gate current degradation, during the stress, is field driven. EL intensity is uniform along both gate fingers with some regions where EL intensity is higher after 1h stress, as shown in Fig - 15, with EL intensity increasing after 24h stress.

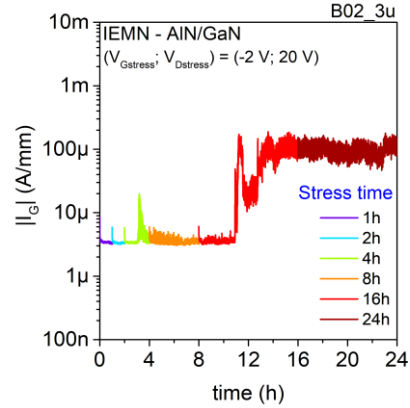


Fig - 14. Variation of gate current during 24h step-stress experiment carried out at  $(V_{GStress}, V_{DStress}) = (-2 \text{ V}, 20 \text{ V})$  with the electrical parameters monitored at 1h, 2h, 4h, 8h, 16h and 24h of AlN/GaN HEMT

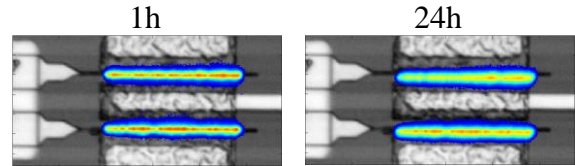


Fig - 15. Electroluminescence emission microscopy images during 24h stress test at two steps: 1h and 24h at  $(V_{GStress}, V_{DStress}) = (-2 \text{ V}, 20 \text{ V})$  of AlN/GaN HEMT.

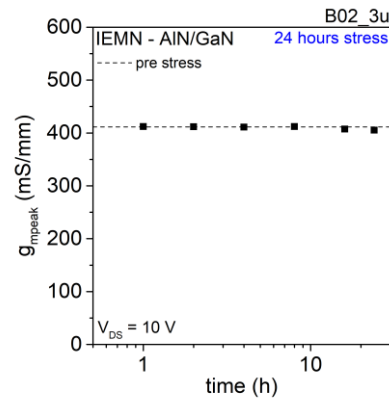


Fig - 16.  $g_{mpeak}$  at  $V_{DS} = 10 \text{ V}$  monitoring during 24h stress carried out at  $(V_{GStress}, V_{DStress}) = (-2 \text{ V}, 20 \text{ V})$  of AlN/GaN HEMT

Moreover,  $g_{mpeak}$  values monitored after the different steps of the 24h stress are superimposed with their initial values before stress as illustrated in Fig - 16.

$$1.4. (V_{GStress}; V_{DStress}) = (-2.5 V, 25 V)$$

Fig - 17 shows the variation of gate current during 24h stress test at different steps: 1h, 2h, 4h, 8h, 16h and 24h, carried out at  $(V_{GStress}, V_{DStress}) = (-2.5 V, 25 V)$  of AlN/GaN HEMT.

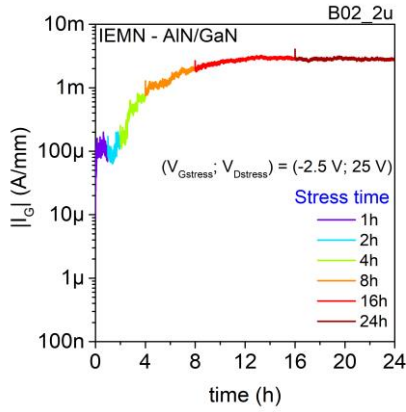


Fig - 17. Variation of gate current during 24h step-stress experiment carried out at  $(V_{GStress}, V_{DStress}) = (-2.5 V, 20 V)$  with the electrical parameters monitored at 1h, 2h, 4h, 8h, 16h and 24h of AlN/GaN HEMT

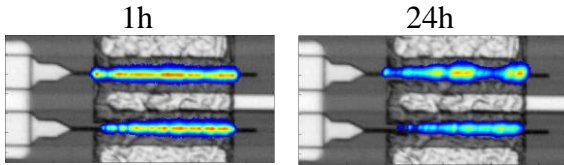


Fig - 18. Electroluminescence emission microscopy images during 24h stress test at two steps: 1h and 24h at  $(V_{GStress}, V_{DStress}) = (-2.5 V, 25 V)$  of AlN/GaN HEMT.

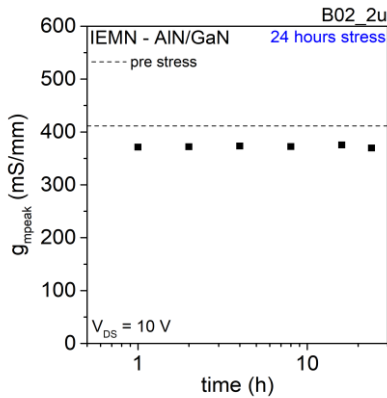


Fig - 19.  $g_{mpeak}$  at  $V_{DS} = 10 V$  monitoring during 24h stress carried out at  $(V_{GStress}, V_{DStress}) = (-2.5 V, 25 V)$  of AlN/GaN HEMT

The gate current at the early hour of stress is at higher value of  $100 \mu A/mm$ , that keeps increasing during the first 12 hours of stress and stabilizes at about  $3 mA/mm$  at the last 12 hours of the stress.

The gate current increase during 24h stress is field dependent and associated with EL hot spots along the gate fingers as shown in Fig - 18.

The monitoring of  $g_{mpeak}$  during 24h stress shows a constant decrease of about 10 % during all the stress, as shown in Fig - 19. The uniform degradation of  $g_{mpeak}$  is not correlated with gate current increase during stress. The latest is related more likely to Schottky contact degradation and not to the AlN/GaN heterostructure.

#### 4. Discussion and conclusions

In this work, we have demonstrated the potential of AlN/GaN HEMTs in terms of linearity and robustness under high electric field up to 25 V. The high performance and reliability are attributed to the high epilayer and processing quality as well as the use of the in-situ SiN passivation enabling in particular an enhancement of the surface robustness.

The degradation of gate current during stress is field dependent related more likely to degradation of Schottky contact or gate/barrier interface.

In spite of adopting only SiN passivation without air bridges or field plates, these devices exhibit state-of-the-art power-added-efficiency of about 50% at 40 GHz, that has been achieved for an output power density in excess of  $3 W/mm$  using gate width of  $2 \times 50 \mu m$  demonstrating the potential of AlN/GaN heterostructure for millimetre wave applications.

#### 5. Acknowledgements

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