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Buffer breakdown in GaN-on-Si HEMTs: a comprehensive study based on a sequential growth experiment

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M. Borga[a]*, M. Meneghini[a], D. Benazzi[a], E. Canato[a], R. Püsche[b], J. Derluyn[b], I. Abid[c], F. Medjdoub[c], G. Meneghesso[a], E. Zanoni[a]

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[a] *Department of Information Engineering, University of Padova, 35131 Padova, Italy*
[b] *EpiGaN, 3500 Hasselt,Belgium*
[c] IEMN-*CNRS, 59652 Villeneuve d'Ascq, France*
**borgamat@dei.unipd.it*

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Abstract

The aim of this work is to investigate the breakdown mechanisms of the layers constituting the vertical buffer of GaN-on-Si HEMTs; in addition, for the first time we demonstrate that the breakdown field of the AlN nucleation layer grown on a silicon substrate is equal to 3.2 MV/cm and evaluate its temperature dependence.
To this aim, three samples, obtained by stopping the epitaxial growth of a GaN on Silicon stack at different steps, are studied and compared: Si/AlN, Si/AlN/AlGaN, full vertical stack up to the Carbon doped buffer layer.
The current-voltage (IV) characterizations performed at both room temperature and high temperature show that: (i) the defectiveness of the AlN nucleation layer is the root cause of the leakage through an AlN/Silicon junction, and causes the vertical I-V characteristics to have a high device-to-device variability; (ii) the first AlGaN layer grown over the AlN, beside improving the breakdown voltage of the whole structure, causes the leakage current to be more stable and uniform across the sample area; (iii) a thick strain-relief stack and a carbon-doped GaN buffer enhance the breakdown voltage up to more than 750V at 170°C, and guarantee a remarkably low device-to-device variability. Furthermore, a set of constant voltage stress on the Si/AlN sample demonstrate that the aluminum nitride layer shows a time dependent breakdown, with Weibull-distributed failures and a shape factor greater than 1, in line with the percolation model.

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1. Introduction

Gallium Nitride (GaN) based transistors are promising devices in the voltage range between 200V and 1200V [1], being suitable for the next generation of switching power converters. Thanks to the high breakdown field of GaN, which is greater than 3 MV/cm [2], the devices can withstand high voltages, showing an excellent robustness toward OFF-state condition. Moreover, growing the GaN material system over a silicon substrate, improve the process yield and reduces the costs of the final device.

The optimization of the GaN-on-Silicon technology is crucial to improve the efficiency of power High Electron Mobility Transistors (HEMTs), by reducing the leakage losses between drain and substrate when the devices are kept in a high-voltage OFF-state condition. Different approaches have been exploited in order to improve the vertical robustness of the devices, such as a partial removal of the silicon substrate in the drain-gate region [3][4], or a local doping of the silicon substrate below the drain contact [5]. Nevertheless, we recently presented a study [6] on the failure statistics, demonstrating that the failure of a complete GaN-on-Si structure show a time dependent breakdown, with Weibull distributed time to failure. Previous works in literature studied the conduction mechanisms though the vertical stack, showing that the vertical leakage current is determined by a Space Charge Limited conduction through trap states within the materials [7][8]. In addition, Li at all [9] presented and extensive analysis on the conduction mechanisms through the nucleation layer grown on silicon, showing that the defects, deep levels, and interfacial states, play a key role in the current conduction through a defective AlN layer.

The aim of this paper is to investigate the breakdown mechanisms in the vertical buffer used for the fabrication of GaN-on-Si HEMTs. To this aim, we carried out a **buffer-decomposition**

* Corresponding author. borgamat@dei.unipd.it
Tel: +39 (049) 827 7625

experiment: three different wafers were fabricated, where the epitaxial growth was interrupted at different stages. In this way we were able to separately evaluate the role of the AlN nucleation layer, of the AlGaN buffer, and of the vertical stack up to the C-doped layer on the conduction and breakdown processes. We also show **the temperature dependence** of the current through the tested structures. Moreover, focusing on the Silicon-AlN layer, we evaluate **for the first time the breakdown field of the AlN nucleation layer** grown on a silicon substrate, and its dependency on the ambient temperature. Finally, a set of constant voltage stresses suggest that the **failures of the AlN layer are Weibull-distributed**.

2. Experimental details

In this work three different samples were tested and studied. The first sample consists of a 200nm thick layer of AlN epitaxially grown on a conductive $1 \cdot 10^{19}$ cm^{-3} boron-doped silicon substrate; in the next paragraphs this will be referred as Sample A. The second sample, Sample B, has a similar structure to sample A, but over the thin AlN layer, an additional 350nm thick $Al_{70}Ga_{30}N$ layer is grown. Lastly, sample C is made up of a p-doped silicon substrate, a 200nm AlN layer, a 2350nm thick multi-layer AlGaN backbarrier, and a 2450nm thick carbon doped GaN layer; the carbon doping concentration is $2 \cdot 10^{19}$ cm^{-3}. The ohmic Ti(40nm)/Au(20nm) contacts were defined by photolithography; 95x95 µm patterns have been used for the electrical measurements. The structures details are summarized in Figure 1, while a schematic representation of the band diagrams at zero-bias of the three described structures are shown in Figure 2.

The voltage-current characterizations were carried out with a high voltage parameter analyzer Keysight B1505A, whose high voltage (HV) Source Measurement Unit (SMU) is limited at ±3kV, 4mA. The breakdown voltage is extrapolated with a failure-current level of 8mA.

The constant current stresses were performed by means of a Keithley 2410, a high voltage source meter limited at 1.1kV, 20mA. In order to determine the time to failure of a device, a threshold current level of 1µA was set.

The high temperature measurements were carried out heating the samples with a ceramic heater controlled by a Thorlabs TC 200 heater controller.

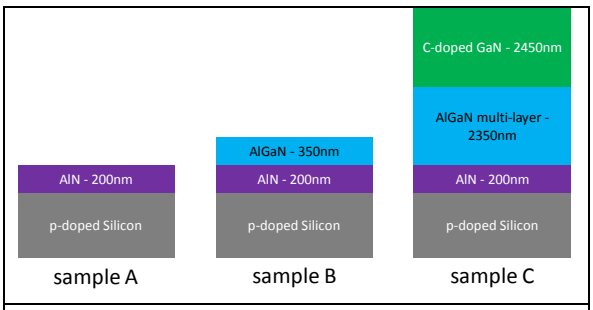

Figure 1: schematic representation of the three tested samples. Sample A (left) consists of 200nm thick layer of AlN grown on a conductive ($1 \cdot 10^{19}$ cm^{-3} boron-doped) silicon substrate. Sample B (center) has an additional 350nm thick AlGaN layer. Sample C (right), over the AlN nucleation layer, has a 2350nm thick strain-relief layer and a 2450nm carbon doped ($2 \cdot 10^{19}$ cm^{-3}) GaN layer.

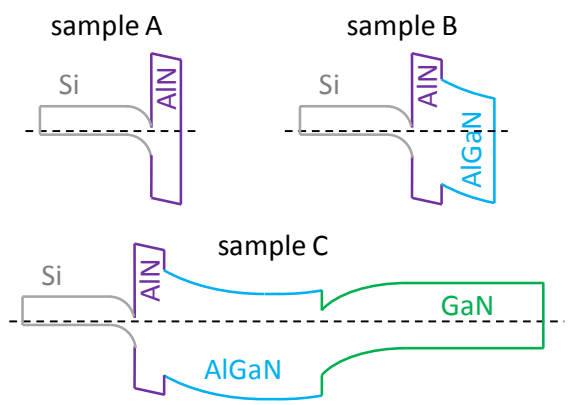

Figure 2: schematic equilibrium band diagram of the studied samples: (top-left) sample A, (top-right) sample B and (bottom) sample C

3. Results and discussion

The discussion is split in two sections. The first one addresses the comparison of the three samples, while the second one concerned the sample A, and is focused on the failure statistics of the AlN layer.

3.1 Current-Voltage characterization

Several devices on each sample were submitted to a voltage sweep on the ohmic pad, while the substrate was grounded. These measurements have been carried out at 30°C, 100°C, and 170°C. The applied voltage was swept from 0V up to the failure of the device, so that both the leakage current behavior and the failure voltage were monitored on a single measurement as a function of the ambient temperature.

Sample A consists of just a thin AlN layer

epitaxially grown over a conductive p-doped silicon substrate. The AlN layer, beside avoiding the Ga-Si eutectic reaction, act as a base layer for the growth of the subsequent (Al)GaN layers. Due to the remarkably high lattice mismatch between the Aluminum Nitride and the Silicon as well as the low surface mobility of Al species during the epitaxial growth, the AlN layer has a high defectivity. This results in both an unstable current-voltage characteristic of the devices and a high device-to-device variability (Figure 3(a)). The current behavior shows a low dependency on the ambient temperature, since the current mostly depends on the local defectivity of the material.

Due to the conductive nature of the silicon substrate, we can suppose that all the applied voltage drops on the AlN layer. Moreover, the AlN can be considered as an insulating material, meaning that the electric field through it is almost constant within the whole thickness. These two approximations allow us to estimate the maximum electric filed that cause the breakdown of the AlN layer by calculating the ratio between the failure voltage and the thickness of the AlN layer (Figure 3(b)). At 30°C the mean breakdown electric field of the AlN layer results 3.2 MV/cm, and it drops to 2.78 MV/cm at 170°C. These breakdown filed values are compatible with previous works in literature [10][11].

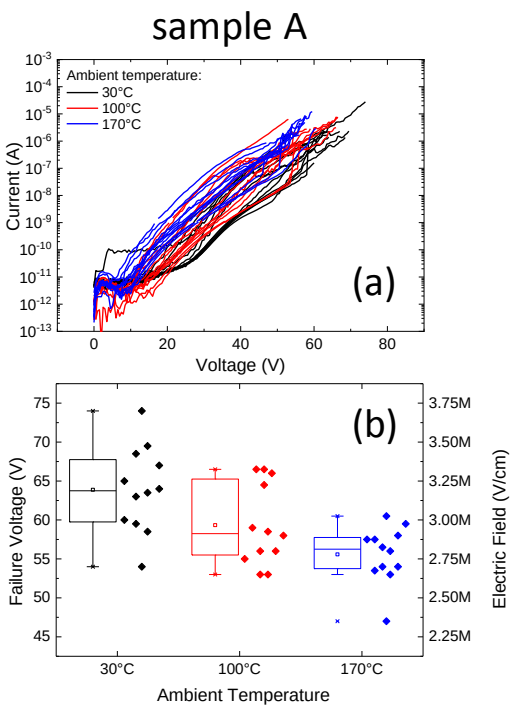

Figure 3: (a) current-voltage characteristics of the devices on sample A at different ambient temperature (i.e. 30°C, 100°C and 170°C). (b) box chart of the failure voltages of the tested device of sample A. Right y-axis shows the corresponding electric field.

The sample B has a thicker structure with respect to the sample A, and over the AlN nucleation layer, a first strain relief 350nm thick AlGaN layer was grown. Usually, in a GaN-on-Si stack, several AlGaN layers are interposed between the nucleation layer and the GaN layer; the aim of these layers is to generate compressive stress to compensate for the thermal-mismatch-induced tensile stress that is generated during cool-down. At the same time, the strain fields at the layer transitions cause some of the threading dislocations to bend and thereby limit the density of the dislocations that propagate from the defective nucleation layer toward the subsequent layers. This guarantees a reduced defect and trap densities close to the active region of the final devices.

By comparing the current-voltage characteristics of the devices grown on sample B (Figure 4(a)) with those grown on sample A, it is clear the role of the AlGaN layer: the current-voltage curves of sample B results more stable, and the device-to-device variability is considerably reduced. Moreover, due to the higher total thickness of the epitaxial layers, the breakdown voltage of the devices on sample B is considerably higher with respect to the failure voltage of the devices of sample A. In the case of sample B, the average electric field at the breakdown was calculated as the ratio of the failure voltage and the total thickness of the AlN and the AlGaN layers, and it results 2.58 MV/cm at 30°C. This calculation is a strong approximation, since a non-uniform partitioning of the applied voltage is present. The failure electric field of sample B is lower than the one calculated in sample A, meaning that the electric field is not uniformly distributed within the AlN/AlGaN stack. This can be ascribed either to the different dielectric constant and the different conductivity of the two materials; moreover, also the piezoelectric charge may play a role in the voltage partitioning within the epitaxial layers. As on sample A, the higher ambient temperature results in a lowered breakdown voltage (Figure 4(b)).

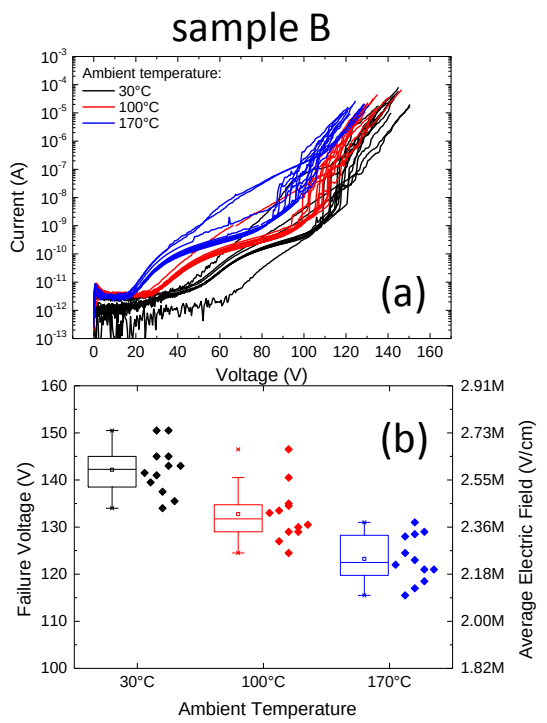

Figure 4: (a) current-voltage characteristics of the devices on sample B at different ambient temperature (i.e. 30°C, 100°C and 170°C). (b) box chart of the failure voltages of the tested device of sample B. Right y-axis shows the corresponding electric field.

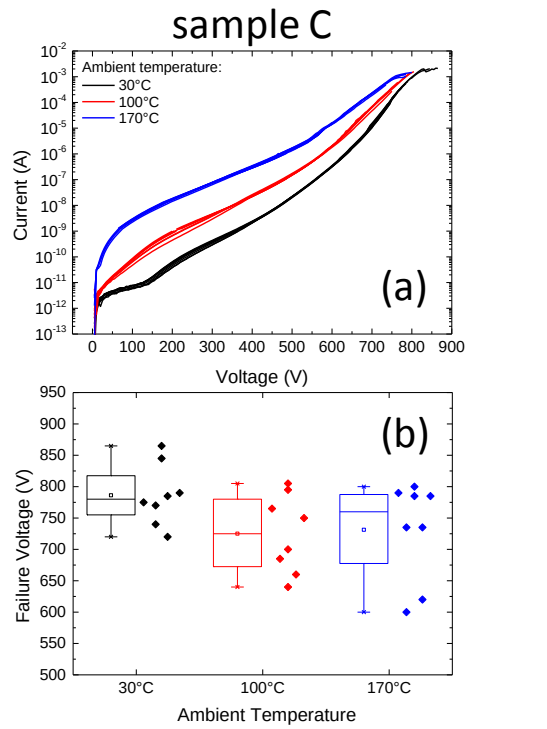

Figure 5: (a) current-voltage characteristics of the devices on sample C at different ambient temperature (i.e. 30°C, 100°C and 170°C). (b) box chart of the failure voltages of the tested device of sample C.

The third tested sample, sample C, consists of the AlN nucleation layer grown on a silicon substrate, a complete stack of AlGaN strain relief layers, which prevents the dislocation to propagate through the epitaxial stack, and a 2450nm thick carbon doped GaN layer. The aim of the C-doped layer is to prevent punch-through effect on the final devices, and to reduce the intrinsic conductivity of the GaN. Several works in literature show that this layer plays a crucial role not only in the vertical robustness but also in the stability of the devices under dynamic bias conditions.

The current-voltage characteristics of the sample C are shown in Figure 5(a). Thanks to the thick epitaxial layer and thanks to the high material quality of the carbon doped GaN layer, Figure 5(b) shows that the breakdown voltage is considerably improved (higher than 700V), and there is a remarkably low variability among the tested devices. The ambient temperature has a clear impact on the current through the structure, causing this latter to be higher at higher temperatures. This can be explained either by the improved thermal generation of free charges within the semiconductors, and by the enhanced conductivity of the defective material under high temperature and high electric field conditions.

3.2 Constant voltage stress SAMPLE A

This section focuses on the failure mechanisms of the AlN layer grown on a silicon substrate. The leakage characterizations at different ambient temperatures show a very unstable behavior of the current with the applied voltage, thus indicating the high defectiveness of the material. Studying the failure statistic of this sample allow us to better understand if the defects play a role in the breakdown of the devices.

A set of constant voltage stresses were carried out by biasing at 50V the ohmic contact on top of the AlN layer and by keeping the silicon substrate grounded. Due to the high conductivity of the silicon substrate, all the applied voltage drops on the AlN layer, thus allowing the study of its failure statistic. During these voltage stresses the ambient temperature was 30°C.

In Figure 6(a) one can observe the noisy behavior of the current through the AlN layer over the time; this can be ascribed to the defectiveness of the material, which results in a dynamic formation and disruption of leakage paths. Once a set of defects is aligned, a conductive path gets formed between

the ohmic contact and the silicon substrate, the device shows a catastrophic breakdown. This failure mechanisms was previously defined as percolation [12], and it is typical of the breakdown of the dielectric materials.

By plotting the time to failure of a set of 10 devices grown on sample A on a Weibull plot (Figure 6(b)), it can be noticed that the points perfectly align, meaning that the failure are Weibull distributed. The beta parameter value of the distribution extracted with 99% confidential level is 1.05, meaning that the failures are caused by a wear-out process that degrades the devices. The alpha parameter, which represent the time at which the 63.2% of the devices is expected to be failed, is 189 s for the adopted stress condition. The Weibull distribution of the failures agrees with the percolation model, confirming the hypothesis made on the failure mechanism of the AlN layer.

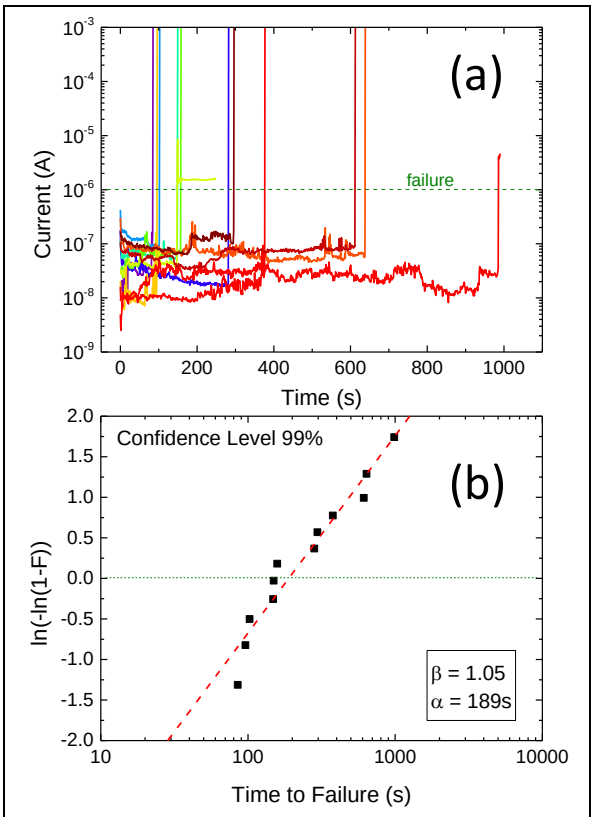

Figure 6: (a) current behavior during the constant voltage stress at 50V of sample A. (b) Weibull plot of the failed devices submitted to the constant voltage stress at 50V.

Conclusions

In this work we studied the electrical behavior of three different structures obtained by stopping the epitaxial growth of a standard GaN-on-Silicon process, showing that both the thickness and the composition of the epitaxial stack, beside enhancing the breakdown voltage, improve the material quality by limiting the propagation of defects and dislocations. Furthermore, for the first time we evaluated the critical electric of the AlN nucleation layer grown on a silicon substrate, which is equal to 3.2MV/cm. In addition, focusing on sample A, we showed that the nucleation layer shows a wear-out process when submitted to a constant voltage stress, with Weibull-distributed times to failure, thus suggesting that a percolation process is the failure mechanism of the aluminum nitride layer.

Acknowledgement

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