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ABSTRACT

The development of quantum electronic devices operating below a few Kelvin degrees is raising the demand for cryogenic complementary metal-oxide-semiconductor electronics (CMOS) to be used as *in situ* classical control/readout circuitry. Having a minimal spatial separation between quantum and classical hardware is necessary to limit the electrical wiring to room temperature and the associated heat load and parasitic capacitances. Here, we report prototypical demonstrations of hybrid circuits combining silicon quantum dot devices and a classical transimpedance amplifier, which is characterized and then used to measure the current through the quantum dots. The two devices are positioned next to each other at 4.2 K to assess the use of the cryogenic transimpedance amplifier with respect to a room-temperature transimpedance amplifier. A quantum device built on the same substrate as the transimpedance amplifier is characterized down to 10 mK. The transimpedance amplifier is based on commercial 28 nm fully depleted Silicon-on-insulator (FDSOI) CMOS. It consists of a two-stage Miller-compensated operational amplifier with a 10 M Ω polysilicon feedback resistor, yielding a gain of 1.1×10^7 V/A. We show that the transimpedance amplifier operates at 10 mK with only 1 μ W of power consumption, low enough to prevent heating. It exhibits linear response up to ± 40 nA and a measurement bandwidth of 2.6 kHz, which could be extended to about 200 kHz by design optimization. The realization of custom-made electronics in FDSOI technology for cryogenic operation at any temperature will improve measurement speed and quality inside cryostats with higher bandwidth, lower noise, and higher signal-to-noise ratio.

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I. INTRODUCTION

Massive worldwide research is currently focused on exploring disruptive technologies based on quantum properties of matter. Quantum computing is certainly the most ambitious goal. Its building blocks, the so-called qubits, encoding elementary bits of quantum information, must have long quantum coherence and be susceptible to large-scale integration. Superconducting¹ and semiconductor-based² qubits are among the most promising candidates since they benefit from a low footprint and a good controllability.

The coherent control of such qubits requires the application of microwave pulses typically generated by room temperature sources and conveyed through coaxial lines running down to the qubit chip. The latter is thermally anchored to the coldest stage of a cryostat, which is usually well below 1 K. On the other hand, the readout of a qubit requires measuring small signals coming from the device and carried up to room temperature via meter-long lines and low-noise

amplifiers at intermediate temperatures (usually around a few degrees Kelvin).

A number of control and readout lines proportionally increasing with the number of qubits³ would not be viable due to the thermal load of the wiring and the limited available space at cryogenic temperatures. A way around this problem may come from the use of cryogenic electronics,⁴ such as low-temperature multiplexers in combination with broad-band low-temperature amplifiers positioned as close as possible to the quantum chip in order to reduce parasitic capacitance. Efficient circuits involving High Electron Mobility Transistors (HEMT) have been realized down to 1 K for, e.g., GHz oscillators,⁵ low-noise amplifiers,⁶ and voltage references.⁷

Silicon-based quantum dots attract attention since they can leverage the well-established semiconductor technology. In this case, qubits are encoded in the spin degree of freedom of confined electrons. Current sensing of high-impedance quantum-dot structures is done

using a current-to-voltage amplifier, also known as a transimpedance amplifier (TIA). At low temperatures, electron transport measurements can give access to the charge and spin properties of a quantum dot.⁸ For a TIA placed at room temperature, the current measurement suffers from large access-cable capacitance (typically a few hundred pF) forming an RC network with the high-impedance device ($>1\text{ M}\Omega$) limiting the maximal measurement rate to typically $\sim 1\text{ kHz}$. The only way to reduce these effects is by reducing the cable length between amplifier and device either by developing a more compact fridge design or by using a cryogenic amplifier placed at the cold stage, as close as possible to the device.

In Fig. 1, we schematically show the advantages of placing the TIA at low temperature close to the Device Under Test (DUT) by comparing a measuring configuration with the TIA at room temperature to that at temperatures $\leq 4.2\text{ K}$. The short-distance connection between TIA and DUT will reduce leakage currents because of reduced cable length and allow the detection of the smallest features. The TIA at low temperatures would have intrinsically a lower thermal noise. The dissipation of the TIA should be compatible with the cooling capacity of the low-temperature stage. Ultimately, low-temperature TIAs combined with multiplexing circuits⁹ will drastically improve the cycling rate of measurement.

To benefit from the higher cooling power, cryogenic TIAs dissipating mW power are placed at 4.2 K. For the investigated TIAs based on discrete Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs),¹⁰ and bulk CMOS transistors,¹¹ the measurement rate improves significantly up to 250 kHz. Yet, such arrangements still use cables of tens of centimeters for thermal isolation between the sub-K and 4.2 K stages.

Further improvements in the TIA performance require amplifiers to operate at sub-K temperatures¹² assembled with a quantum device

a few millimeters away. In such a scheme, it becomes primordial to operate at a low power consumption (typically smaller than tens of μW) to avoid thermal destruction of quantum effects in quantum dots.¹³

Complete integration at μm distance between amplifier and quantum device can be reached by producing the classical electrical circuit and the quantum device in the same semiconductor technology.¹⁴ The recently developed CMOS spin qubit made on an industrial foundry for 300-mm wafers¹⁵ would open this route toward on-chip integrated electronics for qubit control and readout. The measurement throughput can be increased by parallel processing requiring low-footprint identical amplifiers that motivated the use of industrial state-of-the-art silicon-based CMOS technologies for the development of cryogenic electronic circuits.

Majority charge-carrier freeze out in CMOS bulk transistors leads to non-ideal behavior such as kink effects and hysteresis in current-voltage characteristics,¹⁶ thereby degrading the circuit performance. The newly developed 28-nm Fully-Depleted Silicon-On-Insulator (FDSOI) technology has shown itself to be less sensitive to carrier freeze out.¹⁷ The additional oxide buried beneath the silicon conduction channel enables back biasing to compensate for the increased threshold gate-voltage at cryogenic temperatures.¹⁸

In this article, we present the electrical characteristics of passive elements and individual transistors of the industrial 28-nm FDSOI technology in a large temperature range, going from room temperature to sub-Kelvin temperature. The relevant parameters such as threshold gate-voltage, transconductance, and conductance, were extracted for the transistors. These characteristics were used for the design optimization of a cryogenic TIA based on an operational amplifier (OP-AMP) with on-chip resistive feedback to measure the current through a nearby-placed high-impedance quantum-dot device as a

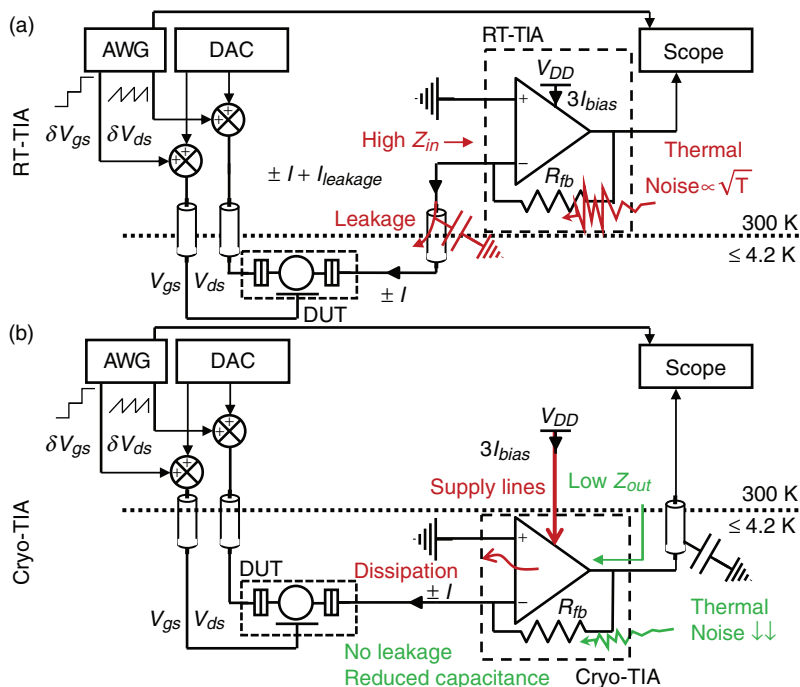


FIG. 1. Schematics of the TIA amplifier for high-speed current measurement of a high-impedance quantum dot (Device Under Test, DUT). The comparison between (a) 300 and (b) $\leq 4.2\text{ K}$ highlights the issues of leakage current, thermal noise, dissipation, and trace impedance. It is clearly visible that the short-distance connection between TIA and DUT will reduce leakage currents because of reduced cable length and allow the detection of the smallest features. The TIA at low temperatures has intrinsically a lower thermal noise.

function of varying gate and bias voltages. The TIA is made of a two-stage Miller-compensated operational amplifier dissipating only $1 \mu\text{W}$, resulting in a negligible heat load compared to the usually available cooling power of a $^3\text{He}/^4\text{He}$ dilution refrigerator (typical cooling power $\approx 100 \mu\text{W}$ at 100 mK).

We systematically investigate the temperature dependence of gain, gain-bandwidth product, and noise between 0.25 and 300 K. To demonstrate the low-temperature quantum-classical device, a nanometer-sized quantum-dot device was wired-bonded to the TIA after positioning the respective chips at a few millimeters distance. The configuration with the TIA at cryogenic temperatures is compared with the configuration with the TIA outside the cryostat at room temperature linked to the quantum device by meter-scale wiring. We show that the cryogenic configuration is less prone to current leakage and achieves a better bandwidth. Finally, we use the cryo-TIA to characterize a quantum device made in the same silicon substrate following the founder design rules, demonstrating the full capabilities of cryo-TIAs and FDSOI CMOS technologies down to 10 mK. Further improvements are identified to increase the performance of the cryogenic TIA with respect to bandwidth for the same power consumption in future designs.

II. FDSOI CHARACTERIZATION

The 28-nm FDSOI technology has many advantages for the development of cryogenic electronics for quantum experiments that require high-speed and potentially large-scale integration. The use of an undoped fully depleted transistor channel significantly lowers the variability. The FDSOI technology at 4.2 K remains competitive with the mismatch of bulk technology at room temperature.^{19,20} The thin gate oxide (1.1 nm) ensures a very good gate-voltage control of the channel allowing low-power operation with a supply voltage V_{DD} of only 1 V. The 7 nm-thick silicon channel isolated from the substrate via the silicon-on-insulator technology prevents the appearance of bulk-like regions under high source-drain voltage V_{ds} , which are subjected to freeze out of charge carriers. The freeze out effect would lead to kink effects and hysteresis at cryogenic temperatures, degrading the analog performance of MOSFETs. The lower capacitance due to reduced transistor size with minimal gate-length of 28 nm reduces the dynamic power consumption and increases the maximal frequency of operation (up to 350 GHz at 77 K²¹). To fully exploit the FDSOI potential for cryogenic circuitry design, we characterized integrated resistors down to 4.2 K and transistors down to 0.25 K to extract important low-frequency quantities as sheet-resistivity, threshold voltage, transconductance, and conductance.

Integrated resistors are important to implement feedback and achieve stability in closed-loop amplifier systems. The resistance of weakly disordered, highly doped metallic resistors realized from silicon, silicided silicon, and silicided polysilicon decreases from room temperature down to liquid helium temperature because of reduced phonon scattering. The relative sheet resistance variation down to 4.2 K is -25% for silicon and -37% for silicided silicon and silicided polysilicon (see Fig. S1 in the [supplementary material](#)). The resulting low value of the sheet resistance at 4.2 K of $400 \Omega/\square$ for silicided resistors and $1.3 \text{ k}\Omega/\square$ for non-silicided silicon resistors is not suitable for the fabrication of $\text{M}\Omega$ -range resistors generally used for high-gain TIA. The preferred option is to use polysilicon resistors that only show a 4% variation from 300 to 4.2 K and a high sheet-resistivity of

about $20 \text{ k}\Omega/\square$ at 4.2 K due to their highly disordered crystalline structure.

Interdigitated Metal-Oxide-Metal (MOM) capacitors on five metal levels are chosen for their high capacitance density ($6.45 \text{ fF}/\mu\text{m}^2$) with an expected weak dependence on temperature.²²

MOSFETs are characterized by the relation between the current flowing from drain to source I_{ds} , the gate-source voltage V_{gs} , and drain-source voltage V_{ds} . Transistors operate in the saturation regime in most analog circuits (e.g., amplifiers) for which V_{gs} exceeds the threshold voltage V_{th} and V_{ds} is greater than $V_{gs} - V_{th}$. In such conditions, MOSFETs behave as non-ideal voltage-controlled current sources characterized by a voltage-to-current gain, called the transconductance, $g_m = \partial I_{ds} / \partial V_{gs}$, and a parallel resistance, called the conductance, $g_{ds} = \partial I_{ds} / \partial V_{ds}$. For thin-oxide regular threshold-voltage (RVT), $V_{th} \approx 0.6 \text{ V}$ at 4.2 K transistors, the transconductance g_m is extracted from DC-voltage characteristics at 300, 4.2, and 0.25 K for $|V_{gs} - V_{th}| = 200 \text{ mV}$ and $V_{ds} = 0.9 \text{ V}$. The conductance g_{ds} is extracted from the characteristics for $|V_{gs}| = |V_{ds}| = 0.9 \text{ V}$. The intrinsic voltage gain $A_V = g_m / g_{ds}$ is shown in Fig. 2 for transistors of gate-width 0.08, 0.32, and $1 \mu\text{m}$ as a function of gate-length L . A_V is weakly dependent on the gate width and corresponds to the maximum amplification gain from gate to drain-voltage. For both NMOS and PMOS transistors, A_V increases for decreasing temperature from 300 to 4.2 K, mostly due to the increase in g_m with a roughly constant g_{ds} . For the plotted data in Fig. 2 at 0.25 K, no further change in the MOSFETs DC characteristics is observed compared to 4.2 K. This low-temperature saturation of the electrical transistor characteristics can be explained by considering mobility saturation, band edge broadening,²³ and incomplete ionization effects.²⁴

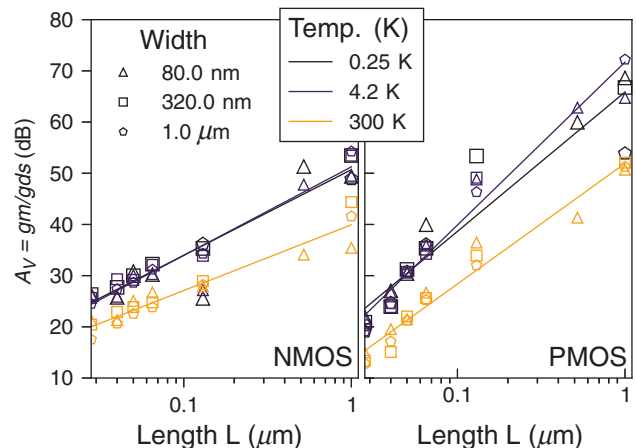


FIG. 2. Intrinsic voltage gain $A_V = g_m/g_{ds}$ for NMOS and PMOS transistors of different gate-widths W at 0.25, 4.2, and 300 K as a function of gate-length L . Straight lines are linear fits for all data points at the specified temperature. In these plots it is visible that A_V is weakly dependent on the gate width and corresponds to the maximum amplification gain from gate to drain-voltage. It is also visible that, for NMOS and PMOS transistors, respectively, A_V increases for decreasing temperatures from 300 to 4.2 K, mostly due to the increase in g_m with roughly constant g_{ds} . For the plotted data at 0.25 K, no changes in the MOSFETs DC characteristics is observed compared to 4.2 K. This low-temperature saturation of the electrical transistor characteristics can be explained by considering mobility saturation, band edge broadening, and incomplete ionization effects respectively.

As foundry models are not available at cryogenic temperatures, we fitted an FDSOI compact model²⁵ to a large set of DC experimental data of MOSFETs in saturation at 4.2 K.¹⁹

III. CRYOGENIC AMPLIFIER

A. TIA Design

Using the above-given characterizations of the 28-nm FDSOI technology, we designed a transimpedance amplifier (TIA) composed of an operational amplifier (OP-AMP) with a resistive feedback. The OP-AMP is made of two amplifying stages of total open-loop gain $G_{ol} = A_1 A_2$ where A_1 (respectively, A_2) is the voltage gain A_V of the first (respectively, the second) stage corresponding to the intrinsic voltage gain of transistors N1, N2 (respectively, P1) indicated in Table I. The feedback polysilicon resistor R_{fb} (150-nm width, 31.5- μm length) sets the desired current-to-voltage closed-loop gain $Z_T \approx 11 \times 10^6 \text{ V/A}$ of the TIA. The NMOS current sources shown (Fig. 3, bottom MOSFETs) bias the two stages by copying the reference bias current I_{bias} . The first stage (respectively, the second stage with wider transistors) is biased with I_{bias} (respectively, $2I_{bias}$). The power consumption P_{DD} of the TIA that needs to be compensated by the cooling capacity of the fridge is $P_{DD} = 3I_{bias} V_{DD}$ with V_{DD} the power supply level (1 V).

From room temperature simulations, the OP-AMP operates for I_{bias} from 10 nA to 10 μA leading to a power consumption from 0.03 to 30 μW . At low temperatures, the MOSFET temperature is higher than the fridge temperature due to self-heating. From self-heating study at 4.2 K,²⁶ the computed temperature increase would be 2 mK at 0.1 μW (respectively, 1.8 K at 100 μW) if all power were consumed in only one device. However, only N1 is directly connected to the quantum device and consumes only one-ninth of the power dissipated within the TIA (assuming a typical value of $V_{ds} = V_{DD}/3$). In the mid-range at 1 μW , heating from N1 would then lead to only 2 mK higher temperature. At sub-Kelvin temperatures, assuming the same saturating trend as observed in,²⁶ the temperature increase will remain identical with a negligible heating of electron temperature.

The dominant pole in the frequency response for V_{out}/V_{in} of the OP-AMP corresponds to the Miller capacitance of the second stage $(1 + A_2)C_s$ and the output impedance of the first stage $R_{out,1}$ leading to a cutoff frequency $f_{op} = 1/2\pi R_{out,1} C_s (1 + A_2)$ where C_s is the

TABLE I. Single MOSFET properties from foundry models at 300 K and custom models at 4.2 K for a power consumption $P_{DD} = 1 \mu\text{W}$. Cryogenic models are obtained by fitting a UTISOI model²⁵ on cryogenic transistor data from¹⁹ in saturation.

MOSFETs	L (μm)	W (μm)	T (K)	A_V (dB)	g_m (μs)	g_{ds} (ns)	g_m/I_{ds} (V^{-1})
N1, N2	0.6	20	300	37	5.8	1.6	35
			4.2	47	12	—	72
N0, N3	0.3	20	300	—	12	13	35
			4.2	—	21	—	61
N4	0.3	40	300	—	23	19	35
			4.2	—	21	—	32
P1	0.4	40	300	43	22	16	33
			4.2	59	15	—	23
P2, P3	0.4	20	300	—	5.6	4.4	34
			4.2	—	8.2	—	50

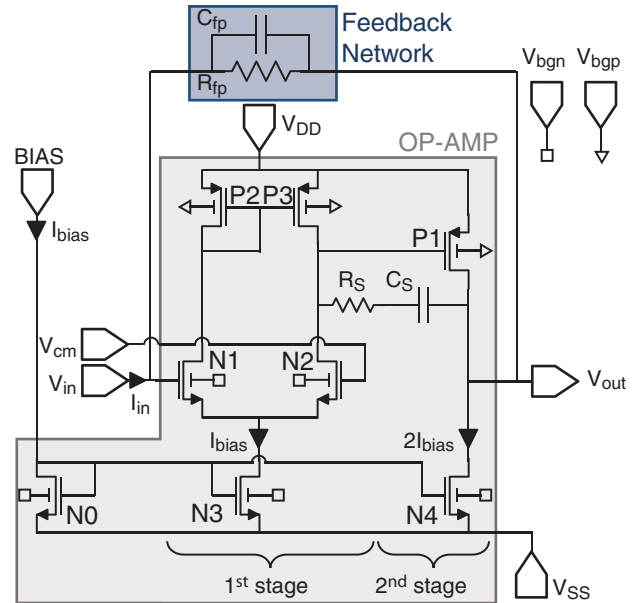


FIG. 3. The Miller-compensated two-stage topology of the OP-AMP mounted as TIA with the feedback network. The expected TIA gain is $G = V_{out}/I_{in} = R_{fb}$. The common-mode V_{cm} is set to 0.65 V. R_s and C_s ensure the stability of the two stages. In this work, a polysilicon resistor R_s in series with a MOM capacitor C_s ensures the two-stage stability with a phase margin above 75° from 30 nW to 30 μW . The MOM capacitor C_{fb} in parallel with R_{fb} ensures the stability in closed-loop mode with interconnection capacitance C_{in} present at the input V_{in} .

added compensation capacitance, and $R_{out,1}$ is the first-stage output impedance (cf. Table II). This leads to a predicted gain-bandwidth (GBW) given by $f_{op} G_{ol}$ at 1 μW of 32 kHz at 300 K (see Table II), which would be the maximal TIA bandwidth when measuring an infinite impedance current source (without C_{fb}). Assuming that N1 and N2 mainly contribute to A_1 and $A_2 \gg 1$, this expression reduces to

TABLE II. Predicted OP-AMP and TIA specifications at $P_{DD} = 1 \mu\text{W}$ obtained from the MOSFETs properties (in Table I) and passive elements at 4.2 and 300 K (see Fig S1 in the supplementary material). G_{ol} , $R_{out,i}$, GBW are respectively the open-loop gain, the output impedance of the i -th stage and the gain-bandwidth product of the OP-AMP. R_{out} is the output impedance of the TIA. Gain and range of linear response are estimated for the TIA.

Circuit	Property	Temperature		Unit
		4.2	300	
OP-AMP	G_{ol}	106*	114	dB
	$R_{out,1}$	—	167	M Ω
	$R_{out,2}$	—	29	M Ω
	GBW	66	32	kHz
TIA	Gain	10.6	10.6	10^6 V/A
	Range	± 47	± 47	nA
	R_{out}	298 ^a	642	Ω
	R_{fb}/C_{fb}	4.29	4.29	kHz

^aEstimated from A_V of N1, N2, and P1 (Table I).

$GBW = g_m^{N1,N2}/2\pi C_s$ with less than 1% error in the predictions at room temperature. This expression can then be used at 4.2 K where the conductance g_{ds} is not reliably known and predicts a GBW of 66 kHz. The second pole corresponds to the TIA output impedance R_{out} in parallel with the large access capacitance $C_{cables} \simeq 100$ pF. The associated cutoff is shifted to high frequency (>1 MHz) thanks to the low output impedance $R_{out} \simeq 1/A_1 g_m^{P1}$ induced by the TIA feedback (see Table II).

The AC stability analysis was performed with foundry models by extrapolating results down to cryogenic temperatures. A polysilicon resistor $R_s = 10.6$ k Ω in series with a MOM capacitor $C_s = 29.1$ pF (see Fig. 3) ensures the two-stage stability with a phase margin above 75° from 30 nW to 30 μ W [see Figs. S3 and S4(a) in the supplementary material]. The MOM capacitor $C_{fb} = 3.2$ pF in parallel with R_{fb} ensures the stability in closed-loop mode with interconnection capacitance $C_{in} \simeq 3$ pF present at the input V_{in} . The RC feedback network sets the maximal TIA bandwidth $f_{fb} = 1/2\pi R_{fb} C_{fb} = 4.29$ kHz (see Table II) regardless of the measured device impedance R_m as long as $R_m > R_{fb} \times f_{fb}/GBW \simeq 715$ k Ω .

In the absence of prior knowledge of noise at cryogenic temperature for this technology, no further optimizations have been performed in the design procedure. With room temperature models, the OP-AMP output-noise is limited by the flicker noise in the first stage that is amplified by the second. P2 and P3 represent 64% of the output noise, contributing 98% together with N1 and N2. The output noise generates a voltage noise directly on the measured device. This kick-back voltage noise is independent of the dot impedance and is estimated to be equal to $350 \mu V_{rms}$ at 300 K integrated from 1 Hz to 1 GHz. These random voltage fluctuations are smaller than usual Coulomb-diamonds features in V_{ds} but remain non-negligible and could result in potential electron heating. However, due to the presence of capacitance at the TIA input from parasitics (bonding pads, interconnections, etc.) and at the TIA output from cables, the kick-back noise reduces to $32 \mu V_{rms}$ with 3 pF at the input and 100 pF at the output from cables (see Fig. S5 in the supplementary material). The frequency-integrated kick-back noise is dominated by high-frequency thermal noise expected to decrease at cryogenic temperatures.

All transistors are placed in a triple well structure (N-well for PMOS and P-well for NMOS, the latter being isolated from the substrate by a surrounding N-well). This well structure allows for independent back-gate biasing of NMOS (respectively, PMOS) at voltages V_{bgn} (respectively, V_{bgp}). In this article, back-gate biasing voltages are kept at 0 V.

B. TIA Characterization

1. Experimental setup

The TIA chip is wire-bonded onto a 48-pin Dual-In-Line (DIL) package held in a socket soldered to a 4-layer PCB with a continuous ground plane and via-free routing to a 51-pin micro-D connector toward room temperature electrical equipment [see Fig. 4(a)]. Supply lines for the circuit (V_{DD} and V_{SS} shown in Fig. 3) are decoupled from potential environmental noise to ensure stable voltage levels. For this purpose, three capacitors are connected in parallel to the supply lines: two tantalum capacitors of 10 and 1 μ F (decrease by 30% at 4.2 K) and

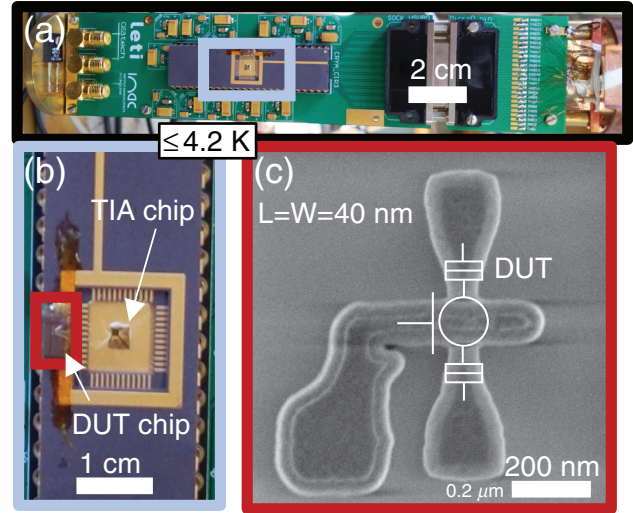


FIG. 4. Pictures of the experimental devices. (a) PCB with the co-integrated TIA and quantum dot device to be placed on a dipstick (≥ 4.2 K) or inside a dilution fridge (down to 10 mK). (b) The FDSOI chip with the TIA circuit is bonded on a 48-pin DIL package. The quantum dot chip (DUT) is glued nearby and wire-bonded to the CMOS chip. (c) SEM image of the FDSOI quantum dot with source and drain contacts and gate dimensions $L = W = 40$ nm.

one ceramic capacitor of 100 nF ($< 10\%$ variation) improve the filtering with the three different equivalent series resistances.

A helium-4 dipstick is used for 4.2 K tests. The PCB is placed at the end of a stick in a closed metal tube with a small quantity of helium gas for thermal exchange to a liquid helium (nitrogen) bath to reach 4.2 K (77 K). Bandwidth and noise measurements are performed in the dipstick by placing a 1 M Ω Metal-Electrode Leadless Face thin film resistor as DUT on the PCB as close as possible to the TIA in order to operate in a voltage-amplifier configuration. For sub-Kelvin measurements, the PCB is placed in a He3-He4 dilution fridge with RC-filtered lines. Thermometers in both setups allow us to monitor the fridge temperature and look for potential heating by the TIA.

At room temperature, a 16-channel low-noise (≤ 3 nV/ $\sqrt{\text{Hz}}$) 15 mA 21-bit digital-to-analog converter provides the DC voltages, and a 50-MHz lock-in amplifier is used to measure bandwidth and noise.

2. Results

The best low-power/high-bandwidth trade-off in analog circuits coincides with transistors operating in moderate inversion. We study the TIA over a wide range of bias current (setting the power consumption) to find the sweet-spot of transistors in moderate inversion. The TIA output V_{out} as a function of the input current I_{in} , shown in Fig. 5(a), exhibits a rail-to-rail linear behavior with a transimpedance gain $Z_T = 11.6 \times 10^6$ V/A from -35 to 55 nA both at 50 mK for a 1- μ W power consumption and at 250 mK for a larger range of P_{DD} allowed by the higher cooling power. An identical transfer function is observed at higher temperatures 77 and 300 K as the TIA gain is set by the temperature-independent feedback resistor R_{fb} (see Fig. S2 in the supplementary material). The transimpedance gain Z_T and the supply voltage $V_{DD} = 1$ V set the current span $\Delta I = V_{DD}/Z_T = 86$ nA while

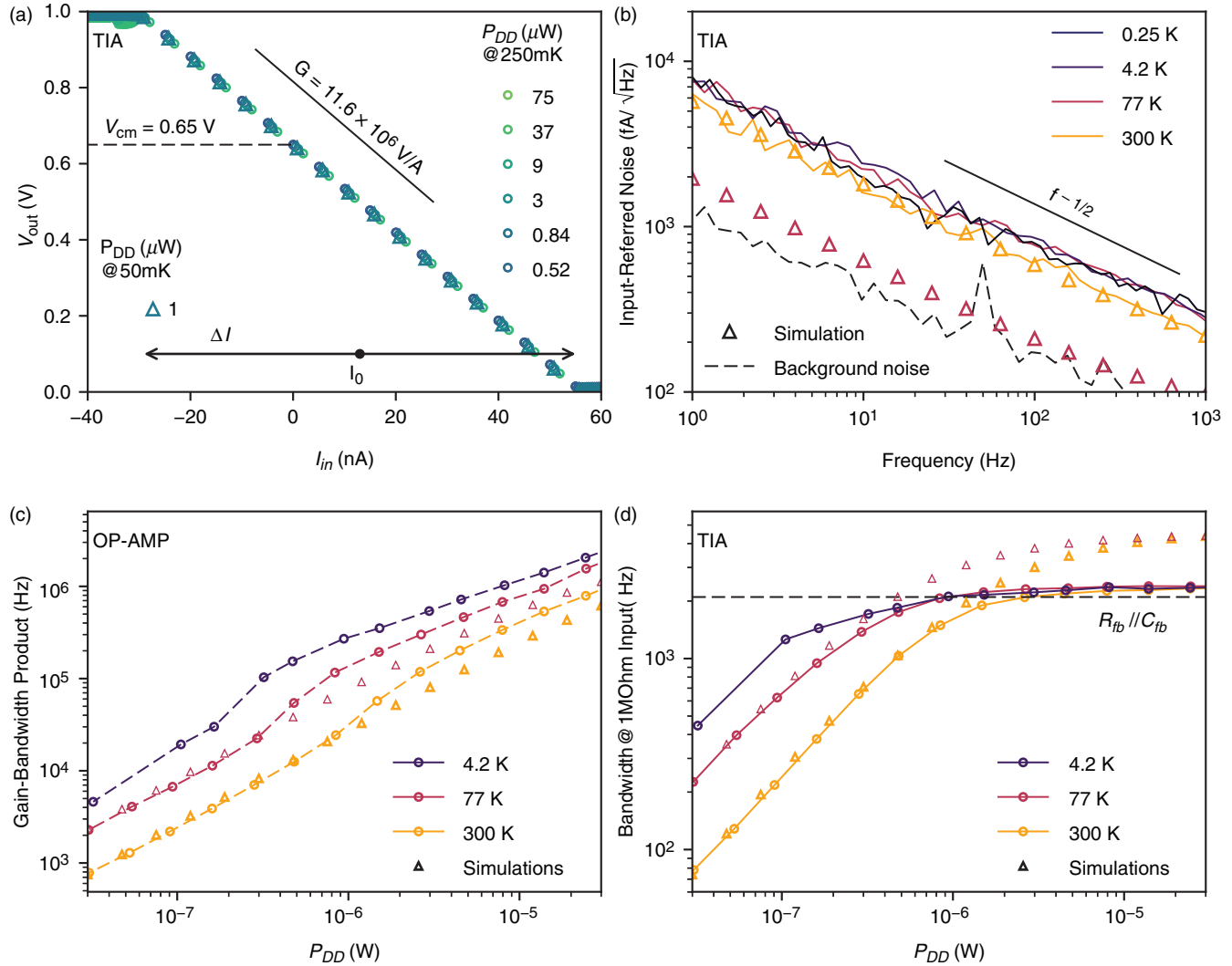


FIG. 5. (a) TIA output voltage V_{out} as a function of the input current I_{in} for several power consumption $P_{DD} = 3I_{bias}V_{DD}$ at 0.25 K and for $P_{DD} = 1 \mu$ W at 50 mK. The impedance gain $Z_T = R_{fb}$ is extracted from the slope. (b) Input-referred current noise of the TIA as a function of frequency for different temperatures, with the background noise of our measuring instrument. The straight line indicates the expected slope for the $1/f$ flicker noise. (c) OP-AMP Gain-Bandwidth and (d) TIA bandwidth when measuring a 1 M Ω impedance as a function of the power consumption P_{DD} for the indicated temperatures.

the common-mode voltage $V_{cm} = 0.65$ V sets the center of the span $I_0 = (V_{cm} - 0.5)/Z_T = 13$ nA [see Fig. 5(a)]. Due to increased threshold voltage $V_{th} \approx 0.6$ V at 4.2 K and the need for $V_{cm} > V_{th}$ (saturation region), V_{cm} cannot be chosen equal to the ideal value $V_{DD}/2 = 0.5$ V thus leading to a slight asymmetry in the measured current-range for linear response.

Transforming the TIA into a voltage amplifier of gain 10 by placing a 1 M Ω resistor connected to V_{in} pin at a close distance of 5 cm on the PCB to avoid the interconnection capacitance allows accurate measurement of the noise and bandwidth of the TIA from 300 to 0.25 K in relevant experimental conditions. The low-frequency voltage noise of the TIA is measured with a lock-in amplifier by averaging the demodulated signal from the OP-AMP output. The input current noise is obtained by dividing the voltage noise by the transimpedance

Z_T [see Fig. 5(b)]. The noise as a function of the lock-in reference frequency f , plotted in Fig. 5(b), shows the characteristic $f^{-1/2}$ dependence for flicker noise. The flicker noise increases by only 30% from 300 K to 250 mK, which is 10 times less than in bulk CMOS.²⁷ This difference in flicker noise between SOI and bulk technologies is known at room temperature.²⁸ The SOI flicker noise has been reported to even decrease at 77 K for some PMOS devices.²⁹ The minimal achievable current noise at 4.2 K, given by the broad-band thermal noise of the 11.6 M Ω feedback resistor, is 5 fA/ \sqrt Hz. The TIA has an enhanced noise of 300 fA/ \sqrt Hz at 1 kHz resulting from flicker noise [see Fig. 5(b)]. As the overall noise changes only slightly with temperature, we expect that P2 and P3 stay the major contributors at cryogenic temperatures, as found with room temperature models. For a typical measurement of quantum dots with currents of

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1 nA,¹¹ the cryo-TIA achieves a signal-to-noise ratio of 60 for an integration time of 10 ms.

The frequency response of the TIA, mounted as a voltage amplifier of gain $\simeq 10$, is measured with the lock-in amplifier from 10 Hz to 50 MHz. Two cutoff frequencies can be identified: one that depends on the bias current, attributed to the Miller capacitance inside the OP-AMP, and one that does not depend on the bias current, attributed to the $R_{fb}C_{fb}$ feedback network (see Fig. S3 in the [supplementary material](#)). In Fig. 5(c), the gain-bandwidth product GBW for the bias-current dependent bandwidth of the OP-AMP is shown as computed from the measured voltage gain and bandwidth at 4.2, 77, and 300 K. The increase in the OP-AMP bandwidth by a factor of 5 corresponds to the transconductance at constant current (similarly, g_m/I_{ds}) largely increasing at cryogenic temperatures in moderate inversion.³⁰ The second bias-current independent cutoff is shown in Fig. 5(d) for the bandwidth data as a function of P_{DD} when measuring a 1 M Ω device. At low power consumption, the frequency limitation is due to the finite gain-bandwidth product of the OP-AMP while at higher power consumption, the measured bandwidth is limited by the feedback network $R_{fb}C_{fb}$ at 2.6 kHz, independently of the temperature.

As expected within the typical accuracy range -40 to 185 °C, the foundry model predicts well the noise and bandwidth of the OP-AMP and TIA at 300 K [see Figs. 5(b)–5(d)]. Simulation results at 77 K still predicts the TIA and OP-AMP bandwidth as seen in Figs. 5(c) and 5(d). The observed difference in the TIA bandwidth at high P_{DD} [Fig. 5(d)] comes from the variability with respect to the nominal resistance value of the highly doped resistor R_{fb} . Unfortunately, models predict a decreased flicker noise at 77 K [see Fig. 5(b)]. Below 77 K, the model stops converging and is unable to predict the circuit specifications change that happen between 77 and 4.2 K.

IV. QUANTUM-CLASSICAL CIRCUIT

We have employed the cryo-TIA to measure the current through quantum dot devices. In the first scenario, we ran a control experiment to validate the measurements with the cryo-TIA and compared them with a room-temperature TIA. To assess the use of the cryo-TIA at sub-Kelvin temperatures, we measured an on-chip quantum-dot structure at 10 mK.

A. 4.2 K Assembly

We mounted the semiconductor chip containing the quantum dot at a few millimeters distance from the chip embedding the cryo-TIA (see Fig. 4). Electrical connections between the two chips were made using standard bonding wires. The quantum dot device consists of an n-type SOI transistor with a 40-nm-wide silicon channel and a 40-nm-long gate electrode. Because of the presence of intentionally wider insulating spacer layers, the gated region is well separated from the heavily doped source/drain contact regions. As a consequence, the electron accumulation induced by a sufficiently positive gate voltage results in the formation of an electron quantum dot under the gate.³¹ The dot is weakly coupled to the source and drain contacts via tunnel barriers naturally formed under the gate spacers. The addition of an extra electron to the dot involves a charging energy cost $U \sim e^2/C$ where e is the electron charge and C is the total capacitance of the dot. Due to the small dot size, U is of the order of a few meV, which can largely exceed the thermal energy $k_B T$ when $T < 10$ K. In this

cryogenic regime, electron transport through the quantum dot is governed by the Coulomb blockade effect.³¹

The right panel of Fig. 6(b) shows a color-scale plot of the source-drain current I_{ds} as a function of the voltages V_{gs} and V_{ds} applied to the gate and to the drain electrodes. This measurement was taken with the quantum dot and the cryo-TIA at 4.2 K. The cryo-TIA was set to dissipate 1 μ W in order to reach a 2.6 kHz bandwidth for a measured impedance ≥ 1 M Ω . The two-dimensional plot shows characteristic diamond structures where current transport is suppressed due to Coulomb blockade. Each of these regions are associated with a well-defined integer number, N , of excess electrons in the dot, increasing progressively from left to right (we estimate $N \sim 100$ in the displayed V_{gs} range).

To confirm the faithful operation of our quantum-classical circuit, we carried out a control experiment by replacing the cryo-TIA with a room temperature transimpedance amplifier (RT-TIA) with comparable performance. More specifically, the RT-TIA employed an off-the-shelf operational amplifier with the same circuit architecture as in the cryo-TIA and a feedback resistor of 10 M Ω . It exhibits an 18-MHz gain-bandwidth product and a 2-mW power consumption.³² In Fig. 6(a), we compare the frequency response of the cryo-TIA and the RT-TIA when measuring a resistance of 14 M Ω . While the cryo-TIA reaches the expected 2.6-kHz bandwidth, the response of the RT-TIA is cut at 600 Hz. We ascribe this to the RC time associated with the 14-M Ω DUT impedance and the capacitance of the input wire, $C_{cable} \simeq 100$ pF.

The stability diagram measured with the RT-TIA and with the quantum dot device at 4.2 K is shown in the left panel of Fig. 6(b). We find no significant differences with respect to data from the cryo-TIA. We emphasize that for a fair comparison the two data sets were acquired by spanning the same V_{gs} and V_{ds} ranges in the same amount of time (about 2 min). For further clarity, we compare in Fig. 6(c) representative horizontal linecuts, $I_{ds}(V_{gs})$ at $V_{ds} = \pm 1$ mV. The Coulomb blockade oscillations are clearly visible with comparable quality. Yet the cryo-TIA is much less power consuming (1 μ W against 2 mW). Moreover, it shows a lower current-offset (0.3 pA against 26 pA for the RT-TIA), which can be attributed to the higher leakage current associated with the long cable connecting the quantum dot to the RT-TIA. (We note that for both measurement configurations, the TIA offset was zeroed by adjusting the common-mode voltage V_{cm} when the device was open, i.e., no current flowing.)

Co-integration experiments at 4.2 K validated the use of the cryo-TIA to characterize quantum-dot devices. The low power of the cryo-TIA allows placement of it at sub-Kelvin temperature in the vicinity of the DUTs. The ultimate quantum-classical integration will consist of classical circuitry built in the same silicon substrate as the quantum devices. In Sec. IV B, we demonstrate such integration at 10 mK.

B. 10-mK Integration

Small gate lengths of modern industrial CMOS technologies enable the fabrication of nm-sized MOS quantum dots on a 300-mm wafer. Tiny MOSFETs turn into quantum devices such as single electron transistors at cryogenic temperature (4.2 K and below) under the right voltage biasing. More complex quantum structures are then built such as in Refs. 14 and 33. We laid out a quantum device as shown in Fig. 7(b). Two 40-nm-long polysilicon gates are deposited on top of a 80-nm-wide FDSOI channel. The two gates are placed as close as

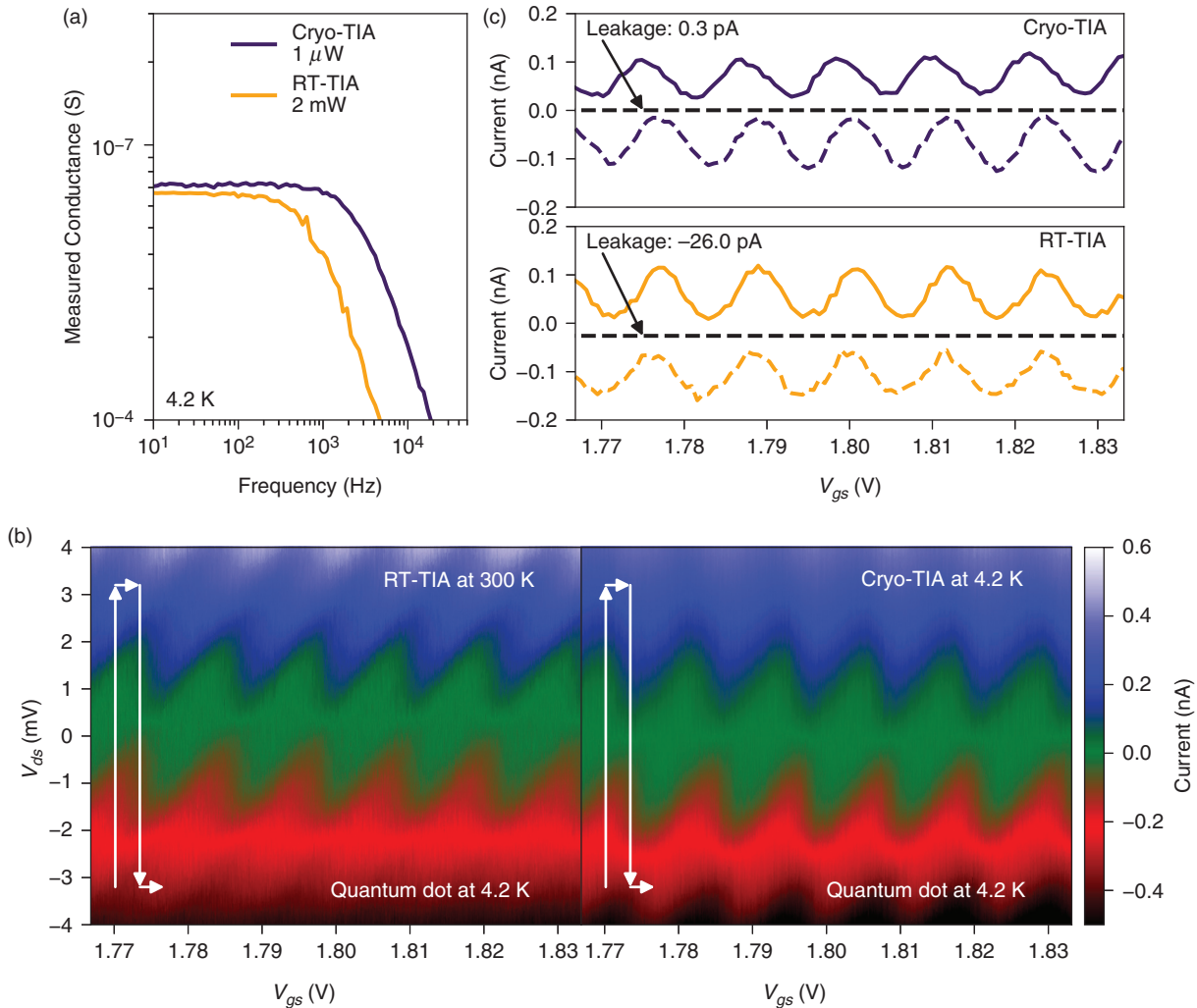


FIG. 6. (a) The frequency response of the RT-TIA at 300 K and the cryo-TIA at 4.2 K when measuring the quantum-dot placed at 4.2 K for a resistance of about 14 MΩ at the same (V_{ds} , V_{gs}) bias point. Extracted bandwidths of 0.6 and 2.6 for, respectively, RT-TIA, and cryo-TIA. (b) Coulomb-diamond structure in the measured current $I_{ds}(V_{ds}, V_{gs})$ for the same single quantum dot at 4.2 K measured with the cryo-TIA and the RT-TIA for the same acquisition time (2 min). White arrows illustrate how voltages V_{ds} and V_{gs} are swept. V_{ds} is a triangular signal of period $2t$ and V_{gs} is stepped each $t = 260$ ms by $100 \mu\text{V}$. Coulomb oscillations in (c) are extracted from (b) at $V_{ds} = \pm 1$ mV. The leakage currents extracted by averaging the signals for positive and negative V_{ds} are indicated in the top-left corner.

allowed by the founder design rules and are spaced 96 nm apart. High doping dose is injected in the source, drain, and inter-gate space. The source is directly routed to a pad and linked to room temperature via constantan wiring. The drain is routed to the on-chip cryo-TIA with 10- μm -long first-level metal routing [see Fig. 7(a)]. DC gate-voltages are applied from room temperature through an on-chip bias tee made of a 1 MΩ polysilicon resistor and metal-oxide-metal capacitors routed to high-frequency circuitry discussed in Ref. 14.

At cryogenic temperatures, this device consists of three quantum dots in series. The highly doped inter-gate region forms a metallic quantum dot with equally spaced quantum states related to the island area 96 nm \times 80 nm. Under each gate, a quantum dot can be created by applying the appropriate gate-voltage around the threshold voltage of the associated FET-behavior. Each quantum dot is linked to its

neighbors by tunnel junctions. Applying a voltage difference between the source and drain V_{ds} forces a current to flow through the quantum dots, depending on their individual impedance. Transport through the quantum structure is governed by the lowest tunneling rate of the barriers and by the alignment of quantized states in the V_{ds} window.

The chip containing the cryo-TIA and the quantum device is placed at the mK temperature stage of a dilution fridge. The TIA dissipates only 1 μW , leading to a fridge temperature of 10 mK.

The DC through the structure is measured by applying $V_{ds} = 1$ mV as a function of the gate voltages with a voltmeter connected to the TIA output [see Fig. 8(c)]. Under zero back-gate voltage, transport is dominated by the under-gate dots as attested by the 2D pattern of current triangles shown in Fig. 8(c). The operating regime of the quantum device is depicted in Fig. 8(a).

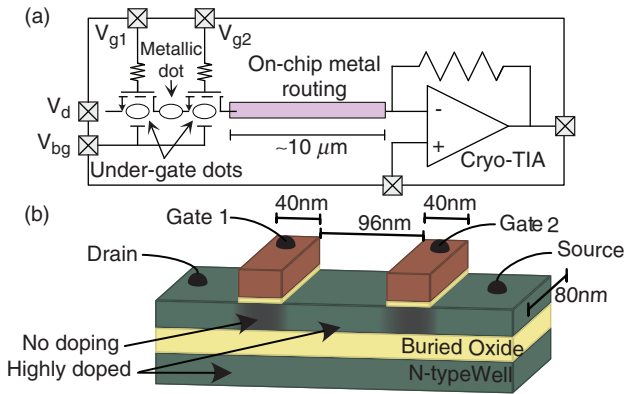


FIG. 7. (a) Integrated quantum dot and cryo-TIA. (b) We laid out a quantum device with two minimally spaced gates on top of a narrow FDSOI channel. It can be seen in this figure that two 40-nm-long polysilicon gates, deposited on top of a 80-nm-wide FDSOI channel are included. The two gates are placed in agreement with the founder design rules, being spaced 96 nm apart. High doping dose is injected in the source, drain, and inter-gate space. The source is directly routed to a pad and linked to room temperature via constantan wiring. The drain is routed to the on-chip cryo-TIA with 10- μm -long first-level metal routing. DC gate-voltages are applied from room temperature through an on-chip bias tee made of a 1-M Ω polysilicon resistor and metal-oxide-metal capacitors routed to high-frequency circuitry.

As the back-gate voltage increases, enhancing back-channel conduction, under-gate dots are bypassed, leading to a direct tunneling junction between the metallic dot and the source and drain. As a result, the single dot behavior emerges, as shown in Fig. 8(b). To

measure the current through the single dot configuration with better sensitivity, we measure the conductance $G_{ds} = dI_{ds}/dV_{ds}$ by applying an 5mV_{pp} AC excitation on V_{ds} and demodulating the cryo-TIA output with a large integration time of 10 ms. Single dot characteristics of Coulomb peaks, equally coupled to each gate, start to dominate transport, as seen in Fig. 8(d) with the tilted lines. A cut view of $G_{ds}(V_{g2})$ demonstrates clear regular Coulomb peaks spaced by a charging energy of $\sim 7\text{mV}$. The peak width is limited by the AC source-drain voltage of 5 mV.

V. CONCLUSION

The analysis of important transistor parameters such as the conductance and transconductance as a function of the gate-length extracted from single transistor current-voltage characteristics measured at 300, 4.2, and 0.25 K allowed us to design a TIA operating down to 10 mK for a 1- μW power consumption to measure high-impedance quantum-dot devices. The TIA is composed of an OP-AMP with an integrated resistive feedback. The two-stage Miller-compensated operational amplifier, whose power consumption can be varied from 300 nW to 30 μW via the bias current, achieves a 250-kHz gain-bandwidth product at 1 μW that rises to 1 MHz at 10 μW . The obtained 1.9-k Ω output impedance combined with the 100-pF cable capacitance placed at the OP-AMP output leads to a higher RC frequency cutoff (5.3 MHz). As a result, the OP-AMP bandwidth is only limited by its intrinsic gain-bandwidth product.

The TIA uses a resistive feedback made of a practically temperature-independent polysilicon resistor R_b to achieve a high transimpedance gain of 11.6×10^6 V/A from room to sub-Kelvin

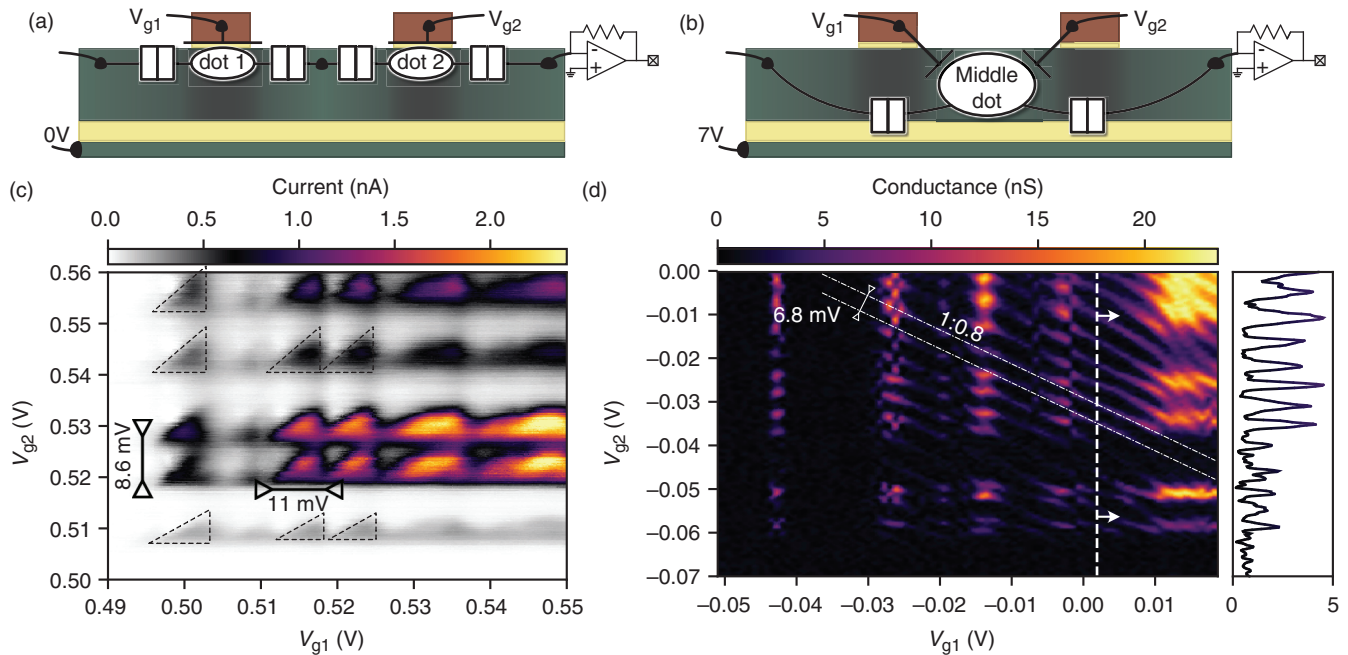


FIG. 8. Schematic of the cryo-TIA to measure stability diagrams of the on-chip quantum device at a fridge temperature of 10 mK in (a) the double quantum dot regime under zero back-gate voltage and (b) the single quantum dot regime under high back-gate voltage $V_{bs} = 7$ V. The single dot is situated on the highly-doped metallic island equally coupled to both gates. (c) Current as a function of DC gate voltages V_{g1} and V_{g2} at $V_{bs, dot} = 0\text{V}$ revealing triangular structures. (d) Lock-in conductance measurement of the quantum device with $V_{bs} = 7\text{V}$ revealing parallel lines of non-zero conductance, signature of a single dot equally coupled to both gates.

temperatures with a linear response for ± 40 nA. When electrically contacted for characterization, the transimpedance amplifier has a large capacitance placed at the input V_{in} from meter-length cables that require the use of the capacitor C_{fb} placed in parallel with R_{fb} to ensure the stability of the TIA circuit. The resulting $R_{fb}C_{fb}$ time limits the maximum bandwidth of the TIA to 2.6 kHz for power consumption above $1 \mu\text{W}$. For lower power consumption, the bandwidth is limited by the GBW product of the op-amp and varies with power. The input-referred noise within the TIA bandwidth is limited by the $1/f$ flicker noise with a current noise given by $300 \text{ fA}/\sqrt{\text{Hz}}$ at 1 kHz, which shows an increase in only 30% down to 0.25 K. Compared to other realizations of TIAs at cryogenic temperatures (see Table III), this cryo-TIA achieves a lower power consumption, a smaller footprint, and a lower operating temperature. The comparably higher noise and lower bandwidth can be improved in future iterations, as discussed in Sec. VI.

At 4.2 K, the cryogenic amplifier was assembled with an FDSOI single quantum dot positioned a few millimeters away to assess its performance. The results were compared to those obtained with a more conventional setup employing a room temperature TIA connected to the quantum chip via a meter-long cable. When measuring the quantum device biased by its source-drain voltage and gate-source voltage at an impedance value of $14 \text{ M}\Omega$, the cryogenic TIA achieves a better bandwidth than the RT-TIA limited at 600 Hz by the cable capacitance. For the same acquisition time, both TIAs were able to measure the usual Coulomb-diamond structure in the transport current across the dot. Thanks to reduced interconnection length, the cryo-TIA exhibits a low 300-fA leakage current while the RT-TIA shows a leakage of 26 pA.

At a fridge temperature of 10 mK, the TIA measurements on a double quantum dot indicate that the quantum properties due to the confined geometries can be observed down to the lowest temperatures for the fully on-chip integration of measuring electronics and quantum device.

VI. PERSPECTIVES

The use of back-gate voltage, as can be done with the FDSOI technology, will improve the performance of the cryogenic TIA. First,

the threshold gate-voltage of the transistors can be lowered at the usual level of about 0.4 V by tuning the back-gate voltage, thus allowing the common-mode voltage to lie at $V_{DD}/2$, resulting in a symmetric range of ± 43 nA for the measurable currents. Second, the flicker noise, presumably mainly coming from the top gate-oxide/silicon interface, will be reduced for applied back-gate voltage as the conduction is displaced toward the much cleaner bottom-gate interface.

The bandwidth of the cryogenic TIA is limited by the RC-network in the feedback loop. While the resistor R_{fb} sets the necessary gain, C_{fb} was added to ensure stability with large cable capacitance present at the V_{cm} pin. C_{fb} can be greatly reduced when measuring a device at a few millimeters distance as the remaining interconnection capacitance has been greatly reduced compared to the cable capacitance. A capacitance of about 10 fF would be sufficient and would lead to a bandwidth of 1 MHz, compatible with the 1 MHz GBW product of the OP-AMP at $10 \mu\text{W}$. At such high frequency, the $1/f$ flicker noise contribution will be highly reduced, reaching the broad-band thermal noise that is expected to even decrease at cryogenic temperature. Increasing the bandwidth will improve the signal-to-noise ratio of the cryo-TIA to meet the requirement for fast quantum dot characterization and readout.

Besides their use for the characterization of quantum-dot stability diagrams, TIAs are implemented to perform single-shot spin-state readout. Measuring the current of a quantum dot near a current step results in a high-speed and low-noise response to a capacitive change occurring due to, for example, moving electrons in nearby dots. Spin-state readout requires only a binary output and not the continuous analog output of usual amplifiers. With the availability of electronics at a low temperature, one way to move toward scalability in the number of qubits is to enhance the amplifier specificity in order to exactly match the needs. This allows reduction of the power consumption and increase of the readout speed. This approach of tailored integrated electronics attracts much attention, and examples have already been presented.³⁴

The back-action of circuits on the quantum systems¹³ from noise or heating needs to be addressed in future work. The control of the

TABLE III. Comparison of the specifications of the RT-TIA with the cryo-TIAs presented in this study and in previous state-of-the-art work with respect to technological layout and electrical performance.

	RT-TIA Off-the-shelf	Cryo-TIA Tagliaferri <i>et al.</i> [11] (2016)		Cryo-TIA This work		Units
	TIA [32]	Low Gain	High Gain	With C_{fb}	Without C_{fb}	
Technology	Discrete CMOS Bulk	CMOS Bulk $0.35 \mu\text{m}$		CMOS FDSOI 28 nm		
Footprint	—	1.1		0.01		mm^2
Gain	10×10^6	4.1×10^6	20×10^6	11.6×10^6		V/A
Range	± 750	± 85		± 45		nA
Power consumption	2000	5000		1		μW
Bandwidth	0.6	250	31	2.6	230	kHz
BW limited by	Cable Capacitance	Feedback Network		Feedback Network		
Noise	40	30	10	300		$\text{fA}/\sqrt{\text{Hz}}$
Lowest temperature of operation	300	4.2		0.01		K

back-action will be a primordial ingredient in circuit design for large-scale quantum applications. Preliminary studies performed at 4.2 K show that mW power leads to a few Kelvin increase in transistor temperature.²⁶ This study needs to be extended down to sub-Kelvin temperature for smaller power dissipation. The presented TIA with varying power consumption at sub-Kelvin temperature offers the ideal platform for such investigations.

The ability to design low-power amplifiers resulting in a reasonable heat load at the sub-Kelvin temperature stage in dilution fridges will increase the measurement rate of cryogenic devices. Ultimately, the realization of custom-made electronics in FDSOI technology for cryogenic operation at any temperature will improve measurement speed and quality inside cryostats with higher bandwidth, lower noise, and higher signal-to-noise ratio.

SUPPLEMENTARY MATERIAL

See [supplementary material](#) for integrated resistors values against temperature, room temperature stability analysis of the OP-AMP, and characterization of the TIA at higher temperatures (4.2, 77, and 300 K).

AUTHORS' CONTRIBUTIONS

All authors contributed equally to this manuscript. All authors reviewed the final manuscript.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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