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Short-term reliability of high performance Q-band AlN/GaN HEMTs

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Abstract— We report on an on-wafer short-term 40 GHz RF reliability stress test comparison between a 3 nm versus 4 nm barrier thickness AlN/GaN HEMT technology showing state-of-the-art power performances in the millimeter wave range. It is found that the barrier thickness in this highly strain heterostructure has a major impact on the device reliability. The superior robustness when using thinner barrier (closer to the critical thickness) is attributed to the reduced strain.

Keywords- GaN, HEMTs, output power density (P_{out}), power added efficiency (PAE), Q-band, on-wafer short-term reliability

I. INTRODUCTION

In the last decade, considerable progress have been made in Gallium Nitride (GaN)-based RF power devices, which will enable new applications such as military wireless communication, SATCOM and 5G next generation of mobile broadband. Those applications operating at high frequency need compact systems, for which the power-added-efficiency (PAE) associated to a high output power density (P_{OUT}) in the millimeter-wave (mmW) range represents currently one of the key goal for the GaN technology. Some promising data have been recently reported in this frame [1]-[3]. Nevertheless, for short GaN transistors delivering high performance with gate lengths below 150 nm, the main limitation is the device reliability due to a significant electric field peak and subsequent high junction temperatures under high drain bias. That is why, very few mmW GaN device reliability reports can be found so far in the literature.

In this work, we studied the RF robustness at 40 GHz of two HEMT structures using 3 nm and 4 nm AlN ultrathin barriers at various temperatures.

II. DEVICE FABRICATION AND STRESS PROCEDURE

The two heterostructures have been grown by metal organic chemical vapor deposition (MOCVD) on 4-in. SiC substrates. They consist in an AlN nucleation layer, a 1- μ m carbon-doped GaN buffer layer followed by an undoped 100 nm GaN channel and a 3.0 and 4.0 nm ultrathin AlN barrier layer, respectively. Both HEMTs were capped with a 10 nm thick in-situ SiN layer used as early passivation as well as to reduce the surface trapping effects. Identical processing has been carried out on the two wafers and verified through several batches.

A short-term on-wafer RF stress has been applied at various drain bias voltage (V_{DS}) and temperatures. $2 \times 50 \mu\text{m}$ transistors with a gate-drain distance (GD) of 1.5 μm and a gate length (L_G) of 110 nm have been monitored during 24 hours by steps of 8 hours under large signal conditions at 40 GHz at the peak PAE. Details of the power bench used for these measurements can be found in [4].

III. DATA/RESULTS AND DISCUSSION

Figure 1 shows the RF monitoring performed at 40 GHz on the 4 nm AlN barrier structure described earlier. The devices have been tested during 24 hours at room temperature with V_{DS}

=12V. We observed a systematic strong degradation of performances over time. The PAE decreases from 45% down to 30% after 24 hours stress while P_{OUT} drops from 1.4 W/mm down to 0.8 W/mm. The same test has been attempted at higher V_{DS} . After few minutes at $V_{DS} = 15\text{V}$ and 20V, the devices deliver significant gate leakage current as shown in Figure 2.

On the other hand, the 3 nm AlN barrier devices show no degradation when subjected to the same RF stress at 40 GHz at room temperature during 24 hours with $V_{DS} = 20\text{V}$ (Fig. 3 and 4) and $V_{DS} = 30\text{V}$ (Fig. 7 and 8). For this 110 nm technology, the PAE (50%) with a P_{OUT} around 3 W/mm at 40 GHz remains stable with no increase of gate and drain leakage currents up to $V_{DS} = 30\text{V}$.

The high robustness has been verified at higher temperature. Thus, the base-plate temperature (T_{bp}) has been increased up to 140°C by steps of 4 hours while using identical RF stress conditions at 40 GHz. The estimated junction temperature in this case is well-above 250°C. Figure 5 shows a slight reduction of the PAE as a function of temperature from 47% at $T_{bp} = 50^\circ\text{C}$ down to 40% at $T_{bp} = 140^\circ\text{C}$. This decrease is due to the thermal impact on the electron mobility, which affects the gain and thus the PAE. Owing to a compensation of the gate bias voltage at every T_{bp} to fix and maintain the drain current at 100 mA/mm, P_{OUT} remains stable. It can be noticed that for each temperature, the PAE is stable during the 4 hours stress. Furthermore, after the entire test of 24 hours at several temperatures, the degradation observed on the PAE is fully reversible and recovers to its initial value. It is also important to note that no leakage current is observed with an off-state current below 100 $\mu\text{A/mm}$ (see Fig. 6). The superior robustness combined with outstanding mmW performance are attributed to the reduction of the barrier thickness. It is believed that the improvement is directly related to the reduced strain when decreasing the barrier thickness. Further investigations will be carried out in order to confirm this assumption.

IV. CONCLUSIONS

In this work, two heterostructures for mmW applications based on AlN/GaN material with 3 nm and 4 nm barrier thickness have been compared in terms of device robustness for 24 hours. The 4 nm AlN barrier devices show a strong RF performance degradation at room temperature at $V_{DS} = 12\text{V}$ and a full degradation for higher V_{DS} . However, no degradation is observed up to V_{DS} as high as 30V and $T_{bp} = 140^\circ\text{C}$ during 24 hours for the 3 nm AlN barrier devices. This is attributed to the strain reduction when using thinner barrier thickness. These results pave the way for highly reliable high performance mmW GaN transistors.

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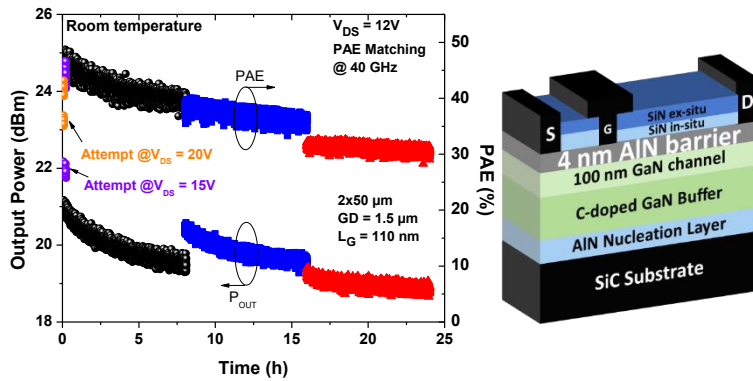


Figure 1. Output power and PAE monitoring for 24 hours at room temperature with $V_{DS} = 12, 15$ and 20 V (PAE matching).

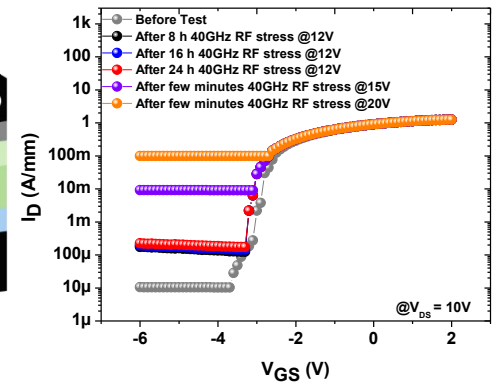


Figure 2. Transfer characteristics before and after 8, 16 and 24 hours of 40 GHz RF stress at $V_{DS} = 12, 15$ and 20 V at room temperature.

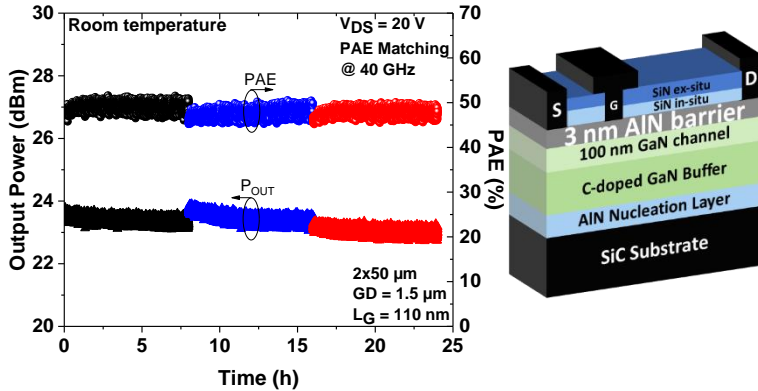


Figure 3. Output power and PAE monitoring for 24 hours at room temperature with $V_{DS} = 20$ V (PAE matching).

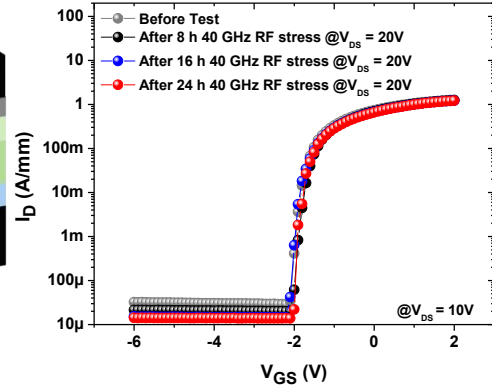


Figure 4. Transfer characteristics before and after 8, 16 and 24 hours of 40 GHz RF stress at $V_{DS} = 20$ V at room temperature.

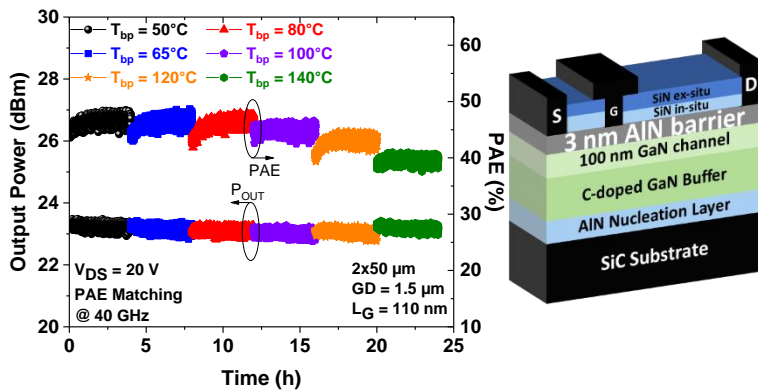


Figure 5. Output power and PAE monitoring for 24 hours for several temperatures up to 140°C with $V_{DS} = 20$ V (PAE matching).

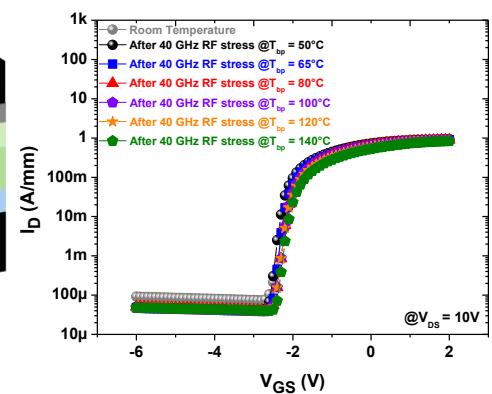


Figure 6. Transfer characteristics before and after 4 hours at $50, 65, 80, 100, 120$ and 140°C of 40 GHz RF stress at $V_{DS} = 20$ V.

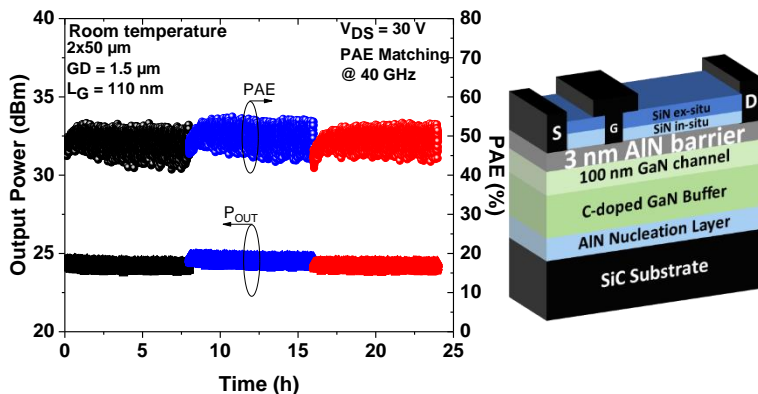


Figure 7. Output power and PAE monitoring for 24 hours at room temperature with $V_{DS} = 30$ V (PAE matching).

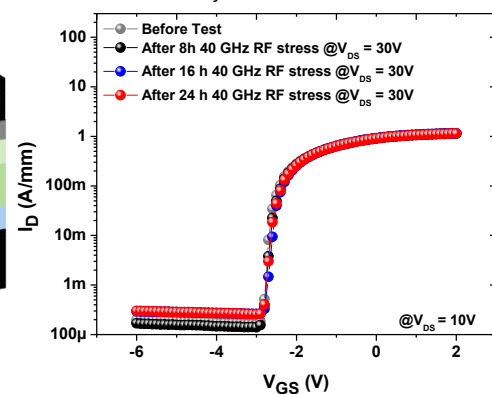


Figure 8. Transfer characteristics before and after 8, 16 and 24 hours of 40 GHz RF stress at $V_{DS} = 30$ V at room temperature.