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High Power AlN/GaN HEMTs with record power-added-efficiency >70% at 40 GHz

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Abstract—We report on breakthrough power-added-efficiency (PAE) Q-band performances using a vertically scaled AlN/GaN HEMT technology. The comparison between a 3 nm and 4 nm barrier thickness shows both superior performance and robustness for the thinner barrier layer attributed to the reduced mechanical strain into the heterostructure. Large signal characteristics at 40 GHz revealed an outstanding PAE of 73% at $V_{DS} = 30V$ associated to an output power density > 5 W/mm in pulsed mode. Also, the load-pull measurements mapping across the 4-inch wafer demonstrates a high uniformity and reproducibility of the results. Consequently, significantly improved PAE can be expected for next generation of high power MMICs operating in the millimeter-wave range.

Keywords—GaN, HEMTs, AlN/GaN, output power density (P_{out}), power added efficiency (PAE), Q-band.

I. INTRODUCTION

GaN technology has been commercially available for about a decade and is being used for power applications into the millimeter-wave (mm-wave) range owing to its outstanding material properties. In this context, the power-added-efficiency (PAE) becomes a key parameter in order to support complex wave forms with high peak-to-average ratio and large instantaneous bandwidth required for 5G applications for instance. Overall, a high PAE is mandatory in order to reduce the power dissipation, which is a major issue for next generation of compact solid state power amplifiers. Due to its high electron velocity and high breakdown voltage, GaN-based material is well suited for future power amplifier requirements which will enable newer emerging applications. High electron mobility transistors (HEMTs) on SiC substrate have already demonstrated attractive efficiencies in the mm-wave range [1]–[5]. However, state-of-the-art GaN HEMT PAE performances are typically limited to below 50% in the Ka-band and above, especially for significant power density > 2 W/mm. This is mainly due to the lack of power gain, the enhanced trapping effects and reduced electron confinement when downscaling the device size or the self-heating.

Ultrathin barrier AlN/GaN heterostructure is promising for mm-wave range because of the possibility to highly scale the epitaxial structure while still benefiting from a high polarization (i.e. high current density). In this work, a comparison of device performances of two HEMT structures using 3 nm and 4 nm AlN barrier layer is reported with the aim of pushing the PAE limit of mm-wave GaN-based HEMTs.

II. DEVICES TECHNOLOGY

The heterostructure has been grown by metal organic chemical vapour deposition (MOCVD) on 4-inch SiC substrates. Fig. 1 shows the schematic cross section of the HEMT structures based on an AlN nucleation layer, a carbon-doped GaN buffer layer followed by a 100 nm GaN channel. The GaN channel thickness has been optimized with respect to the trade-off between deep-level-traps generation and a proper electron confinement. Two different AlN barrier thickness 3 nm (Fig. 1.a) and 4 nm (Fig. 1.b) have been used in order to study the impact on the device performances considering that residual strain is highly dependent on the barrier thickness in such a material system. Finally, a 10 nm thick in-situ Si_3N_4 was deposited for both structures as early passivation as well as to reduce the surface trapping. The source drain ohmic contacts have been formed by etching the in-situ Si_3N_4 layer followed by a Ti/Al/Ni/Au metallization annealed at 850°C for structure (a) and 875°C for structure (b). Then, asymmetric self-aligned Ni/Au T-gates have been used to maintain a high breakdown voltage. The gate-to-drain distances (L_{GD}) were 1 and 2 μm and the gate length was 110 nm. Finally, the devices were passivated with 200 nm PECVD Si_3N_4 .

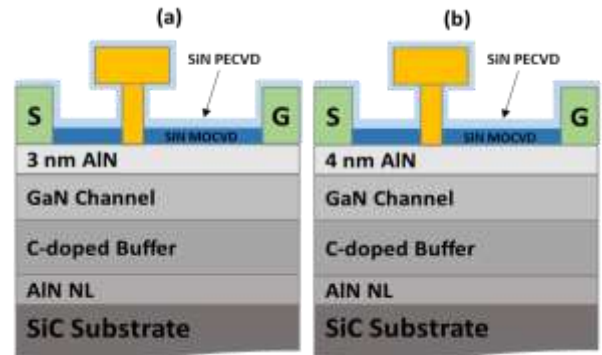


Fig. 1. Schematic cross section of the fabricated (a) $2 \times 50 \mu m$, 3 nm AlN/GaN HEMT (b) $2 \times 50 \mu m$ 4 nm AlN/GaN HEMT.

III. RESULTS AND DISCUSSION

Fig. 2 shows the transfer characteristics with a compliance fixed at 150 mA/mm and swept from $V_{DS} = 2V$ to 20V for both devices in order to evaluate the electron confinement. Fig. 2a shows an excellent electron confinement for the 3 nm AlN barrier structure reflected by a low DIBL of 14 mV/mm. On the other hand, the 4 nm AlN barrier structure shows a rather poor electron confinement with a much higher DIBL of 55 mV/mm. Also, we observed a systematic degradation of the drain leakage current as a function of the drain bias. This degradation is attributed to the higher residual strain when using thicker

barrier layer as the critical thickness of AlN on GaN is about 2 to 3 nm.

Large signal performances have been assessed at 40 GHz. For all load-pull measurements, the impedance matching has been tuned to favor the PAE. Fig. 3.a shows CW and pulsed power performances at $V_{DS} = 20V$ of a 4 nm AlN/GaN HEMT with $L_G = 110$ nm and $L_{GD} = 2 \mu m$. Under pulsed operation, a saturated P_{OUT} of 3.2 W/mm associated to a peak PAE of 60% has been achieved. However, due to the trapping effects the PAE drops to 45% in CW mode with a saturated P_{OUT} of 2.9 W/mm. Despite the attractive power performance, a strong degradation of the drain leakage current on the transfer characteristics is observed after the load-pull measurements at $V_{DS} = 20$ V as shown in Fig. 3.b. Again, it appears that the strain increases considerably with the AlN barrier thickness enhancing the defect density into the barrier layer thus dramatically reducing the device robustness.

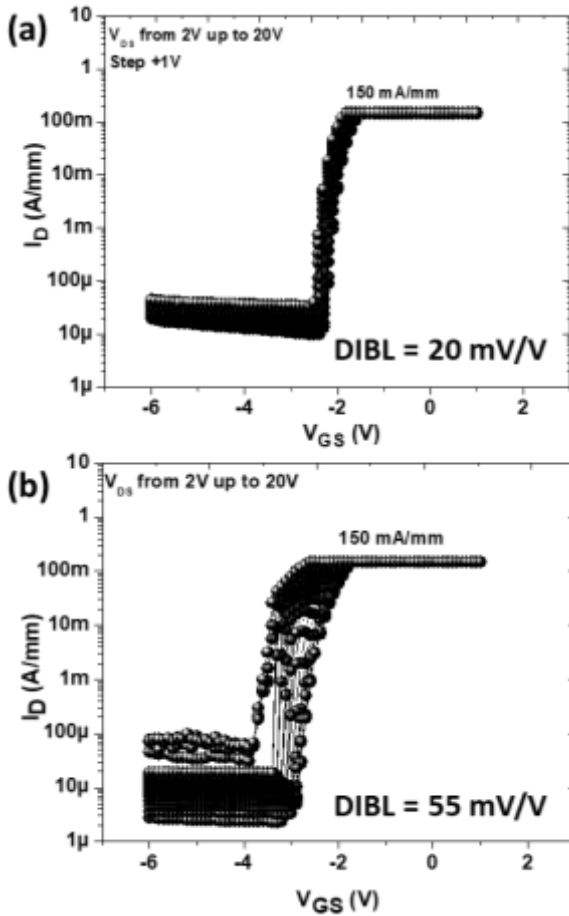


Fig. 2. Transfer characteristics with a compliance fixed at 150 mA/mm and V_{DS} swept from 2V to 20V for 2x50 μm 3 nm AlN/GaN HEMT (a) and 4 nm AlN/GaN HEMT (b)

On the other hand, the 3 nm AlN barrier structure using identical design and processing shows a high PAE of 65% and 53% with a saturated P_{OUT} of 3.3 W/mm and 2.5 W/mm in pulsed mode and CW, respectively (see Fig. 4.a). Interestingly, the transfer characteristics after load-pull measurements at V_{DS}

= 20V show no-degradation of drain leakage current in pulsed mode and a slight increase in CW as seen in Fig. 4.b. This confirms that the thinner barrier layer reduces the mechanical strain leading to a lower defect density, thus resulting in a significantly improved device robustness as compared to thicker barrier.

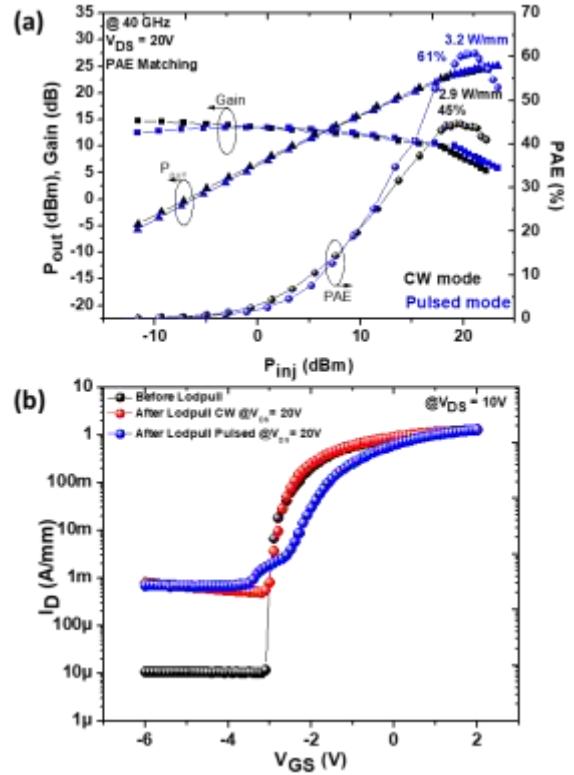


Fig. 3. CW and pulsed power performances of a 4 nm AlN/GaN HEMT 2x50 μm with $L_G = 110$ nm and $L_{GD} = 2 \mu m$ at $V_{DS} = 20V$ (a) and Transfer characteristic before and after load-pull measurements at $V_{DS} = 20V$ (b).

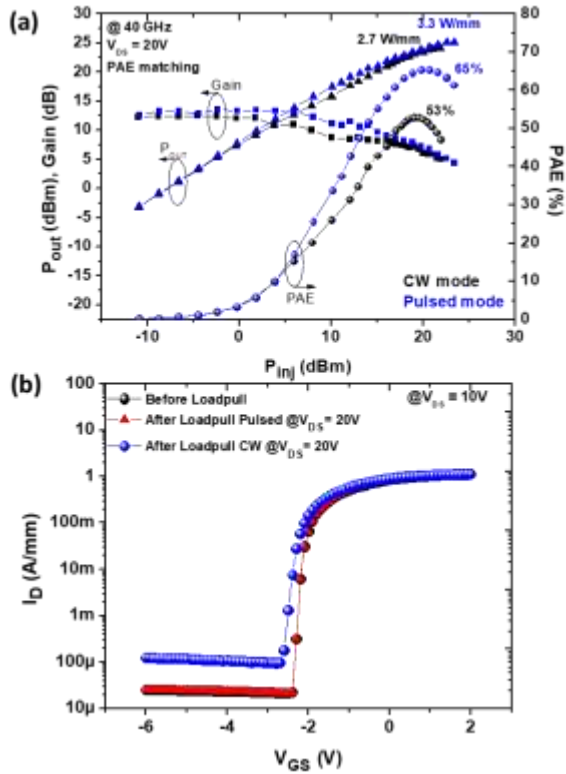


Fig. 4. CW and pulsed power performances of a 3 nm AlN/GaN HEMT $2 \times 50 \mu\text{m}$ with $L_G = 110 \text{ nm}$ and $L_{GD} = 2 \mu\text{m}$ at $V_{DS} = 20 \text{ V}$ (a) and Transfer characteristic before and after load-pull measurements up to $V_{DS} = 20 \text{ V}$ (b).

Further scaling of the 3 nm AlN/GaN device design (shorter L_{GD}) enabled a record PAE for GaN HEMT at 40 GHz. Fig. 5 shows the CW and pulsed power performances at $V_{DS} = 30 \text{ V}$ of devices with $L_G = 110 \text{ nm}$ and $L_{GD} = 1 \mu\text{m}$. An outstanding peak PAE of 73% associated to a saturated P_{OUT} above 5 W/mm was achieved under pulsed operation. CW PAE was close to 60% with a P_{OUT} of 4.3 W/mm . Moreover, as previously discussed no-degradation of the devices has been observed after load-pull measurements up to $V_{DS} = 30 \text{ V}$ although a shorter design has been used.

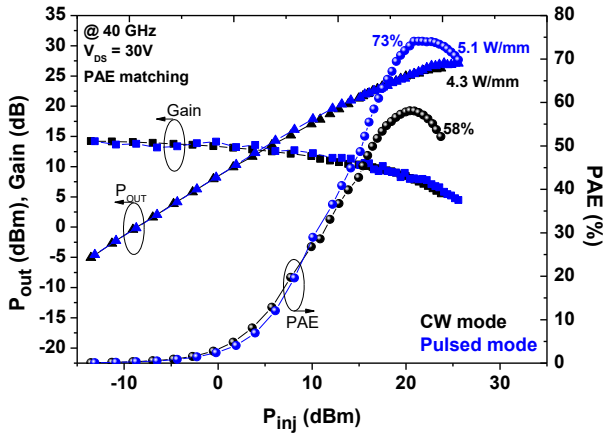


Fig. 5. CW and pulsed power performances of a 3 nm AlN/GaN HEMT $2 \times 50 \mu\text{m}$ with $L_G = 110 \text{ nm}$ and $L_{GD} = 2 \mu\text{m}$ at $V_{DS} = 30 \text{ V}$.

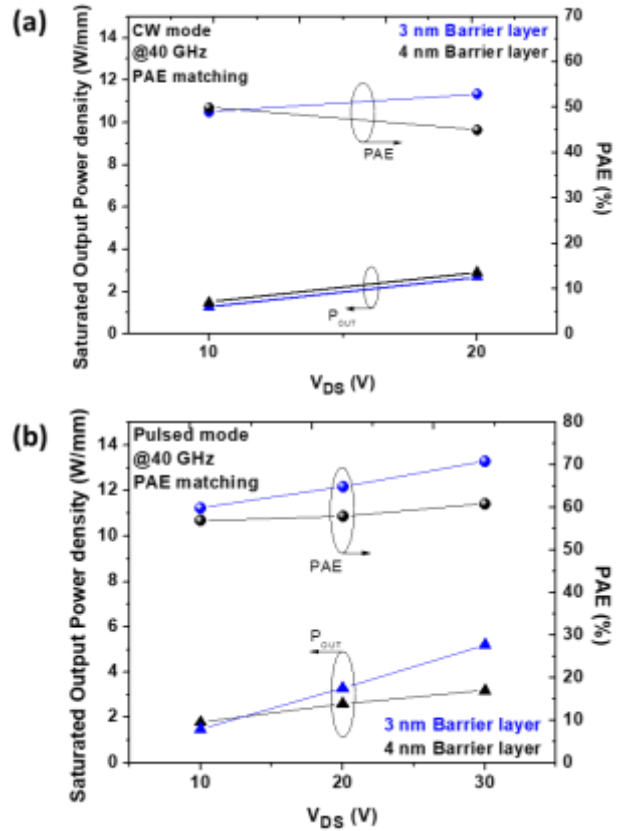


Fig. 6. CW (a) and Pulsed (b), P_{OUT} and PAE as a function of V_{DS} for 3 nm and 4 nm AlN/GaN HEMT.

The power performance comparisons between the 3 nm and 4 nm AlN/GaN structures in CW and pulsed mode are reported in Fig. 6. At low drain bias voltage ($V_{DS} < 15 \text{ V}$), we observed no differences between the 2 structures in terms of power performances both in CW (Fig. 6a) and pulsed mode (Fig. 6b). In contrast, for higher drain bias ($V_{DS} > 15 \text{ V}$) an increasing gap appears especially for the PAE as a function of V_{DS} . To a large extent, this can be attributed to the degradation of the DC characteristics after load-pull measurements of the 4 nm AlN/GaN structure.

Fig. 7 shows the large signal manual mapping across the 4-inch 3 nm AlN/GaN wafer. Several tenths of devices with similar design ($2 \times 50 \mu\text{m}$, $L_G = 110 \text{ nm}$, $L_{GD} = 1 \mu\text{m}$) have been measured across the wafer at 40 GHz with $V_{DS} = 20 \text{ V}$ under pulsed operation. We clearly observe an excellent yield and uniformity illustrated by a stable PAE/ P_{OUT} combination (mean PAE $\sim 70\%$, mean $P_{out} \sim 25 \text{ dBm}$). This power performance combination sets a new benchmark in Q-band as highlighted in Fig. 8.

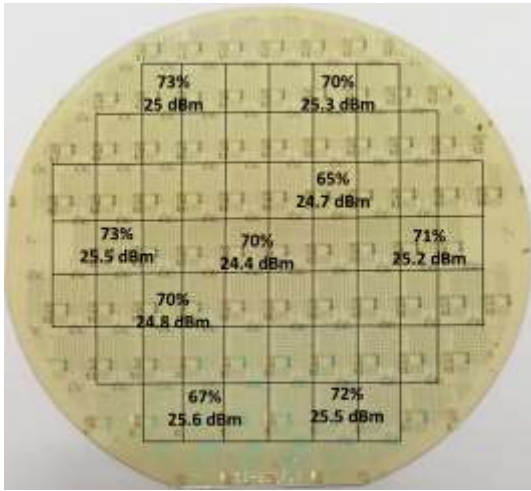


Fig. 7. Manuel mapping of 40 GHz pulsed large signal performances at $V_{DS} = 20V$ of the 3 nm AlN/GaN wafer with $L_G = 110$ nm and $L_{GD} = 1 \mu m$ (PAE matching).

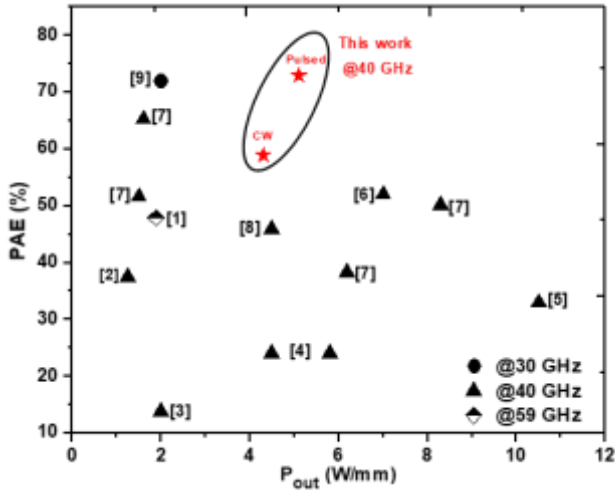


Fig. 8. Benchmark of GaN HEMT devices in Ka and Q-band.

IV. CONCLUSION

In this work, we performed a comparison between two AlN/GaN HEMT structures on 4-inch SiC substrate using a 3 nm and 4 nm barrier thickness. The power performances of both structures demonstrated the benefit of the AlN barrier layer. However, the 4 nm AlN/GaN structure shows a poor device robustness with a strong degradation after large signal measurements. On the other hand, the 3 nm AlN/GaN structure delivered unprecedented performances at 40 GHz with high drain bias on the full 4-inch wafer while showing a promising device robustness. This is attributed to the strain reduction when using thinner AlN barrier layer (closer to the critical thickness). These results pave the way for next generation of high power MMICs operating in the millimeter-wave range with significantly higher efficiencies than current state-of-the-art.

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