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# Giant step-bunching occurrence during graphene growth on 4H-SiC(0001)

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## Motivations

The main obstacle to the use of graphene on the industrial scale is the growth of a large and homogenous monolayer graphene. Concerning this issue, it is worth noting that our group has recently developed a reproducible and controlled growth process of a monolayer graphene on SiC(0001) by sublimation at low Ar pressure. i.e. 10 mbar [1]. Still, the control of the electronic properties of the obtained graphene by this process is very challenging. E.g. the mobility on our graphene on 4H-SiC(0001) is around  $2000 \text{ cm}^2\text{v}^{-1}\text{s}^{-1}$  at RT which is in the range of the measured mobilities on similar substrates [2]. Yet, it is still very low when compared with the mobilities reported for suspended graphene [3]. It is well accepted that the electronic properties of graphene on SiC are highly sensitive to the substrate underneath. It was reported that the mobility of graphene on SiC(0001) increases with increasing SiC steps width, and its resistance increases with increasing SiC steps height [4;5]. This means that the electronic properties of graphene on SiC(0001) can be tuned by controlling the height and width of the terraces that results from the surface reconstruction of SiC before the growth i.e. Step bunching phenomenon.

## State of the art : Step bunching on SiC(0001)

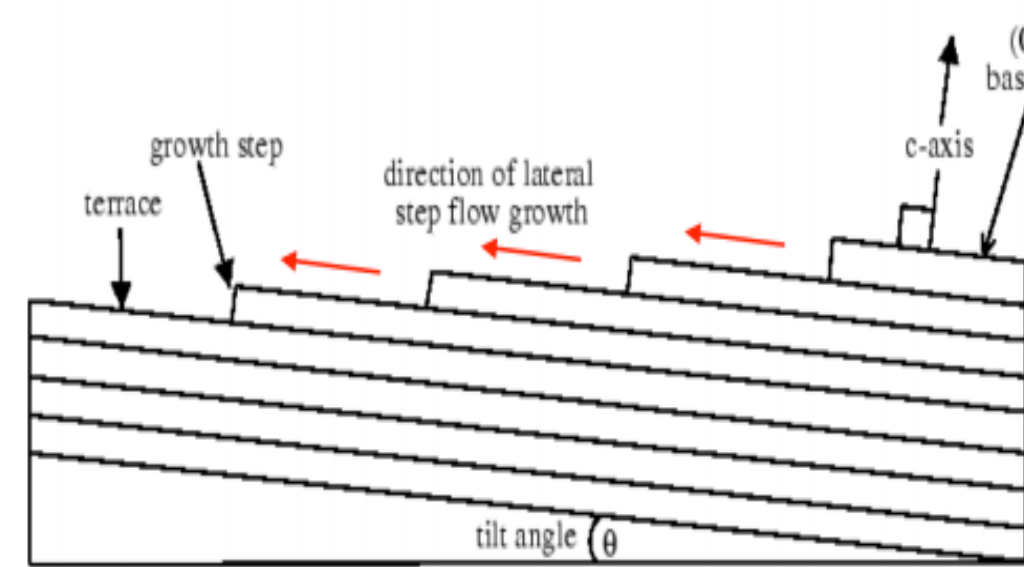
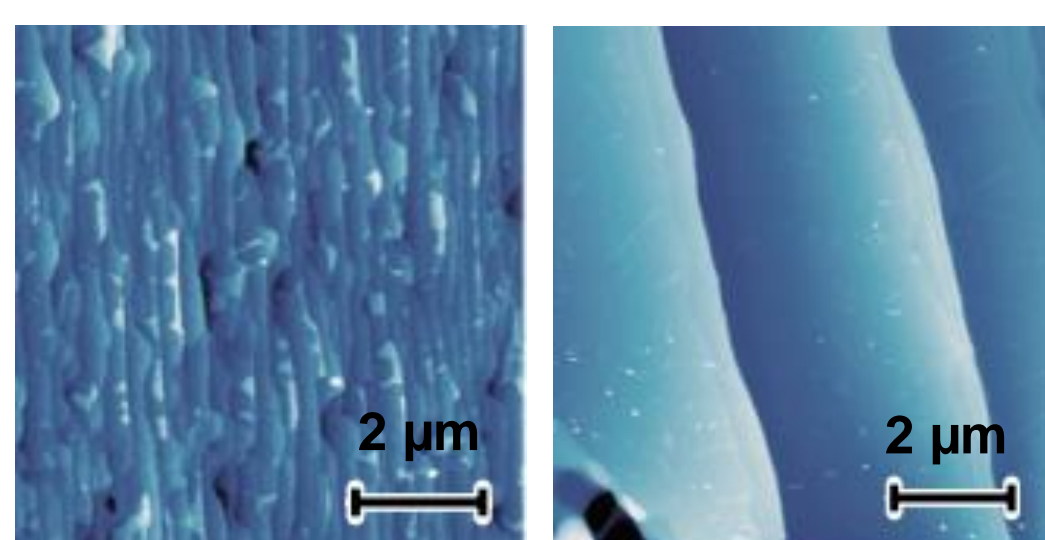
Movement of the surface atoms at high temperature and the formation of high steps and wide terraces

H. Matsunami et al, *Materials Science and Engineering: R: Reports*. 1997, 20, 25–166

How to control step bunching on SiC(0001) ?

- Temperature ramp
- Miscut angle ( $\theta$ )
- H<sub>2</sub> etching

1 °C/s      0.66 °C/s



- Remove polishing damages

G.R. Yazdi et al, *Carbon*. 2013, 57, 477–484

- Delay the buffer layer graphene formation

Kruskopf et al, *Thin solid films*. 2018, 659, 7–15

Steps width increases with lowering the temperature ramp

Bao et al, *Appl. Phys. Lett.* 2016, 109, 081602

The width of terraces is sensitive to SiC miscut angle even if "small" ( $\theta < 0.1^\circ$ )

Dimitrakopoulos et al, *Appl. Phys. Lett.* 2011, 98, 22105

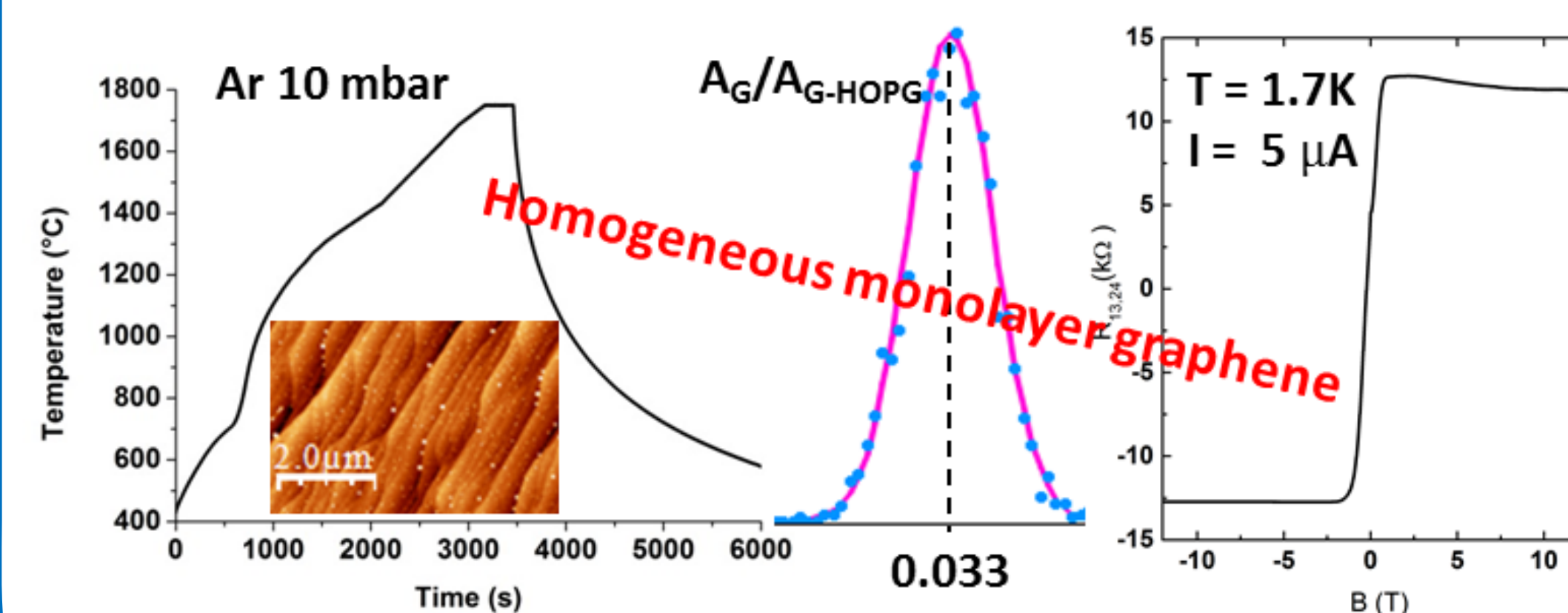
## Our sublimation process to grow graphene

### HTA-100 characteristics (prototype)

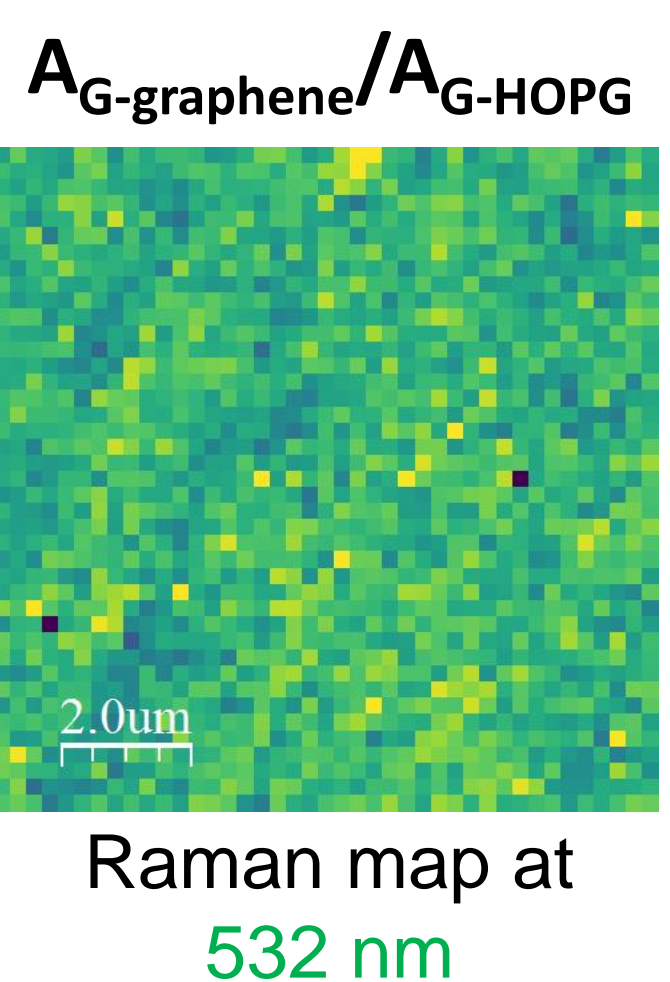
Gas lines: Ar, N<sub>2</sub>, CH<sub>4</sub>, C<sub>2</sub>H<sub>4</sub>, C<sub>3</sub>H<sub>8</sub>, H<sub>2</sub>  
Stainless steel water-cooled chamber  
Up to 2000°C  
Ramp rate up to 10 °C/s  
Vacuum range: Atmosphere to 10<sup>-6</sup> Torr  
Sublimation or CVD



### Growth process: 10 mbar, 1750°C



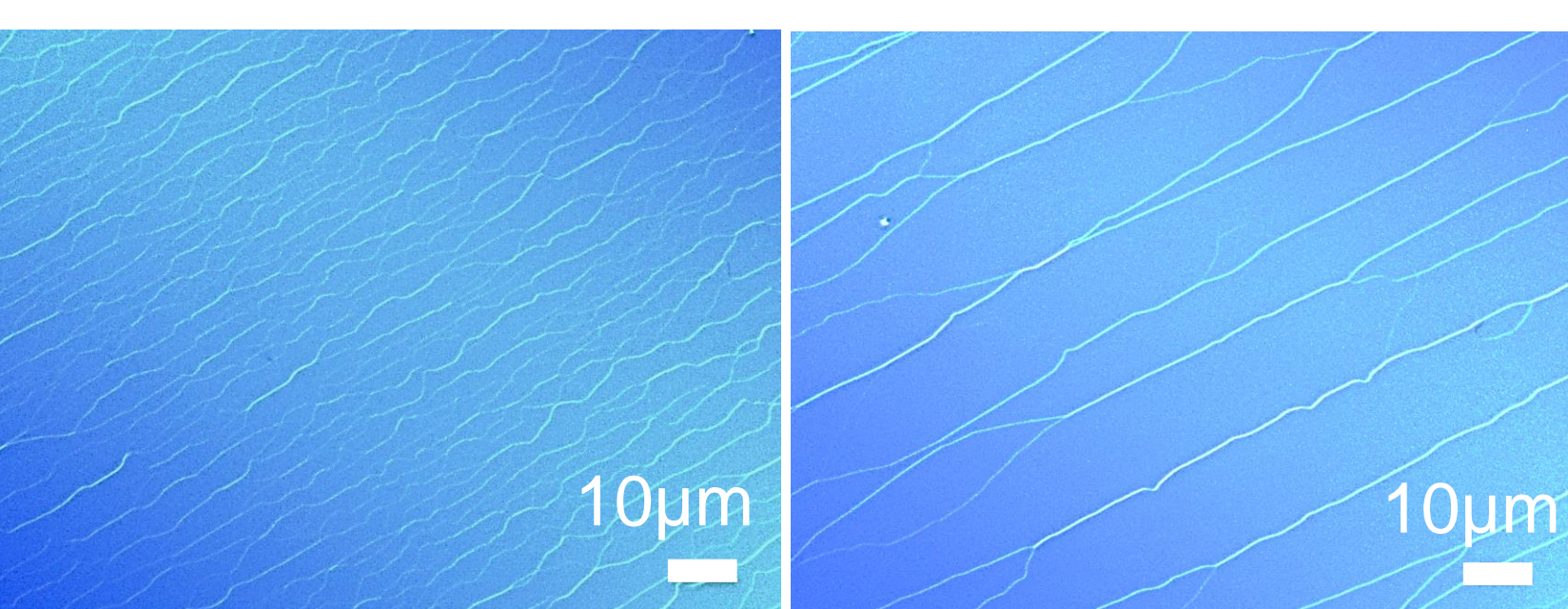
P. Landois et al, *Phys. Chem. Chem. Phys.*, 2017, 19, 15833–15841  
N. Camara, *Phys. Rev. B*, 2009, 80, 125410



## H<sub>2</sub> etching

- Evidence of H<sub>2</sub> effect by MO (DIC)

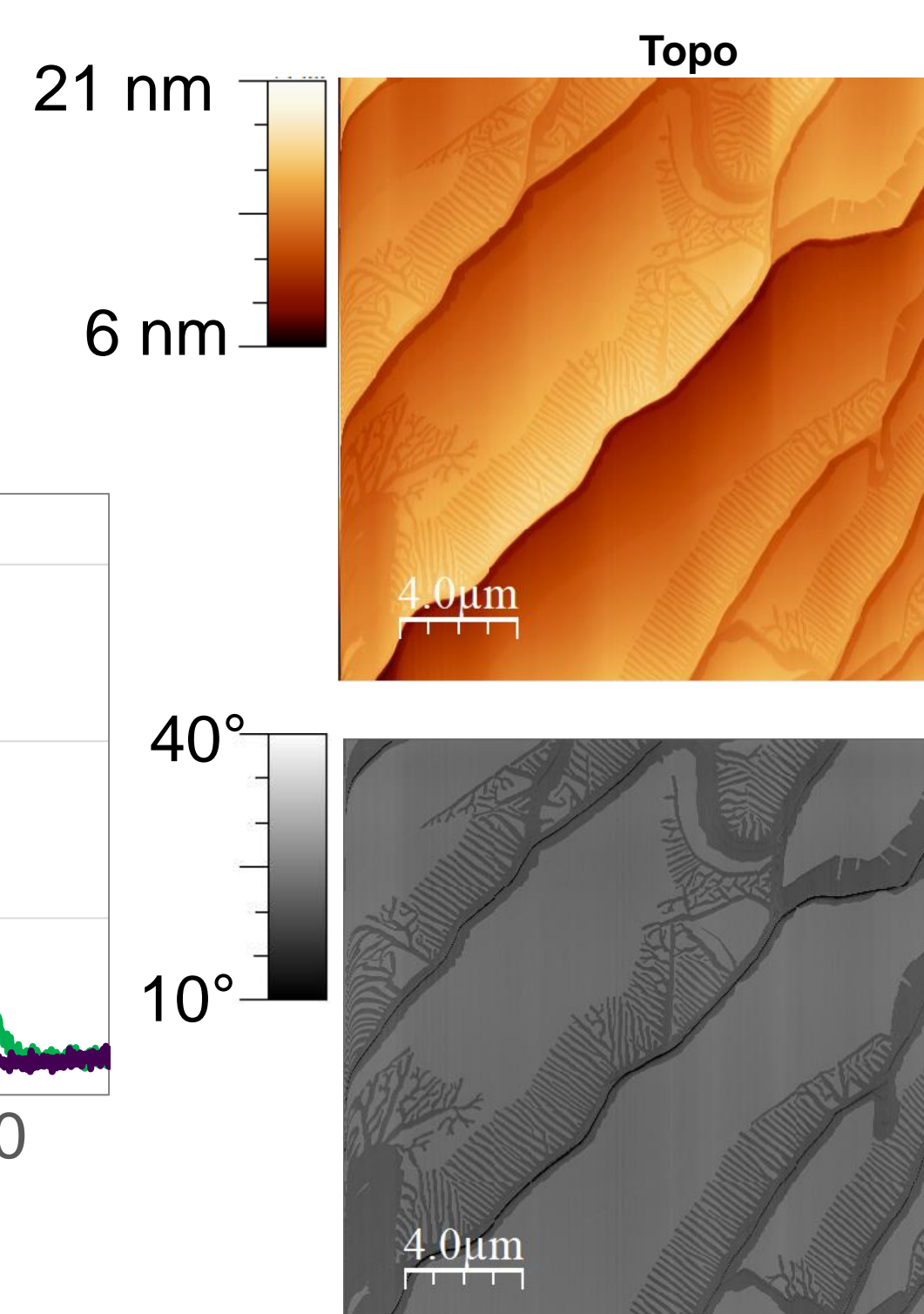
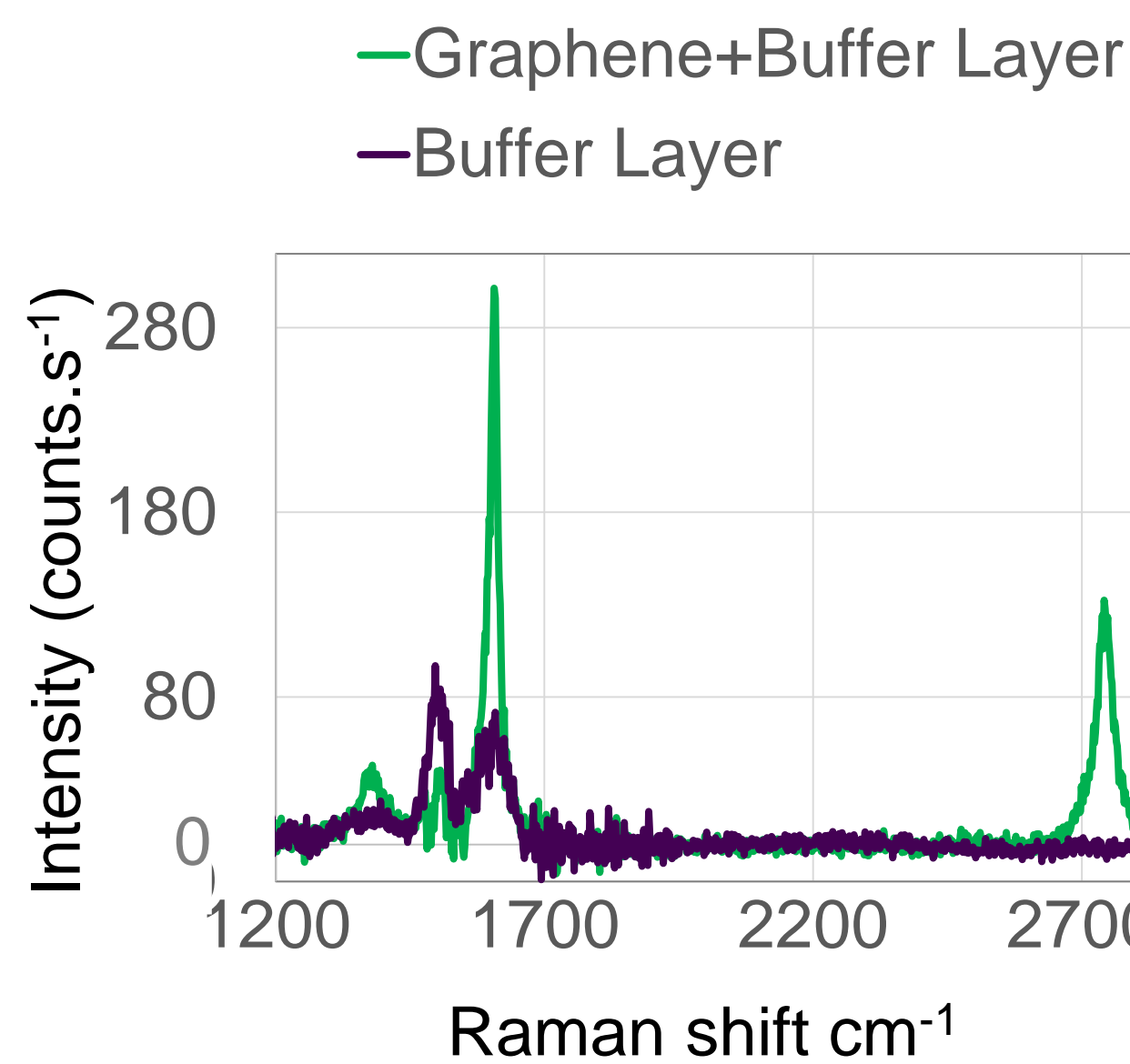
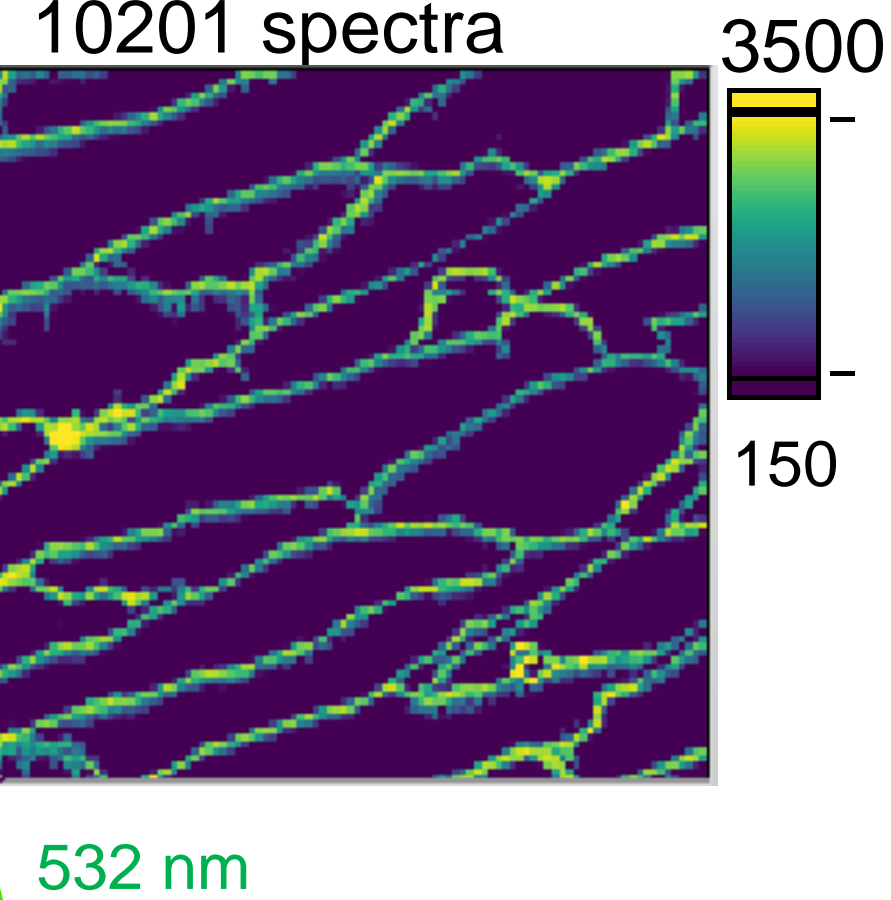
Without H<sub>2</sub>      With H<sub>2</sub>



Large terraces up to 15 μm with H<sub>2</sub> covered with buffer layer

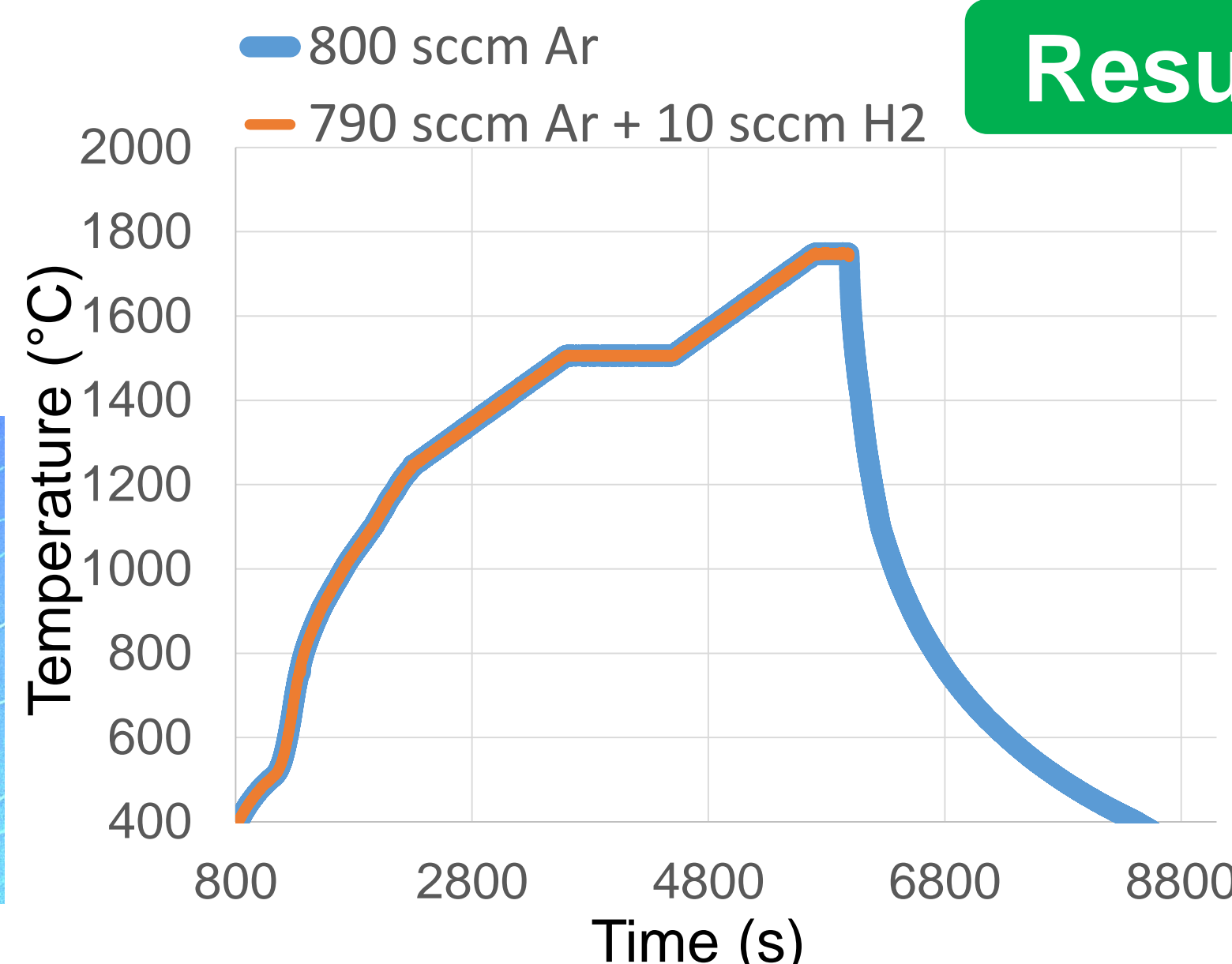
- Terraces characterizations: Raman and AFM, complementary techniques

A<sub>2D</sub> counts.s<sup>-1</sup>.cm<sup>-1</sup>  
(50 μm x 50 μm)  
10201 spectra

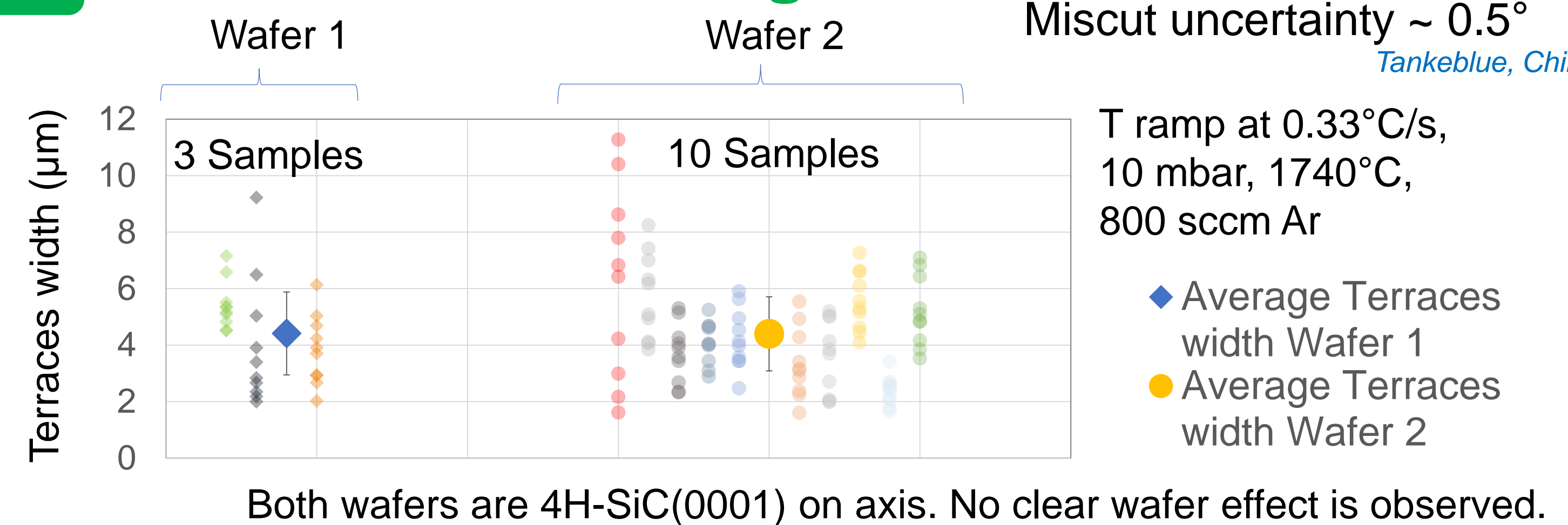


Graphene formation delayed

## Results



## Wafer miscut Angle



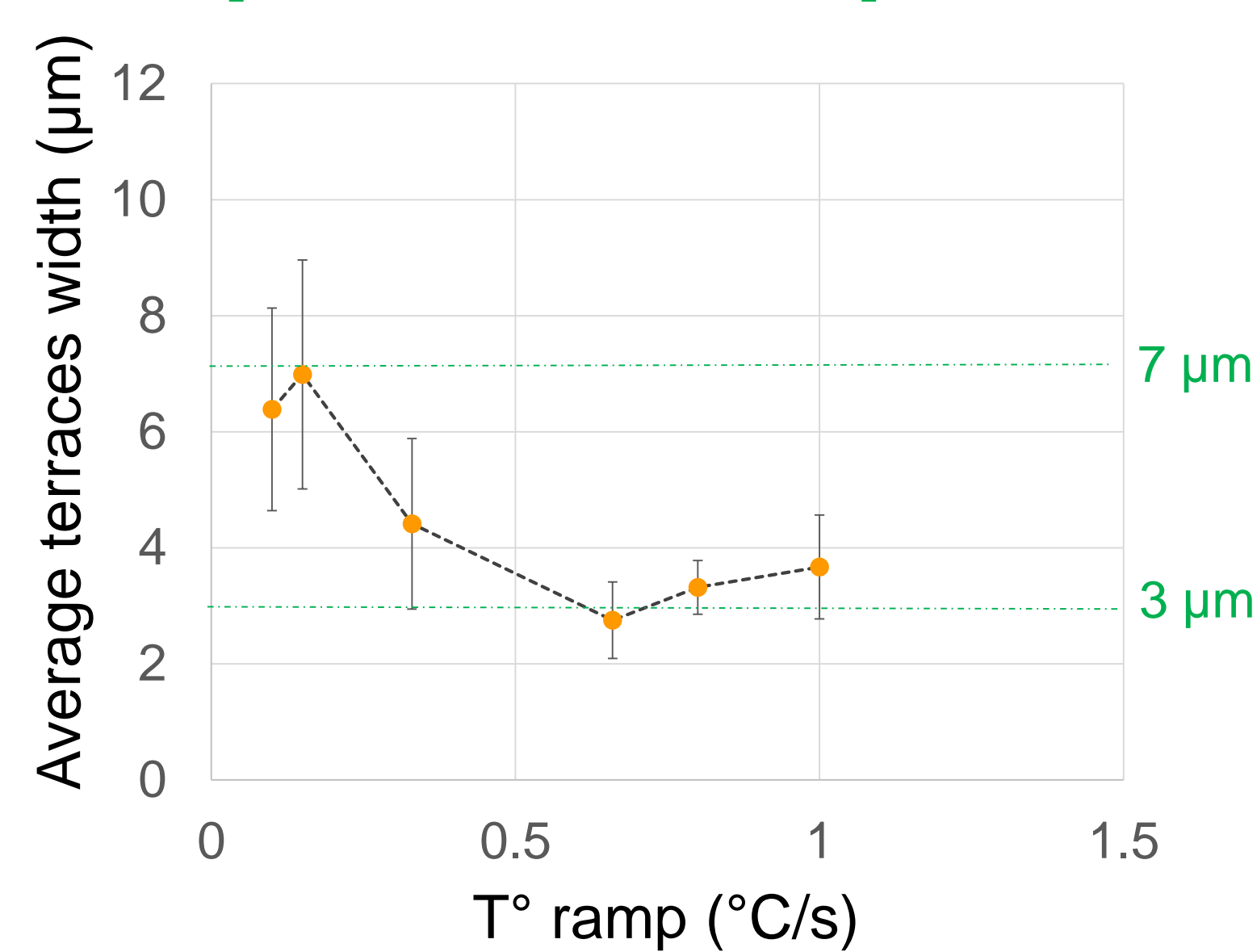
Both wafers are 4H-SiC(0001) on axis. No clear wafer effect is observed.

Perspectives

- Others 4H
- 4H vs 6H
- HR-XRD to determine the miscut with an uncertainty around 0.015

J Enslin et al *Phys. Status Solidi A*. 2019, 216, 1900682

## Temperature ramp effect



Larger terraces at low T ramp confirming our previous results

Tianlin wang, thesis, University of Montpellier, 2018

## Conclusions and perspectives

We have identified in the state of art the parameters allowing the control of step bunching on SiC(0001). We have started testing some of those parameters (temperature ramp, H<sub>2</sub> etching...) and regular steps with a width up to 15 μm have been obtained. As far as we know, our steps are by far larger than those reported in the literature i.e. 100 of nanometers to some μm. The main challenge now would be to cover the large steps by monolayer graphene. Once a reproducible and well controlled process is identified, we will measure the electronic properties of the obtained graphene. At the same time we are exploring some alternative ways to enhance the electronic properties of our graphene such as limiting the buffer layer effect and optimizing the growth on the C face of SiC.

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- [2] E. Arslan et al *Electron. Mater. Lett.* 2014, 10, 387
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- [4] Dimitrakopoulos et al *Appl. Phys. Lett.* 2011, 98, 22105
- [5] F.M. Ross et al *Nature Mater.* 2012, 11 114–119