Selective GaN sublimation and local area regrowth for co-integration of enhancement mode and depletion mode Al(Ga)N/GaN high electron mobility transistors

Thi Huong Ngo, Rémi Comyn, Sébastien Chenot, Julien Brault, Benjamin Damilano, Stéphane Vézian, Eric Frayssinet, Flavien Cozette, Christophe Rodriguez, N. Defrance, et al.

Selective GaN sublimation and local area regrowth for co-integration of enhancement mode and depletion mode Al(Ga)N/GaN high electron mobility transistors

Thi Huong Ngo[1], Rémi Comyn[1], Sébastien Chenot[1], Julien Brault[1], Benjamin Damilano[1], Stéphane Vézian[1], Eric Frayssinet[1], Flavien Cozette[2], Christophe Rodriguez[2], Nicolas Defrance[3], François Lecourt[4], Nathalie Labat[5], Hassan Maher[2] and Yvon Cordier[1]*

1-Université Côte d'Azur, CNRS, CRHEA, rue Bernard Grégory, 06560 Valbonne, France

2-Laboratoire Nanotechnologies Nanosystèmes, CNRS-UMI-3463, Institut Interdisciplinaire d'Innovation Technologique (3IT), Université de Sherbrooke, 3000 Bd de l'université, Sherbrooke, J1KOA5, QC, Canada.

3-CNRS-IEMN – Université de Lille, UMR8520, Av. Poincaré, 59650 Villeneuve d'Ascq, France

4-OMMIC, 94450 Limeil-Brévannes, France

5-Laboratoire de l'Intégration du Matériau au Système, Université de Bordeaux, Talence, France

*Corresponding author: yc@crhea.cnrs.fr

Abstract:

In this paper, we report on the fabrication of a normally-off Al(Ga)N/GaN high electron mobility transistor with selective area sublimation under vacuum of the p type doped GaN cap layer. This soft method makes it possible to avoid damages otherwise induced by post processing with reactive ion etching techniques. The GaN evaporation selectivity is demonstrated on AlN as well as on AlGaN barrier layers. Furthermore, by properly choosing the AlGaN barrier thickness and composition it is possible to co-integrate a normally-off with a normally-on device on the same substrate. Finally, a local area regrowth of AlGaN can complement this process to increase the maximum drain current in the transistors.

HEMT, Normally-off, Normally-on, GaN, sublimation, epitaxy.

I. INTRODUCTION

Gallium nitride (GaN) is a wide bandgap semiconductor of choice for high-frequency and high-power applications [1], [2] thanks to its outstanding material properties (high breakdown voltage, high electron velocity and good thermal conductivity). The standard AlGaN/GaN High Electron Mobility Transistor (HEMT) device is a depletion-mode (D-mode) transistor also called normally-on. However, enhancement-mode (E-mode) or normally-off transistors are required for several applications. First, they are preferred for safe power switch applications [3]. Second the co-integration of E-mode with D-mode devices is desirable for analog and digital applications where one can simplify the design of direct-coupled FET logic (DCFL) circuits [4-5], as well as to simplify the design for RF and microwave circuits [6]. Several schemes have been explored to shift the threshold voltage V_{th} from the naturally negative towards a positive value and then to fabricate an E-mode transistor. A first way consists of

fluorine implantation [6-9] to introduce negative charges inside the barrier but the thermal stability of this process is often under debate. A second way consists of the partial or total etching of the barrier to achieve a gate recess [10-14]. Tri-gate topologies have also been developed to enhance the carrier confinement and V_{th} shift [15]. Yet, another way to shift V_{th} is to introduce additional layers such as p-doped GaN or InGaN on top of the barrier layer [16-20]. However, such layers need to be removed from the transistor access regions to allow the electron current between source and drain. Like for the gate recess, plasma based etching induces some degradation at the surface of the barrier layer [21]. To overcome this problem, the digital etching (DE) process has been developed [22-23]. The self-limiting nature of the DE process based on plasma oxidation and wet oxide removal permits an accurate control of the etching. However, the drawback of this method is that the removal is limited to less than 1 nm per step, which makes the process fastidious in the case of thick cap layers. In order to tackle this limitation, we have developed an original process based on the selective evaporation of GaN caps [24]. We show that a dielectric mask can be patterned to define the region where GaN sublimates. The evaporation stops when the AlN or AlGaN barrier layer is reached and according to previous studies, submicron features can be obtained with selective evaporation [25] which may offer solutions for various applications. The first part of the paper describes this process. In the second part, we show how local evaporation of the p-GaN cap layer can be obtained in the access regions of the normally-off transistor with micrometric gate patterns as well as in adjacent larger areas for exposing the normally-on structure, so that D-mode and E-mode devices are co-integrated on the same substrate. In the third part, we show preliminary results on the local area regrowth of AlGaN developed in order to complement the evaporation process approach to increase the maximum drain current in both E and D mode devices.

II. SELECTIVE AREA SUBLIMATION

The selective evaporation of GaN is performed in a Riber Compact 21 molecular beam epitaxy (MBE) reactor equipped with a turbomolecular pumping unit able to produce a base pressure below 10^{-10} Torr. The reactor uses NH_3 as the nitrogen source [26]. The process starts with the deposition of a dielectric mask. In the present study, SiO_2 with a typical thickness of 50-100 nm is deposited on the GaN surface. After pattern definition in the photoresist by UV-photolithography, the pattern is transferred by reactive ion etching using $Cl_2/Ar/CH_4$ gas mixture until the top of the GaN layer is reached. Then, the photoresist is removed, and the sample is cleaned with oxygen plasma and hydrochloric acid prior to introduction into the MBE reactor. The sample is outgassed up to 500°C under high vacuum in the preparation chamber. After this step, it is introduced into the growth chamber and heated up to the evaporation temperature. Figure 1.a shows the reflection high energy electron diffraction (RHEED) pattern of the GaN surface prior to the evaporation. The streaky pattern confirms the smoothness of the surface. The sample temperature is slightly below 900°C but the presence of NH_3 (200 sccm flow rate) induces a pressure of $4x10^{-6}$ Torr that is sufficient to prevent GaN from evaporation. After the NH_3 supply is stopped, one rapidly notices the change of the RHEED pattern that becomes spotty due to the roughening of the surface (Figure 1.b) while the residual pressure induced by ammonia drops down to a few 10^{-8} Torr. One can notice on Figure 1.c, a change of the RHEED pattern where the streaky pattern reappears and spots vanish. This slow process continues until a streaky pattern is entirely recovered, in 50-60 min for the present case (Figure 1.d).

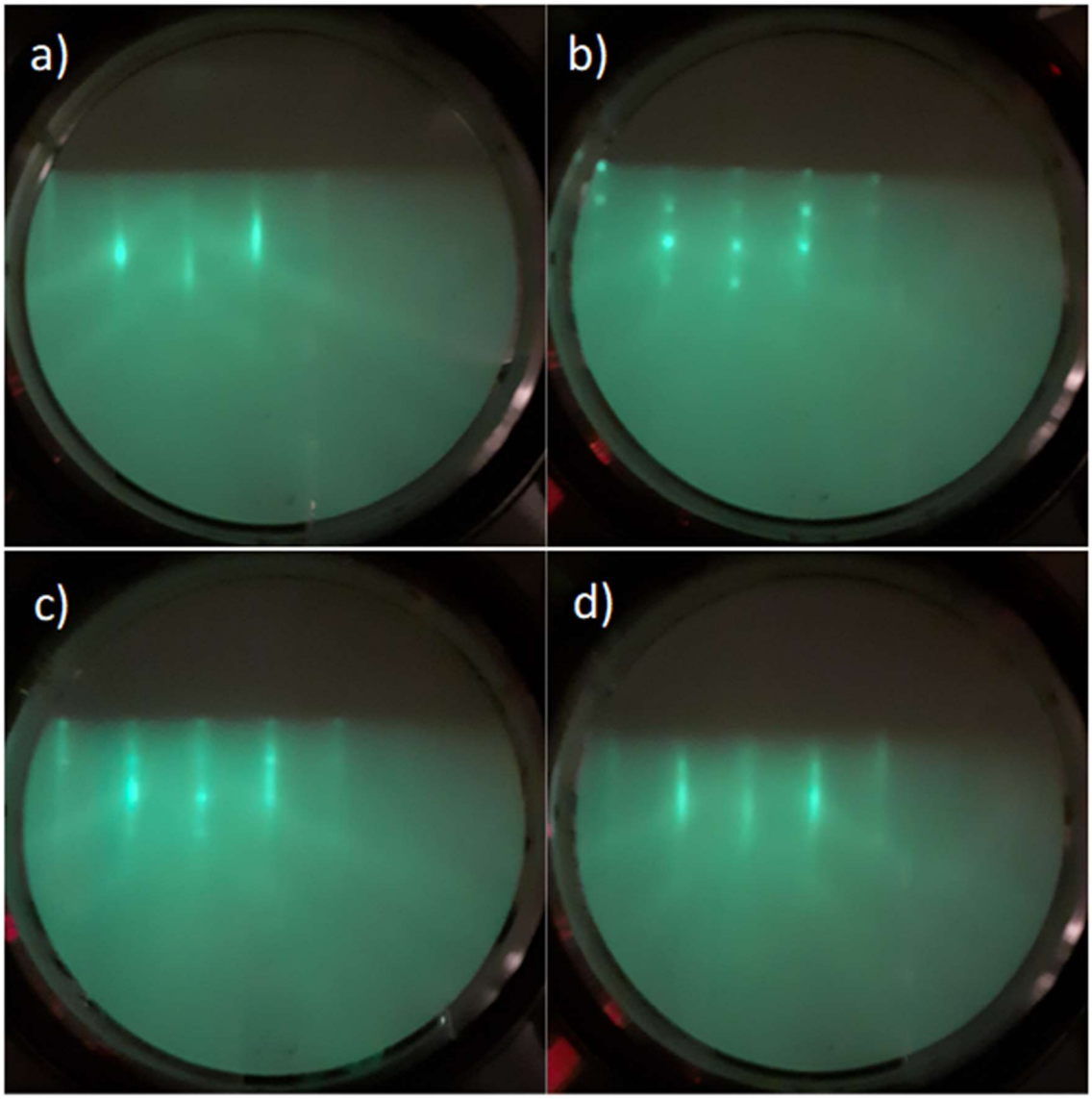

Figure 1. RHEED patterns of the surface at 900°C: a) GaN under NH_3; b) 1 mn c) 15 min and d) 50 min after closing the NH_3 supply.

The present sample consists of a 50 nm GaN cap deposited on a 2 nm AlN barrier layer grown on a GaN buffer layer. These layers have been grown previously in the same MBE reactor. The evolution of the RHEED patterns can be explained by the fact that sublimation of the GaN layer occurs with the formation of 3D islands (Figure 2.a). GaN sublimates preferentially in the vicinity of defects and non-volatile impurities can act as nanomasks restricting the sublimation [27]. Furthermore, semi-polar and non-polar crystallographic planes in GaN are more stable against evaporation than polar ones. For these reasons, GaN 3D islands appear more or less randomly at the surface [28]. When the deeper grooves reach the AlN layer underneath, the local evaporation stops and the sublimation of islands continues slowly to reduce their height and their lateral size. This progressively gives place to a flat surface leading to the recovery of a streaky RHEED pattern. One noticeable point is that the time necessary to eliminate all these islands is much longer than the one expected from the 3D sublimation rate calibrations shown in Figure 2.b. Indeed, it has been shown that the activation energy for the sublimation of the {1-103} planes is higher than for the (0001) plane [29].

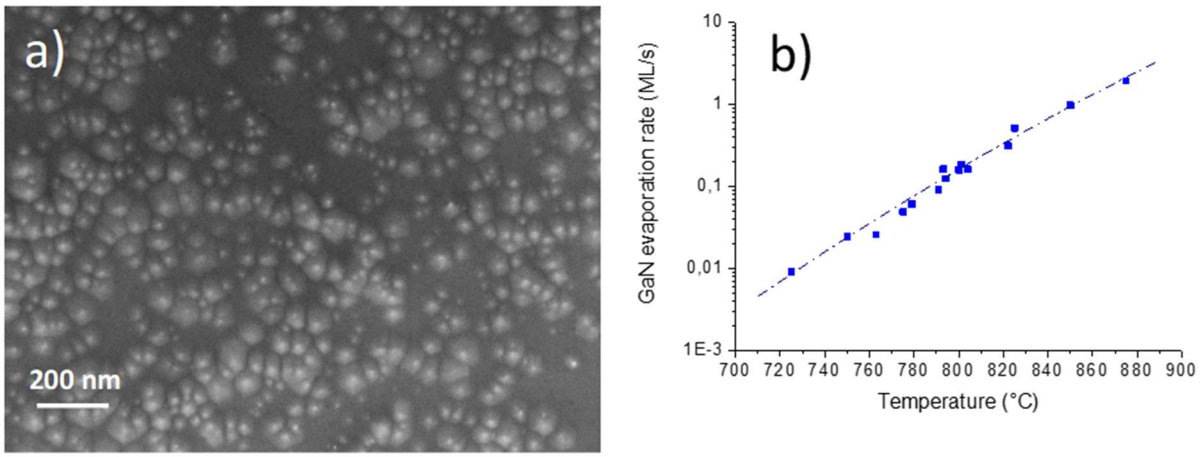

Figure 2. a) SEM view of the surface of partially evaporated GaN; b) GaN evaporation rate as a function of temperature.

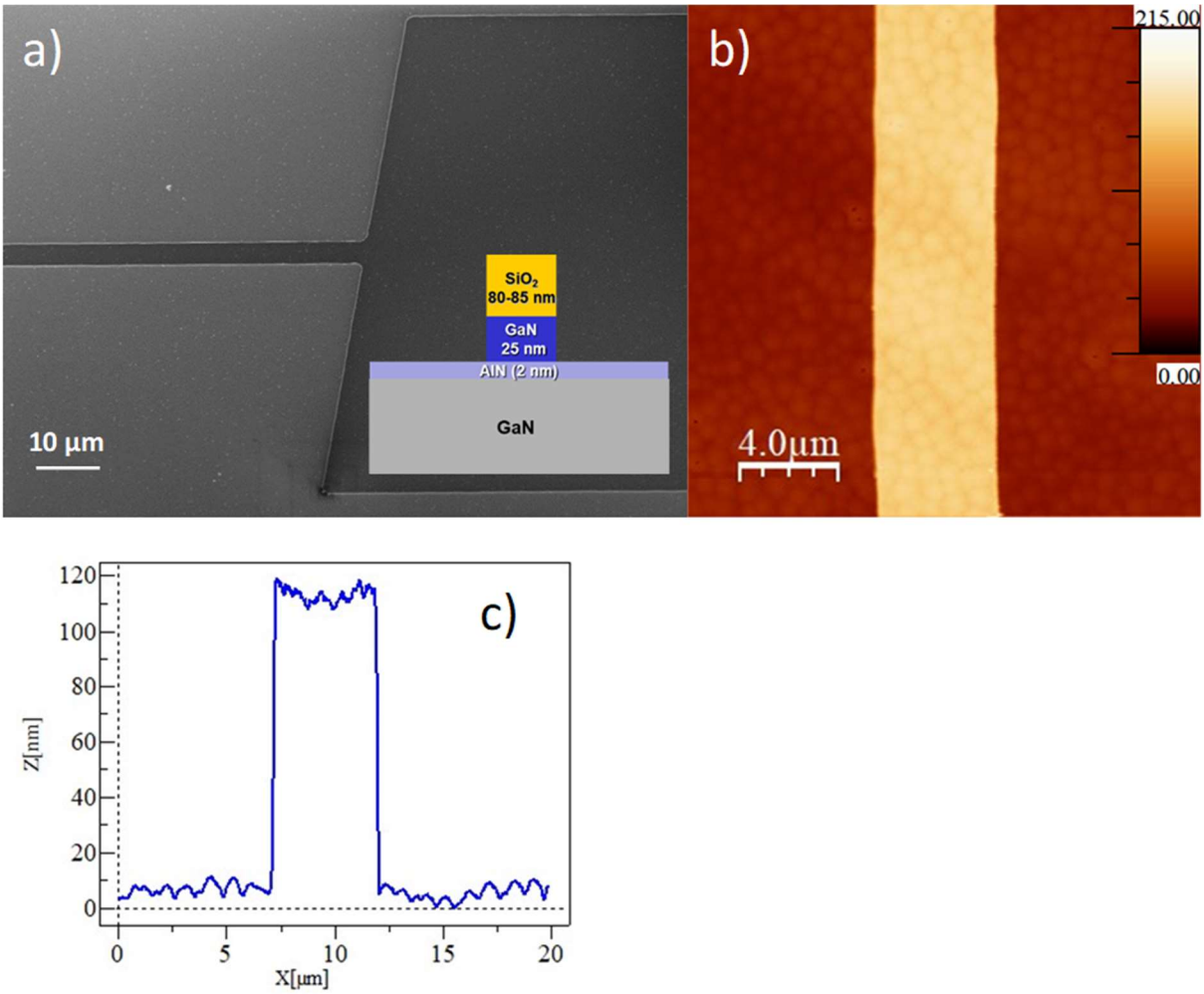

Figure 3. a) Scanning electron microscope view of a gate pattern after complete evaporation of a 25 nm GaN cap on a 2 nm AlN layer covered with 80-85 nm SiO_2 mask (the inset shows the schematic of the HEMT with evaporated GaN cap); b) Atomic Force Microscopy view of the same (z-scale 215 nm); c) height profile of the gate pattern.

Figure 3 shows details of a gate pattern after evaporation of another sample consisting of 25 nm GaN cap covered with 80-85 nm SiO_2 mask. The underlying barrier is a 2 nm AlN on GaN also. The scanning

electron microscope (SEM) and atomic force microscope (AFM) images confirm that an island-free surface can be obtained around the gate finger and its pad still protected with the SiO_2 mask. Furthermore, the height profile measured across the gate finger indicates a total height of 105-115 nm after evaporation which confirms the evaporation of the totality of the 25 nm GaN cap. One can notice that even in the region covered with the SiO_2 mask the typical morphology of GaN layers grown with NH_3 source MBE is present and consists of mounds with a typical diameter of 1 µm resulting in a root mean square roughness (RMS) below 5 nm [30]. This morphology doesn't affect the electron mobility of the two-dimensional electron gas (2DEG) as shown in our previous studies. For instance, electron mobility in the range of 1900-2000 $cm^2/V.s$ has been obtained at room temperature in a HEMT grown on Silicon substrate. At liquid Helium temperature, the mobility reached 8500-13700 $cm^2/V.s$ on Silicon substrate and 30 000 $cm^2/V.s$ on a GaN-on-sapphire template [31-32]. We also notice that the evaporation of the GaN cap layer did not change the morphology.

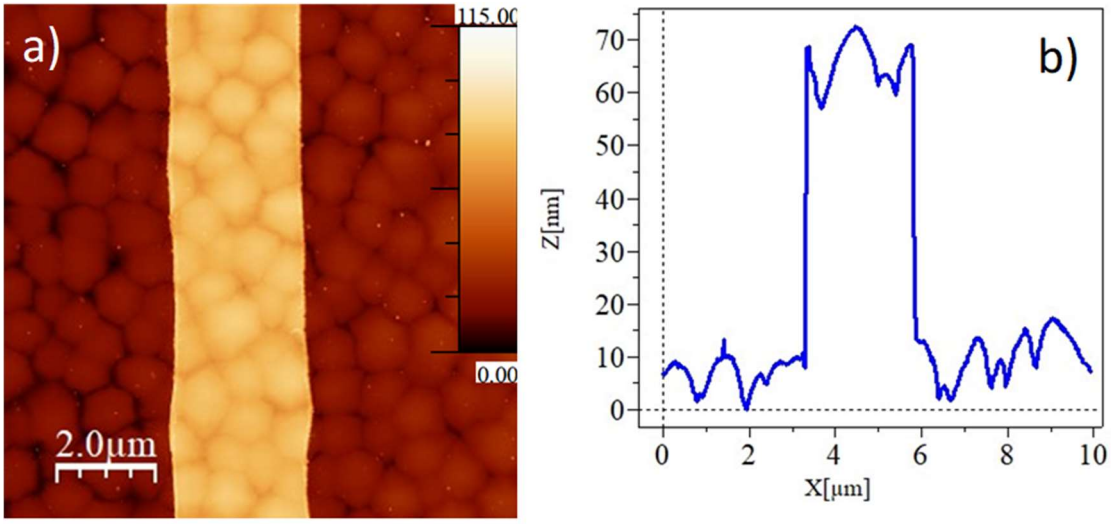

Figure 4. a) Atomic Force Microscopy view (z-scale is 115 nm) of a gate pattern after complete evaporation of a 50 nm GaN cap on a 15 nm AlGaN layer ; b) height profile of the gate pattern after removal of the SiO_2 mask.

A crucial point for the selective evaporation is that temperatures in the range of 800-900°C enable the thermal decomposition of GaN under high vacuum at rates ranging from 0.1 ML/s (~0.025 nm/s) up to more than 1 ML/s, but that they are still too low to decompose the SiO_2 mask and the AlN layer. The strong chemical bond between Al and N atoms explains the large selectivity previously observed with the 2 nm AlN barrier: it behaves like an etch-stop layer towards this thermal etching process. However, the SiO_2 layer should not be so stable under high vacuum and we explain the observed stability with a partial conversion of the mask material into Silicon Nitride when it is exposed to NH_3. A similar process has been applied to evaporate a 50 nm GaN cap layer grown on an AlGaN barrier layer with 26% Al nominal content. Figure 4 shows that the evaporation of the GaN cap is selective with respect to AlGaN. Here, the SiO_2 mask has been removed prior to AFM analysis. Thus, the process temperature is probably too low to evaporate aluminium atoms from an AlGaN matrix. If we assume that aluminium atoms did not evaporate, it is probable that 4 molecular monolayers of the alloy converted to 1 monolayer of AlN which reduces the total thickness of the barrier layer by less than 1 nm. This point is interesting because it makes the process possible for HEMT structures with a wide range of Al content and barrier thickness. In particular, even when normally-off HEMTs have been demonstrated with AlN barriers [33], the leakage current through extremely thin layers as well as the sensitivity to surface

states are of major concern. Similar concerns apply to the co-integration of normally-off HEMTs with normally-on ones [34]. In view of the evaluation of the device structures, we used a maskset defined with 4 x 4 mm² cells containing process and material test devices as well as gated TLM (transmission line method) patterns. As shown in Figure 5.a, only half of the cells were still covered with the SiO_2 mask prior to the evaporation of the GaN cap layer, so that at the end, a chessboard of cap-free normally-on stacks and p-GaN gate normally-off structures was generated.

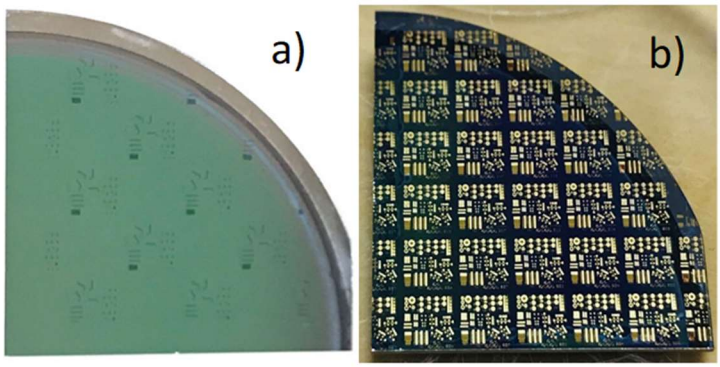

Figure 5. a) Photography of a quarter 2.in substrate prepared for GaN selective evaporation; b) Photography of a quarter 2.in substrate after the device process.

III. DEVICE PROCESS

The three structures studied were HEMTs grown with a 50 nm GaN cap on a 2 in. Si(111) substrate. The two first structures contain 2 nm and 2.5 nm AlN barriers respectively whereas the last one is a 15 nm $Al_{0.26}Ga_{0.74}N$ barrier HEMT. The structures were grown by NH_3 MBE in the Compact 21 reactor with a 1.5 µm GaN buffer on an AlN/AlGaN/AlN stress mitigating stack. Due to the lack of availability of a p-type doping source in the present MBE reactor, the p-GaN cap layer was grown in another MBE reactor (Riber 32P). The the p-GaN cap was doped with magnesium. However, contrary to the Compact 21 reactor [26], the growth in this reactor is not uniform with about 20% thickness variation between the centre and the edge of the substrate with the most important variation beyond 10 mm from the centre. The magnesium flux was chosen to obtain a net acceptor concentration of $3.5x10^{18}/cm^3$ at the centre of the substrate as measured by C-V at low frequencies (20-100 Hz) on calibration samples [35]. As previously described, a 50 nm thick SiO_2 mask was deposited and patterned prior to selective evaporation. After the latter step, the SiO_2 mask was removed in a buffered oxide etchant (BOE 7:1) solution. The device process is achieved with UV-photolithography and an AZ5214 resist. Isolation is performed with RIE etching of a 150 nm depth mesa using a $Cl_2/Ar/CH_4$ gas mixture. Ohmic contacts are formed after deposition of a Ti/Al/Ni/Au sequence in an e-beam evaporator followed by thermal annealing for 30s at 750°C in nitrogen atmosphere. The gate contact consists of a Ni/Au sequence evaporated on AlGaN for depletion mode devices and on p-GaN for enhancement mode ones. Finally, an additional Ni/Au sequence is deposited on the pads of the gates as well as on the ohmic contacts to facilitate electrical measurements which are made with needle probes on a Karl Süss EP4 probe station. SEM views of the gated TLM pattern are shown in Figure 6. The lateral size of the patterns is 150 µm. Figures 6.b and 6.c show details of the gate deposited between source and drain ohmic contacts. For this trial, no additional maskset was fabricated so that the main difficulty was to realign the metal gate pattern with the edges of the p-GaN protected from evaporation (Figure 6.c). On this maskset, nominal gate lengths are 1 µm, 2 µm and 4 µm and the width is 150 µm. Gates are centred between ohmic contacts with nominal distances varying from 2 µm up to 6 µm for each side. However,

our lithography process was not able to maintain such distances and resulted in longer gates within smaller source to drain spacings. To limit effects due to the variation of pattern size and alignment we chose to investigate transistors with nominally 2 µm gate length and 10 µm source to drain spacing, resulting in 2,5 µm gates within 9.5 µm source to drain spacing.

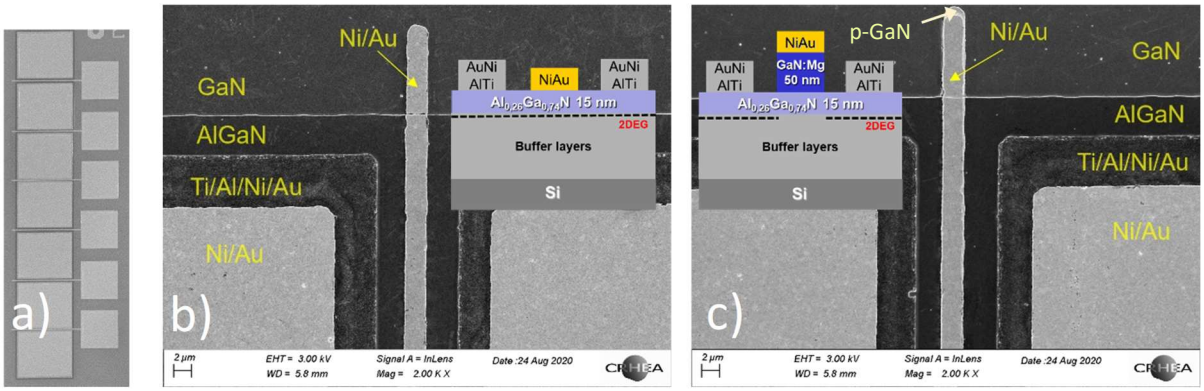

Figure 6. a) SEM overview of a gated TLM device; b) detailed SEM view of a normally-on device; c) detailed SEM view of a normally-off device. The insets show the schematic cross section of the devices.

Depletion mode device:

We first focus on the AlN barrier structures. C-V measurements performed with a mercury probe after the p-GaN regrowth revealed the presence of a two-dimensional electron gas with a density around $1.5x10^{12}/cm^2$ and a threshold voltage of -1.8 V for the 2.5 nm AlN barrier HEMT. On the other hand, C-V measurements have shown that the channel was completely depleted in the 2 nm barrier HEMT, meaning that it is a normally-off structure. However, we did not succeed in obtaining good electrical contacts with this structure after evaporation of the p-GaN cap, so we cannot evaluate the electrical characteristics. On the contrary, ohmic contacts have been obtained with the 2.5 nm AlN structure. The contact resistance extracted from ungated TLM devices is around 1.7 Ohm.mm while the sheet resistance is about 1 kOhm/sq. Hall effect measurements performed on Van der Pauw patterns show that the 2DEG has a sheet carrier density of about $5x10^{12}/cm^2$ with resulting mobility around 1000 $cm^2/V.s$, which attests to the quality of the evaporated structure [36]. Thus, a clear effect of the p-GaN cap on the 2DEG sheet carrier concentration is obtained and the removal of the p-GaN cap layer is achieved with a resulting good transport property AlN/GaN heterojunction. Unfortunately, we did not succeed in depositing good quality NiAu Schottky contacts on this sample.

Then, we analysed the electrical characteristics of the 15 nm $Al_{0.26}Ga_{0.74}N$ barrier HEMT. Figure 7 shows DC output and transfer characteristics of a D-mode transistor. The maximum drain current I_{ds} at V_{gs}=0V is 116 mA/mm and reaches 360 mA/mm at V_{gs}=+2V while the gate leakage remains negligible at 140 nA/mm. As expected, the threshold voltage is negative (V_{th}~-1.5V) but less than the one previously obtained by C-V with a mercury probe prior to p-GaN growth which showed the presence of a two-dimensional electron gas with a density around $5x10^{12}/cm^2$ and a threshold voltage of -2 V. This may be due to a larger Schottky barrier height with Ni and to the previously mentioned slight reduction of barrier thickness. This behaviour is confirmed with a 100 µm diameter Schottky diode fabricated on the AlGaN barrier in the region where p-GaN was evaporated. As shown in the inset of Figure 8, the threshold voltage extracted from the C-V measurement is around -1.5 V. Furthermore, a minimum net donor concentration of 10^{14} $/cm^3$ in the GaN buffer layer is extracted as well as a 2DEG sheet carrier concentration of $5x10^{12}/cm^2$. On the other hand, the 2DEG sheet carrier concentration deduced from Hall effect measurements on Van der Pauw patterns is between 4.3 and $5x10^{12}/cm^2$ and the sheet

resistance is in the 800-900 Ohm/sq range. The sheet resistance deduced from the measurements on ungated TLM devices with contact spacings varying from 5 µm to 40 µm is in the same range. Extrapolation of the resistances indicates contact resistances around 0.5 Ohm.mm. These resistances result in total access resistances of more than 3 Ohm.mm which explains the resulting current density in the transistors. A total resistance R_{on} of 7 Ohm.mm is deduced from the slope of the linear region of output characteristics I_{ds}-V_{ds}. The stability of the drain current against V_{ds} and V_{gs} bias is also shown. The maximum transconductance at V_{ds}=6V is around 130 mS/mm. The breakdown voltage defined at I_{ds}=1mA/mm has been measured for a gate bias of -3V and increasing the drain bias up to 200V, the limit of our equipment. A large breakdown voltage is not expected with this structure which was grown with a 1.5 µm thick GaN buffer. Albeit some transistors present limited breakdown capability in the 50-75 V range, others like the one presented in Figure 7 reached the limit of 200V (Figure 9.a). On the other hand, the lateral breakdown voltage of the buffer layer measured between two ohmic contacts separated by a 10 µm distance mesa is between 90 V and 200 V (Figure 9.b). These results show that in spite of the evaporation of the GaN cap and the absence of deposition of a passivation layer, stable characteristics can be obtained. This confirms the absence of large damage introduced by the present soft thermal etching process.

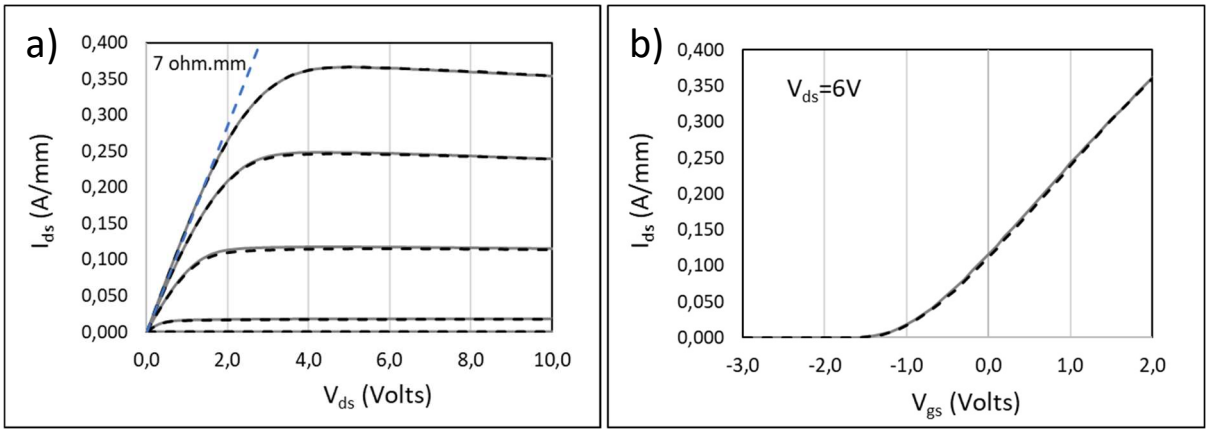

Figure 7. a) DC output characteristics of a 2 µm nominal gate D-mode transistor; b) transfer characteristics recorded at V_{ds} =6V; for both: continuous line (V_{gs}: +2V to -3V), dashed line (V_{gs}:-3V to +2V).

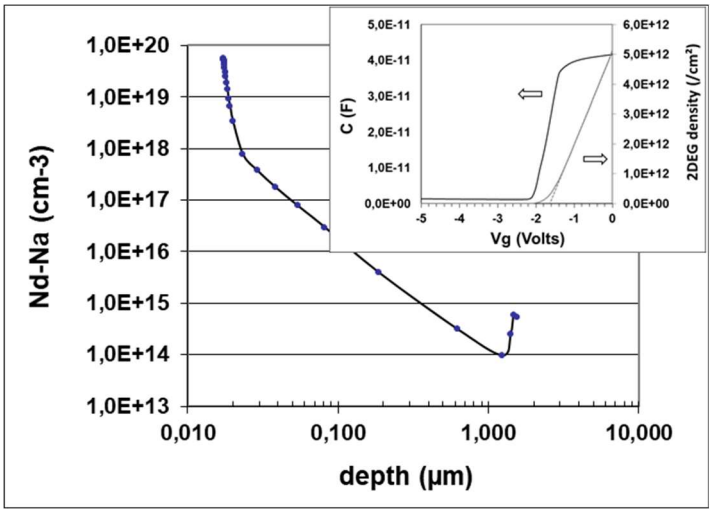

Figure 8. Net donor concentration profile N_d-N_a extracted from the C-V measured on a Schottky diode fabricated on the 15 nm $Al_{0.26}Ga_{0.74}N$ barrier HEMT after p-GaN evaporation. The inset shows the C-V profile as well as the 2DEG density profile.

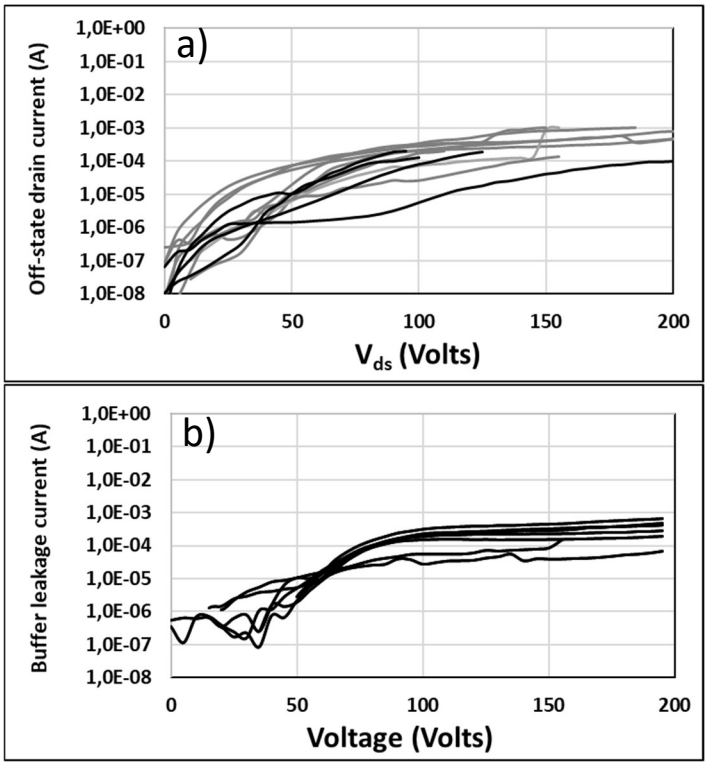

Figure 9. a) Off-state drain leakage current in the D-mode transistors (black lines) and E-mode transistors (gray lines); b) buffer leakage current measured on 300 µm periphery isolation patterns.

Enhancement mode device:

The DC output and transfer characteristics of an E-mode transistor fabricated on the same 15 nm $Al_{0.26}Ga_{0.74}N$ barrier HEMT wafer are shown in Figure 10. The gate length, its development and contact distances are the same as those of the D-mode device. The V_{gs} bias was increased from 0V up to +3V before it was reduced to 0V. Compared to Figure 7 where the gate was biased from +2V down to -3V and then increased to +2V, one can notice a slight hysteresis of the drain current I_{ds}. This limited shift of the characteristics attests again to the limited damages induced by the evaporation process in the vicinity of the gate. On the other hand, one can notice the shift by at least +1.5 V of the threshold voltage between this normally-off device and the normally-on one. This large shift confirms the effectiveness of introducing a p-GaN cap under the gate to shift the threshold voltage towards positive values. Furthermore, the same HEMT structure grown with a non-intentionally doped 50 nm thick GaN cap without any interruptions exhibits a threshold voltage V_{th} of -1.7 V according to mercury probe C-V measurements. This represents a limited shift of +0.3 V compared to the one due to the introduction of the p-type doping (>+1.5V). Despite the previously mentioned non-uniformity of the p-GaN layer over the substrate, a moderate dispersion of the drain current is noticed for transistors from an area of less than 12 mm from the centre (Figure 10.c). We also emphasize that the regrowth of the p-GaN cap in a separate reactor after exposure to air certainly introduced a silicon contamination as previously observed [37]. Thus, the growth of the p-GaN capped HEMT structure without any interruption would certainly result in an even larger positive shift of V_{th}. Furthermore, another interest of the present solution is that a gate bias V_{gs} of +2V makes it possible to obtain a drain current of 175-185 mA/mm and that a bias of +3V allows to reach 245-289 mA/mm without the penalty of a large gate leakage as shown in Figure 10.d. This behaviour is interesting for the integration of E-mode with

D-mode transistors requiring rather balanced currents or power. A total resistance R_{on} of 10 Ohm.mm is deduced from the slope of the linear region of output characteristics I_{ds}-V_{ds} shown in Figure 10.a. At V_{ds}=6V the transconductance is maximum around 100-115 mS/mm for V_{gs}~+1.5 V. The off-state behaviour of these E-mode transistors is quite similar to the one previously observed on D-mode devices with a breakdown voltage ranging from 80 V to 160 V (Figure 9a).

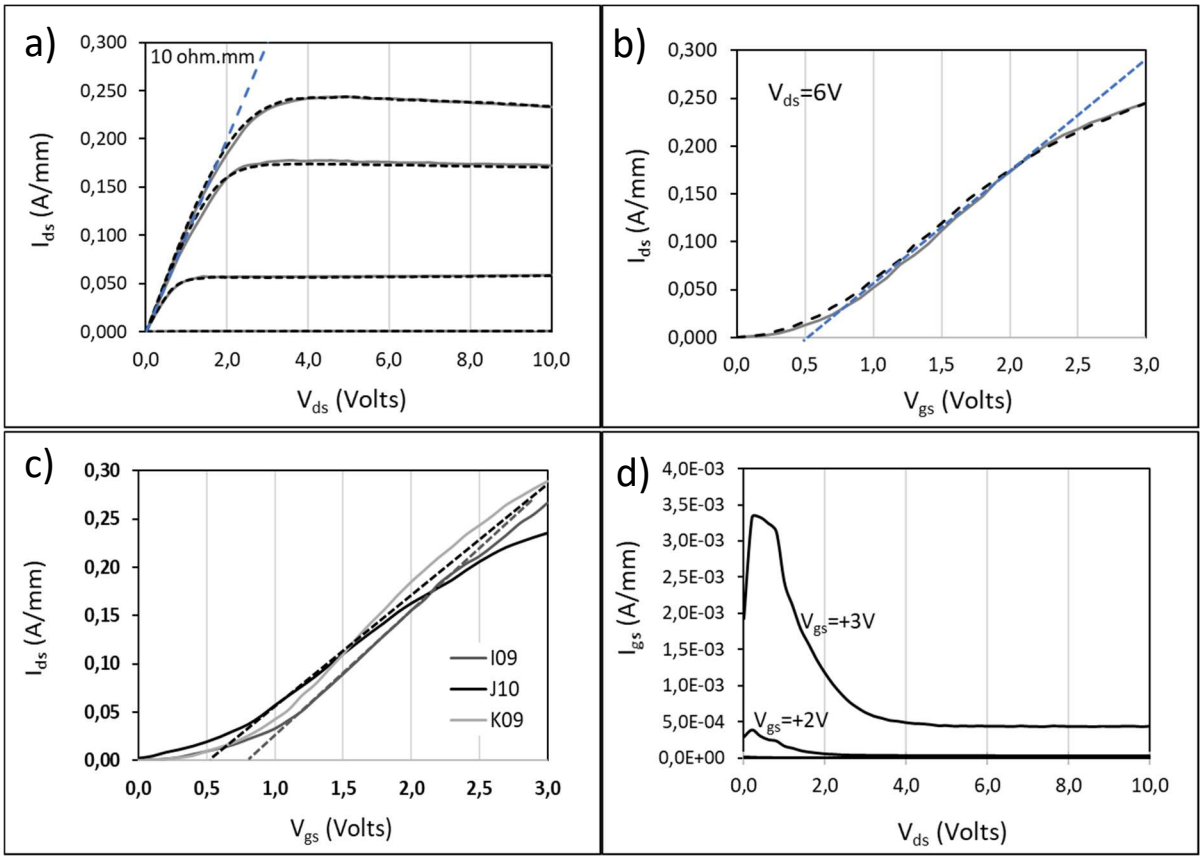

Figure 10. a) DC output characteristics of a 2 µm nominal gate E-mode transistor; b) transfer characteristics recorded at V_{ds}=6V; for both: continuous line (V_{gs}: 0V to +3V), dashed line (V_{gs}:+3V to 0V); c) transfer characteristics recorded on different transistors from an area of less than 12 mm from the centre of the substrate; d) gate leakage current.

Complementary routes employing AlGaN regrowth:

AlGaN barrier thickening may also be envisaged after the p-GaN cap evaporation. This will increase the sheet carrier density in the access regions of the E-mode device as well as in the channel of the D-mode one. This results in an increase of the maximum drain current without affecting the threshold voltage V_{th} of E-mode transistors. For D-mode transistors, this would increase the maximum drain current as well but would shift V_{th} towards more negative values. The idea of AlGaN regrowth has been proposed for normally-off MIS-HEMTs [38] and demonstrated with Metal Organic Chemical Vapor Deposition (MOCVD) techniques after RIE etching of AlGaN barrier. In our case, the Normally-off structure is a 5 nm $Al_{0.21}Ga_{0.79}N$ barrier HEMT capped with 2 nm GaN. The structure was grown by MOCVD with an initial surface RMS roughness of 2 nm for 10 µm x 10 µm area AFM scans. The SiO_2/SiN_x mask deposited by sputtering with total thickness of 80-85 nm is patterned by photolithography as previously described (chessboard with 4 mm size cells). As previously, the sample is outgassed under vacuum prior to introduction into the MBE growth chamber where it is heated under NH_3. A streaky

RHEED pattern attests to a smooth and clean surface before the evaporation of the thin GaN cap and the regrowth of a 17 nm AlGaN layer capped with 3 nm GaN at 800°C. The AFM analysis of the regrown sample is reported in Figure 11 prior to the mask removal. The unchanged height unveils the absence of selectivity for AlGaN regrowth which sticks to SiO_2. Moreover, probably due to the insufficient thickness of the mask, the lift-off of this parasitic deposit appeared difficult for patterns such as transistor gates. Nevertheless, we succeeded in removing it in large areas and performed mercury probe measurements.

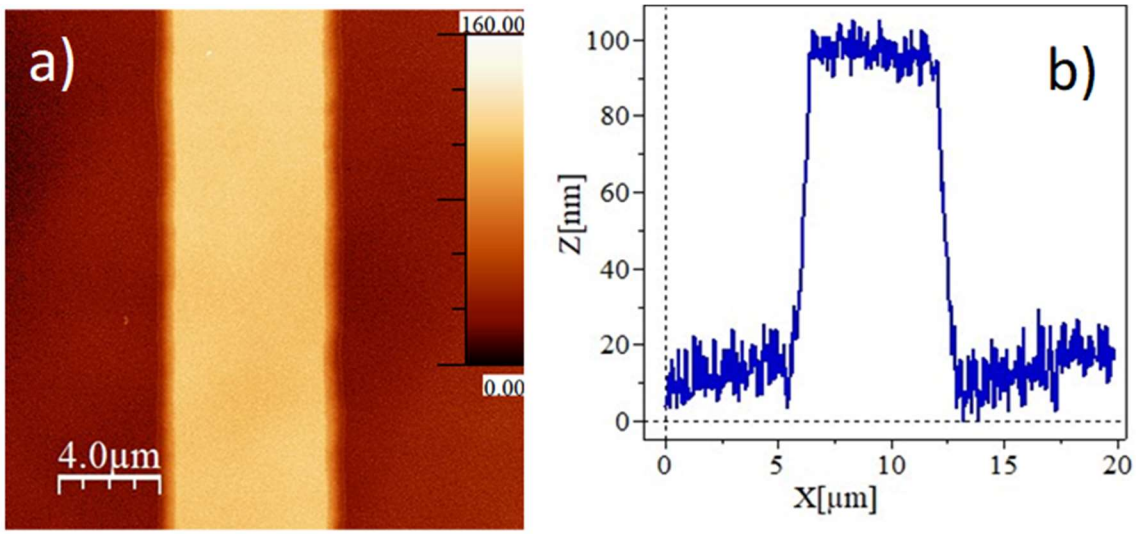

Figure 11. a) Atomic Force Microscopy view of the gate pattern and the access regions with regrown AlGaN (z-scale 160 nm); b) height profile of the gate pattern.

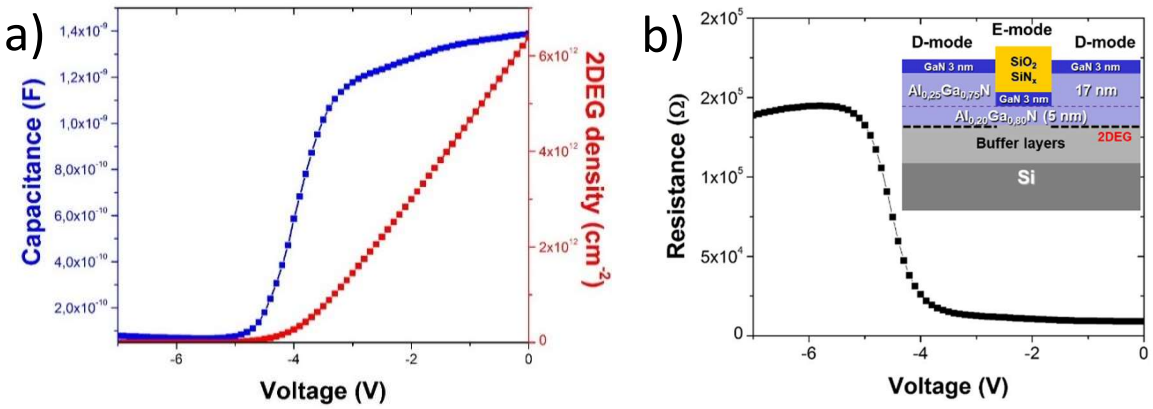

Figure 12. a) C-V profile and 2DEG density in the regrown AlGaN barrier HEMT area; b) parallel resistance deduced from the impedance (the inset shows the schematic of the co-integration of E-mode gate with D-mode regrown areas).

C-V measurements in areas previously protected by the SiO_2/SiN_x mask show that the 5 nm $Al_{0.21}Ga_{0.79}N$ barrier HEMT is still normally-off with a capacitance 25 pF (5 nF/cm²) corresponding to the total depletion of the structure. Furthermore, the series resistance extracted from the impedance is $\approx 10^8$ Ω confirming the high buffer layer resistivity. On the other hand, Figure 12.a shows the C-V profile

obtained in the regrown area. The capacitance was extracted from impedance measurements using a parallel equivalent circuit (C_p, R_p). One clearly sees the capacitance plateau due to the presence of the 2DEG and its pinch-off at a threshold voltage around -4 V. The integration of the capacitance from pinch-off up to 0 V produces a total charge superior to $6x10^{12}/cm^2$. On the other hand, the parallel resistance R_p which represents the inverse of the leakage of the diode drastically increases from more than 10 kOhm up to 0.2 MOhm at pinch-off (Figure 12.b). Considering the mercury dot size of about 0.8 mm, such resistances attest to the good quality of the electrical junction between the metal and the surface of the HEMT as well as the quality of the regrown HEMT structure itself. Even if the mask has to be optimized to demonstrate real devices, these preliminary results validate the idea of thickening the AlGaN barrier with a regrowth step that may be combined with p-GaN cap evaporation.

CONCLUSION:

In summary, we have developed a process to selectively evaporate the GaN cap of HEMTs. The selectivity operates with respect to dielectric masks and to Al containing barriers. We show that after selective area evaporation of the p-GaN cap of the HEMT structure, both depletion mode and enhancement mode transistors can be fabricated on the same substrate. Preliminary results on AlN/GaN HEMTs show that the 2DEG of a 2.5 nm AlN barrier HEMT presents good transport properties after evaporation of the p-GaN cap. Furthermore, the electrical characteristics of a 15 nm $Al_{0.26}Ga_{0.74}N$ barrier transistor with a selectively evaporated 50 nm p-GaN cap show a stable behaviour. A shift of the threshold voltage V_{th} superior to 1.5V is obtained between the cap-free transistor and the one having p-GaN under the gate. We speculate that this shift could be even larger in optimized structures grown without interruption. The relatively low gate leakage current allows the gate to be positively biased to obtain a large drain current in the normally-off (E-mode) transistor. Beyond the development of a normally-off device with a soft etching technique, the present method allows the co-integration of E-mode with D-mode transistors for advanced circuits. The demonstration of the proof of concept on transistors with a nominal gate length of 2 µm may be extended toward smaller dimensions depending on the lithography capability. Selective area evaporation of p-GaN cap with submicron gate patterns would open the possibility to fabricate enhancement mode HEMTs with GHz frequency capability and may lead to their co-integration with high frequency depletion mode devices into highly efficient RF circuits. After p-GaN cap evaporation, AlGaN barrier thickening can also be envisaged to increase the sheet carrier density in the access regions of the E-mode device as well as in the channel of the D-mode one. The combination of selective area sublimation with such selective area epitaxy can open new routes for the development of high-performance circuits for applications in the field of high power and high frequency electronics. Furthermore, the present sublimation process performed in an MBE reactor is compatible with in-situ deposition of SiN_x films that can be used as passivation layers to stabilize surface states and to further reduce access resistances.

ACKNOWLEDGEMENTS

This work was supported by French technology facility network RENATECH and the French National Research Agency (ANR) through the projects ED-GaN (ANR-16-CE24-0026-02) and the "Investissements d'Avenir" program GaNeX (ANR-11-LABX-0014). Prof. Borge Vinter is acknowledged for helpful reading of the manuscript.

REFERENCES

[1] P. Altuntas, F. Lecourt, A. Cutivet, N. Defrance, E. Okada, M. Lesecq, S. Rennesson, A. Agboton, Y. Cordier, V. Hoel and J.-C. De Jaeger, "Power Performance at 40 GHz of AlGaN/GaN High-Electron Mobility Transistors Grown by Molecular Beam Epitaxy on Si(111) Substrate," IEEE Electron Device Lett., vol. 36, no. 4, pp. 303–305, Apr. 2015, doi: 10.1109/LED.2015.2404358.

[2] R. Mitova, R. Ghosh, U. Mhaskar, D. Klikic, M.-X. Wang, and A. Dentella, "Investigations of 600-V GaN HEMT and GaN Diode for Power Converter Applications," IEEE Trans. Power Electron., vol. 29, no. 5, pp. 2441–2452, May 2014, doi: 10.1109/TPEL.2013.2286639.

[3] R. Chu, A. Corrion, M. Chen, R. Li, D. Wong, D. Zehnder, B. Hughes, K. Boutros, "1200-V Normally Off GaN-on-Si Field-Effect Transistors With Low Dynamic on -Resistance", IEEE Electron Device Lett., vol. 32, no. 5, pp. 632–634, May 2011, doi: 10.1109/LED.2011.2118190.

[4] M. Micovic, T. Tsen, M. Hu, P. Hashimoto, P.J. Willadsen, I. Milosavljevic, A. Schmitz, M. Antcliffe, D. Zhender, J.S. Moon, W.S. Wong, D. Chow, "GaN enhancement/depletion-mode FET logic for mixed signal applications" Electron. Lett., vol. 41, no. 19, pp. 1081–1083, Sep. 2005, doi: 10.1049/el:20052263.

[5] Y. Cai, Y. Zhou, K. J. Chen, and K. M. Lau, "High-Performance Enhancement-Mode AlGaN/GaN HEMTs Using Fluoride-Based Plasma Treatment", IEEE Electron Device Lett., vol. 26, n°7, JULY 2005 pp.435-437

[6] Z. H. Feng, R. Zhou, S. Y. Xie, J. Y. Yin, J. X. Fang, B. Liu, W. Zhou, Kevin J. Chen, S. J. Cai, "18-GHz 3.65-W/mm Enhancement-Mode AlGaN/GaN HFET Using Fluorine Plasma Ion Implantation", IEEE Electron Device Lett., vol. 31, no. 12, pp. 1386–1388, Dec. 2010, doi: 10.1109/LED.2010.2072901.

[7] Z. Tang, Q. Jiang, Y. Lu, S. Huang, S. Yang, X. Tang, K. J. Chen, "600-V Normally Off SiN_x/AlGaN/GaN MIS-HEMT With Large Gate Swing and Low Current Collapse", IEEE Electron Device Lett., vol. 34, no. 11, pp. 1373–1375, Nov. 2013, doi: 10.1109/LED.2013.2279846.

[8] Z. Xu, J. Wang, Y. Cai, J. Liu, Z. Yang, X. Li, M. Wang, Z. Yang, B. Xie, M. Yu, W. Wu, X. Ma, J. Zhang, Y. Hao, "300°C operation of normally-off AlGaN/GaN MOSFET with low leakage current and high on/off current ratio", Electron. Lett., vol. 50, no. 4, pp. 315–316, Feb. 2014, doi: 10.1049/el.2013.3928.

[9] T. Oka and T. Nozawa, "AlGaN/GaN Recessed MIS-Gate HFET With High-Threshold-Voltage Normally-Off Operation for Power Electronics Applications", IEEE Electron Device Lett., vol. 29, no. 7, pp. 668–670, Jul. 2008, doi: 10.1109/LED.2008.2000607.

[10] S. Liu, S. Yang, Z. Tang, Q. Jiang, C. Liu, M. Wang, K. J. Chen, "Al2O3/AlN/GaN MOS-Channel-HEMTs With an AlN Interfacial Layer", IEEE Electron Device Lett., vol. 35, no. 7, pp. 723–725, Jul. 2014, doi: 10.1109/LED.2014.2322379.

[11] Z. Xu, J. Wang, J. Liu, C. Jin, Y. Cai, Z. Yang, M. Wang, M. Yu, B. Xie, W. Wu, X. Ma, J. Zhang, Y. Hao, "Demonstration of Normally-Off Recess-Gated AlGaN/GaN MOSFET Using GaN Cap Layer as Recess Mask", IEEE Electron Device Lett., vol. 35, no. 12, pp. 1197–1199, Dec. 2014, doi: 10.1109/LED.2014.2359986.

[12] J. Kuzmik, C. Ostermaier, G. Pozzovivo, B. Basnar, W. Schrenk, J. Carlin, M. Gonschorek, E. Feltin, N. Grandjean, "Proposal and Performance Analysis of Normally Off GaN/InAlN/AlN/GaN HEMTs

With 1-nm-Thick InAlN Barrier", IEEE Trans. Electron Devices, vol. 57, no. 9, pp. 2144–2154, Sep. 2010, doi: 10.1109/TED.2010.2055292.

[13] Y. Kong, J. Zhou, C. Kong, X. Dong, Y. Zhang, H. Lu, and T. Chen, "Monolithic integrated enhancement/depletion-mode AlGaN/GaN high electron mobility transistors with cap layer engineering", Appl. Phys. Lett. 102, 043505 (2013); https://doi.org/10.1063/1.4789868

[14] M. Hua, J. Wei, G. Tang, Z. Zhang, Q. Qian, X. Cai, N. Wang, K. J. Chen, "Normally-Off LPCVD-SiNx/GaN MIS-FET With Crystalline Oxidation Interlayer", IEEE Electron Device Lett., vol. 38, no. 7, pp. 929–932, Jul. 2017, doi: 10.1109/LED.2017.2707473.

[15] W. Jatal, U. Baumann, H. O. Jacobs, F. Schwierz, and J. Pezoldt, "Enhancement- and depletion-mode AlGaN/GaN HEMTs on 3C-SiC(111)/Si(111) pseudosubstrates", Phys. Status Solidi A 214, No. 4, 1600415 (2017) / DOI 10.1002/pssa.201600415

[16] Y. Uemoto, M. Hikita, H. Ueno, H. Matsuo, H. Ishida, M. Yanagihara, T. Ueda, T. Tanaka, D. Ueda, "Gate Injection Transistor (GIT)—A Normally-Off AlGaN/GaN Power Transistor Using Conductivity Modulation", IEEE Trans. Electron Devices, vol. 54, no. 12, pp. 3393–3399, Dec. 2007, doi: 10.1109/TED.2007.908601.

[17] O. Hilt, A. Knauer, F. Brunner, E. Bahat-Treidel, and J. Würfl, "Normally-off AlGaN/GaN HFET with p-type Ga Gate and AlGaN buffer", in 2010 22nd International Symposium on Power Semiconductor Devices IC's (ISPSD), 2010, pp. 347–350.

[18] T. Mizutani, M. Ito, S. Kishimoto, and F. Nakamura, "AlGaN/GaN HEMTs With Thin InGaN Cap Layer for Normally Off Operation", IEEE Electron Device Lett., vol. 28, no. 7, pp. 549–551, Jul. 2007, doi: 10.1109/LED.2007.900202.

[19] Y. Zhong, S. Su, Y. Zhou, H. Gao, X. Chen, J. He, X. Zhan, Q. Sun, H. Yang, "Effect of Thermal Cleaning Prior to p-GaN Gate Regrowth for Normally Off High-Electron-Mobility Transistors", ACS Appl. Mater. Interfaces, vol. 11, no. 24, pp. 21982–21987, Jun. 2019, doi: 10.1021/acsami.9b03130.

[20] G. Greco, F. Iucolano, and F. Roccaforte, "Review of technology for normally-off HEMTs with p-GaN gate", Mater. Sci. Semicond. Process., vol. 78, pp. 96–106, May 2018, doi: 10.1016/j.mssp.2017.09.027.

[21] H. Hahn, G. Lükens, N. Ketteniss, H. Kalisch, and A. Vescan, "Recessed-Gate Enhancement-Mode AlGaN/GaN Heterostructure Field-Effect Transistors on Si with Record DC Performance", Appl. Phys. Express, vol. 4, no. 11, p. 114102, Nov. 2011, doi: 10.1143/APEX.4.114102.

[22] Y. Wang, M. Wang, B. Xie, C. P. Wen, J. Wang, Y. Hao, W. Wu, K. J. Chen, B. Shen, "High-Performance Normally-Off \Al2O3\GaN MOSFET Using a Wet Etching-Based Gate Recess Technique", IEEE Electron Device Lett., vol. 34, no. 11, pp. 1370–1372, Nov. 2013, doi: 10.1109/LED.2013.2279844.

[23] A. Chakroun, A. Jaouad, M. Bouchilaoun, O. Arenas, A. Soltani, and H. Maher, "Normally-off AlGaN/GaN MOS-HEMT using ultra-thin Al0.45Ga0.55N barrier layer", Phys. Status Solidi A, vol. 214, no. 8, p. n/a-n/a, Aug. 2017, doi: 10.1002/pssa.201600836.

[24] B. Damilano, S. Vézian, J. Brault, B. Alloing, and J. Massies, "Selective Area Sublimation: A Simple Top-down Route for GaN-Based Nanowire Fabrication", Nano Lett (2016), 16, 1863-1868

[25] B. Damilano, P.-M. Coulon, S. Vézian, V. Brändli, J.-Y. Duboz, J. Massies, P.A. Shields, "Top-down fabrication of GaN nano-laser arrays by displacement Talbot lithography and selective area sublimation", Appl. Phys. Express 12 045007 (2019)

[26] Y.Cordier, F.Pruvost, F.Semond, J.Massies, M.Leroux, P.Lorenzini, C.Chaix, “Quality and uniformity assessment of AlGaN/GaN Quantum Wells and HEMT heterostructures grown by molecular beam epitaxy with ammonia source”, Phys. Stat. Sol (c) 3 (2006) 2325-2328

[27] B. Damilano, S. Vézian, J. Massies, “Mesoporous GaN Made by Selective Area Sublimation for Efficient Light Emission on Si Substrate”, Phys. Stat. Solidi (b) 255, 1700392 (2018)

[28] B. Damilano, S. Vézian, M. Portail, B. Alloing, J. Brault, A. Courville, V. Brändli, M. Leroux, J. Massies, “Optical properties of InxGa1-xN/GaN quantum-disks obtained by selective area sublimation”, J. Cryst. Growth, 477,262, (2017)

[29] S. Fernández-Garrido, T. Auzelle, J. Lähnemann, K. Wimmer, A. Tahraoui, O. Brandt, “Top-down fabrication of ordered arrays of GaN nanowires by selective area sublimation”, Nanoscale Adv. 1, 1893–1900 (2019).

[30] S. Vézian, F. Natali, F. Semond, and J. Massies, “From spiral growth to kinetic roughening in molecular-beam epitaxy of GaN(0001)”, Phys. Rev. B 69 (2004) 125329.

[31] N.Baron, Y.Cordier, S.Chenot, P.Vennéguès, O.Tottereau, M.Leroux, F.Semond, and J.Massies, “The critical role of growth temperature on the structural and electrical properties of AlGaN/GaN high electron mobility transistor heterostructures grown on Si(111)”, Journal of Applied Physics 105, 033701 (2009).

[32] L. Bouguen, S. Contreras, B. Jouault, L. Konczewicz, J. Camassel, Y. Cordier, M. Azize, S. Chenot, N. Baron, “Investigation of AlGaN/AlN/GaN heterostructures for magnetic sensor application from liquid helium temperature to 300 °C”, Appl. Phys. Lett. 92, 043504 (2008).

[33] M. Higashiwaki, T. Mimura, and T. Matsui, “Enhancement-Mode AlN/GaN HFETs Using Cat-CVD SiN”, IEEE Trans. Electron Devices, vol. 54, no. 6, pp. 1566–1570, Jun. 2007, doi:10.1109/TED.2007.896607.

[34] D. F. Brown, K. Shinohara, A. Williams, I. Milosavljevic, R. Grabar, P. Hashimoto, P. J. Willadsen, A. Schmitz, A. L. Corrion, S. Kim, D. Regan, C. M. Butler, S. D. Burnham, and M. Micovic, “Monolithic Integration of Enhancement- and Depletion-Mode AlN/GaN/AlGaN DHFETs by Selective MBE Regrowth”, IEEE Trans. Electron Devices, vol. 58, no. 4, pp. 1063-1067, Apr. 2011; doi: 10.1109/TED.2011.2105268.

[35] S. Brochen, J. Brault, S. Chenot, A. Dussaigne, M. Leroux, and B. Damilano, “Dependence of the Mg-related acceptor ionization energy with the acceptor concentration in p-type GaN layers grown by molecular beam epitaxy”, Appl. Phys. Lett., 103 (2013) 032102

[36] T. Zimmermann, D. Deen, Y. Cao, J. Simon, P. Fay, D. Jena, and H. G. Xing, “AlN/GaN Insulated-Gate HEMTs With 2.3 A/mm Output Current and 480 mS/mm Transconductance”, IEEE Electron Device Lett., vol. 29, no. 7, pp. 661, July 2008

[37] Y.Cordier, M.Azize, N.Baron, S.Chenot, O.Tottereau, J.Massies, “AlGaN/GaN HEMTs regrown by MBE on epi-ready semi-insulating GaN-on-Sapphire with inhibited interface contamination”, J. Cryst. Growth 309, 1-7 (2007)

[38] J. T. Asubar, S. Kawabata, H. Tokuda, A. Yamamoto, and M. Kuzuhara, Enhancement-Mode AlGaN/GaN MIS-HEMTs With High V_{TH} and High ID_{max} Using Recessed-Structure With Regrown AlGaN Barrier, IEEE Electron Device Lett., vol. 41, no. 5, pp. 693-696, May. 2020