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Verilog-A modeling of avalanche dynamics and quenching in Single-Photon Avalanche Diodes

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Abstract—We present a SPAD Verilog-A model accounting for the temporal avalanche buildup and its statistics. This physics-based approach is benched on TCAD mixed-mode analyzing predictions, as well as measurements. The buildup that can be in the order of 50-100ps, affects the pulse width distribution which is experimentally verified. Furthermore, we address in details the voltage swing across the device from the avalanche to its quenching, with a view on power consumption impact. This model can help a chip designer to optimize circuits for quenching the diode.

I. INTRODUCTION

Single-Photon Avalanche Diodes (SPADs) are reverse-biased p-n junctions particularly profitable in Geiger mode. At this regime and when a large voltage is applied, the electric field in the depletion layer becomes strong enough that the charge carriers may acquire sufficient energy to trigger an avalanche through impact ionization mechanisms. Hence, when an absorbed photon leads to a photo electron-hole pair generation, an avalanche current rises swiftly and it has to be quenched using external readout electronics (Fig.1). Literature enumerates different types of quenching circuits for which a specific application is best-suited [1], and the SPAD related physics is reviewed by Spinelli and Lacaita [2]. Nowadays, these devices are gaining popularity in automotive industry (Light Detection and Ranging systems [3]) and time-of-flight imaging [4].

This paper introduces a new VerilogA model to assess the SPAD devices buildup and its statistics. For accurate behavior description, we developed a Verilog-A diode model including the underlying physics and calibrated on Technology Computer Aided-Design (TCAD) [5]. Simulations confronted with measurements show an impact on the pulse width distribution, which will be discussed. Additionally, we investigated the voltage swing on the SPAD sensing node. This phenomenon is due to carriers overflow and has a value larger than the excess bias as it has been also demonstrated in [6]. This voltage drop impacts the power consumption and experimental data attests its relevance. Consequently, we discuss the qualitative outputs which in turn will allow us to evaluate the validity of the approach.

II. MODEL DESCRIPTION

As a representative device, we consider a SPAD with a large collection volume [7]. The currents follow:

$$\begin{cases} \frac{dI_e}{dt} = [M_e \cdot I_e + M_h \cdot I_h - I_e] / \tau_e, \text{ for electrons} \\ \frac{dI_h}{dt} = [M_e \cdot I_e + M_h \cdot I_h - I_h] / \tau_h, \text{ for holes} \end{cases}$$

τ_i is the transit time and M_i the multiplication factor (i represents e for electrons and h for holes). When an electron-hole pair is created, a current $I_0 = \frac{q \cdot v_s}{w}$ (v_s is the carriers saturation velocity, q the elementary charge and w the effective multiplication region width) can initiate the avalanche. Hence, the total current $I_T = I_e + I_h$ that is a succession of ionizations $I_T = I_0(1 + M + M^2 + M^3 + \dots)$ can be written in a familiar way as: $I_T = \frac{I_0}{1-M}$ where $M = M_e + M_h$.

The coefficient $M_i = \alpha_i \cdot w_i$ depends on w_n and w_p [8], as well as on the electric field through: $\alpha_i = a_i \cdot \exp\left(\frac{-b_i}{F}\right)$ (a_i and b_i are constants determined Van Overstraeten-de Man model [9]). Therefore, an accurate estimation of the maximum electric field variation with the diode biasing is compulsory. Even though analytical models exist in certain simple cases (e.g. abrupt junction), we used an empirical method that reproduces well-calibrated TCAD predictions on more complex SPAD architectures. As can be seen in Fig.2, a change in the slope of the field versus voltage is observed at $\sim 17V$, which occurs when the device starts to deplete its collection volume. Fig.3 shows M as a function of voltage, with $w_n = 0.0736 \mu m$ and $w_p = 0.092 \mu m$, one obtains $M=1$ for a voltage $V_B = 17.1 V$ ($25^\circ C$) which is close to the experimental breakdown voltage value. Fig.4 (top) shows the SPAD current and voltage for various applied biasing as a function of time: the buildup takes typically $\sim 150ps$ at operational voltage ($\sim 23V$), and can be even larger for lower biasing which is in line with TCAD simulations (not shown). After the avalanche triggering, the rising current is lowered below the breakdown voltage and the diode rearmed. Fig.4 (bottom) shows the SPAD current-voltage characteristics as well as the output pulse width. As can be noticed, the current swing exceeds the excess bias by a factor ~ 1.4 , which has also been recently reproduced in Ref.[6].

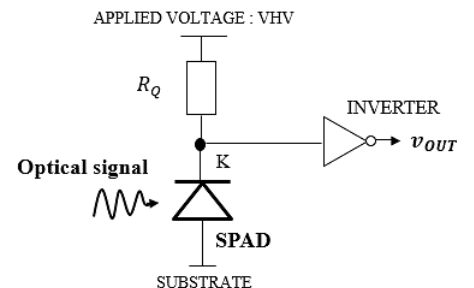


Fig. 1. SPAD diode connected to a high quench resistance $R_Q \sim 500 K\Omega$ from the cathode node K. After avalanche triggering, generated charges accumulate and give rise to a measurable current which will be lowered and the device brought to its quiescent state. The inverter component allowing a square output pulse, reflects the swing voltage and hence, the overall time constant of the circuit.

III. RESULTS

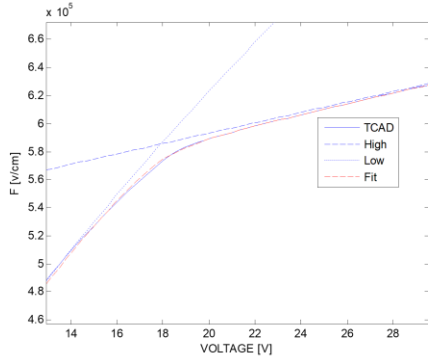


Fig. 2. The empirical model of the electric field (red dashed line) implemented in a Verilog-A code and expressed through a polynomial exploiting the high and low values of the field range. This model is calibrated on TCAD (solid).

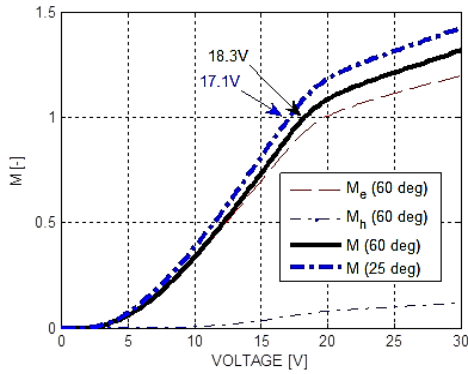


Fig. 3. The mean multiplication factor versus voltage, for two temperatures. $M = 1$ corresponds to $V_B = 17.1$ volts at 25°C ,

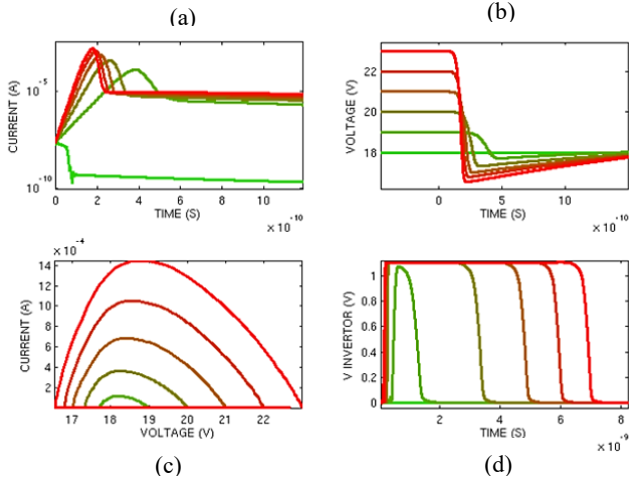


Fig.4: (a) The current buildup evolution with applied voltage (b) The voltage drop seen from the SPAD cathode exhibiting a swing. (c) SPAD I-V curve. (d) The output pulse v_{out} .

This swing voltage denoted V_{KMAX} , affects the charge per pulse C_{PP} (reflecting the power consumption) since $C_{PP} = C_K \cdot V_{KMAX}$ where C_K is the total capacitive charge in the cathode node (including parasitic). Fig.5. shows the evolution of C_{PP} with voltage V_{HV} : as V_{KMAX} increases with applied excess bias, C_{PP} increases as well. Similarly, the Pulse width distribution, which can be inferred from the statistics of the buildup dynamics itself, is accounted for using a statistical distribution of α as testified in Fig.6.

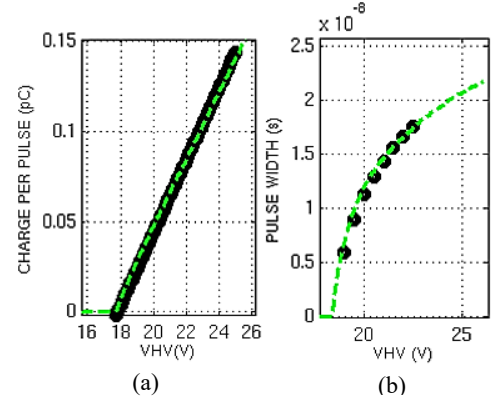


Fig. 5. (a) The charge per pulse C_{PP} and (b) the pulse width versus VHV: Verilog-A model (dashed) versus measurements (symbols).

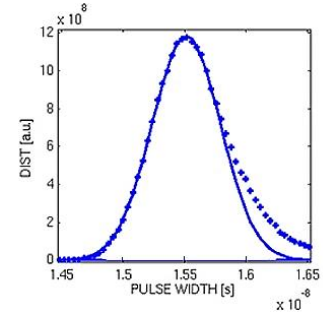


Fig. 6. Pulse width distribution. Solid curve refers to Verilog-A model, symbols to measurements.

IV. CONCLUSION

We have developed a physics-based Verilog-A model for SPADs accounting for the buildup of the avalanche and its statistics. The model compares favorably with more complex TCAD mixed-mode predictions, but also with experimental data. This SPAD model allows SPICE simulations of realistic circuits, including quenching and sensing transistors. It provides an accurate way to estimate the power consumption and the voltage swing on the sensing node.

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