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Article

# High Electron Confinement under High Electric Field in RF GaN-on-Silicon HEMTs

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**Abstract:** We report on AlN/GaN high electron mobility transistors grown on silicon substrate with highly optimized electron confinement under a high electric field. The fabricated short devices (sub-10-nm barrier thickness with a gate length of 120 nm) using gate-to-drain distances below 2  $\mu\text{m}$  deliver a unique breakdown field close to 100 V/ $\mu\text{m}$  while offering high frequency performance. The low leakage current well below 1  $\mu\text{A}/\text{mm}$  is achieved without using any gate dielectrics which typically degrade both the frequency performance and the device reliability. This achievement is mainly attributed to the optimization of material design and processing quality and paves the way for millimeter-wave devices operating at drain biases above 40 V, which would be only limited by the thermal dissipation.

**Keywords:** GaN-on-Si; high breakdown voltage; low leakage current

## 1. Introduction

As a consequence to the rapid development of Radio Frequency (RF) power electronics, wide bandgap materials have been introduced due to their potential in high output power density, high operation voltage and high input impedance. Gallium Nitride (GaN)-based RF power devices have made substantial progress in the last decade, which will enable new applications demanding higher output power and efficiency at higher frequencies, especially in the Ka band (26–40 GHz) and beyond, with the aim of replacing or complementing traveling wave tube amplifiers. Satellite and broadband wireless communications as well as advanced radars are only a few of the many applications that would greatly benefit from the increased reliability, reduced size and reduced noise of these solid state-based amplifiers. In order to achieve the goal of operating at mm-wave frequencies and beyond, new process technologies and device structures have to be developed. Indeed, the device dimensions, such as the gate-to-channel distance, the gate length or the gate-to-drain distance, need to be reduced in order to increase the frequency performance. However, GaN device downscaling is usually achieved at the expense of a much lower breakdown voltage as compared to devices with larger dimensions [1–4]. This is due to the significant increase of the leakage current in these highly scaled devices that can result from many parameters such as bulk defects, interface and surface traps, as well as a poor electron confinement due to the epilayer design or process-induced imperfections.

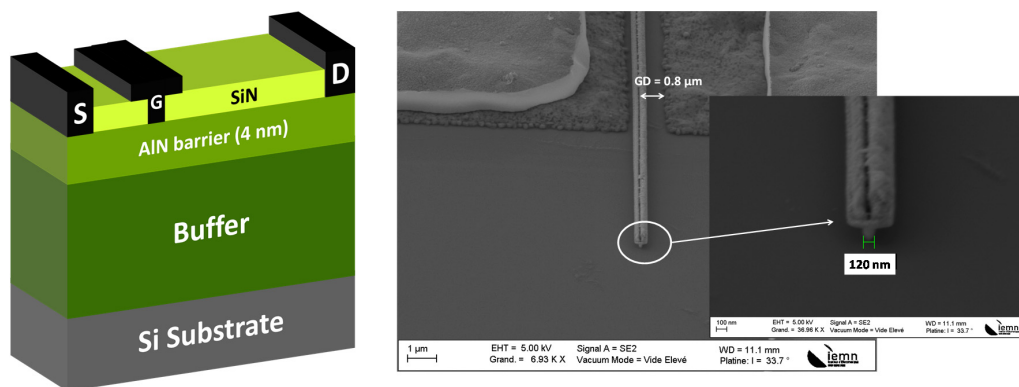
Recently, sub-10-nm ultrathin barrier GaN transistors have been proposed [5] in order to avoid gate recessing which is commonly used to reduce the gate-to-channel distance while shrinking the gate length but generally causes reliability issues due to plasma damage under the gate [6]. In this frame, we have demonstrated the possibility of preventing gate tunneling through highly scaled Aluminum Nitride (AlN) barrier thickness (below 5 nm) by showing an extremely low gate leakage current [7,8]. On top of the material quality, the *in situ* grown SiN cap layer has been a key feature for controlling

the surface parasitic leakage current and achieving high performance [9–11], namely by preventing the strain relaxation of the barrier layer.

In this paper, we report on the high breakdown voltage in highly scaled GaN transistors grown on a silicon substrate, showing that all the above-mentioned issues can be overcome in these emerging types of devices.

## 2. Experimental Section

The AlN/GaN heterostructures were grown by metal organic chemical vapor deposition (MOCVD) on a highly resistive 4 in Si (111) substrate. The High Electron Mobility Transistor (HEMT) structure consists of nucleation and transition layers, a 1.5- $\mu\text{m}$ -thick buffer layer including undoped graded AlGaN back barrier layers, followed by a 100 nm GaN channel and a 4.0 nm ultrathin AlN barrier layer as well as a 5.0-nm-thick *in situ* Si<sub>3</sub>N<sub>4</sub> cap layer (Figure 1). The *in situ* SiN layer is used both as early passivation as well as to prevent strain relaxation [12]. Room-temperature Hall measurements showed a high electron sheet concentration of  $1.5 \times 10^{13} \text{ cm}^{-2}$  with a mobility of  $1250 \text{ cm}^2/\text{Vs}$  in the heterostructure. Sheet resistance ( $R_{\text{sh}}$ ) measurements revealed a high uniformity over the 4 in wafers with  $R_{\text{sh}} = 310 \Omega/\delta \pm 3\%$  in the HEMT structure. A Ti/Al/Ni/Au metal stack annealed at  $875 \text{ }^\circ\text{C}$  has been used to form the ohmic contacts directly on top of the AlN barrier layer by etching the *in situ* Si<sub>3</sub>N<sub>4</sub> layer. Device isolation was achieved by nitrogen implantation. Ohmic contact resistance ( $R_{\text{c}}$ ) extracted from linear transmission line model (TLM) structures was  $0.35 \Omega \text{ mm}$ . Then, a 120 nm Ni/Au T-gate was defined by e-beam lithography (Figure 1). The SiN underneath the gate was fully removed by SF<sub>6</sub> plasma etching through the ebeam lithography. The gate-source was 0.3  $\mu\text{m}$  and gate-drain spacings were 0.8 and 1.8  $\mu\text{m}$ , respectively. The device width was 50  $\mu\text{m}$ .

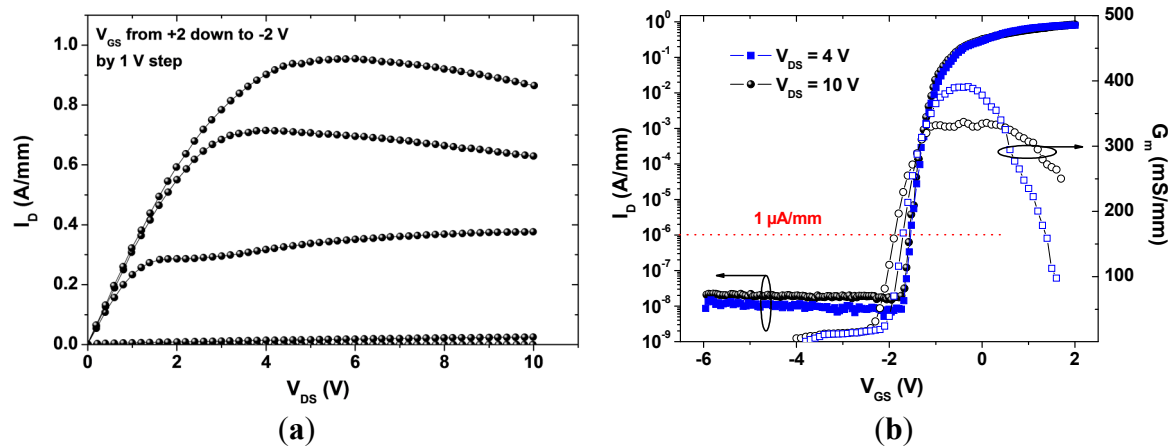


**Figure 1.** Cross-section of the fabricated AlN/GaN-on-Si HEMTs (left) and SEM images of the 120 nm gate technology (right).

## 3. Results and Discussion

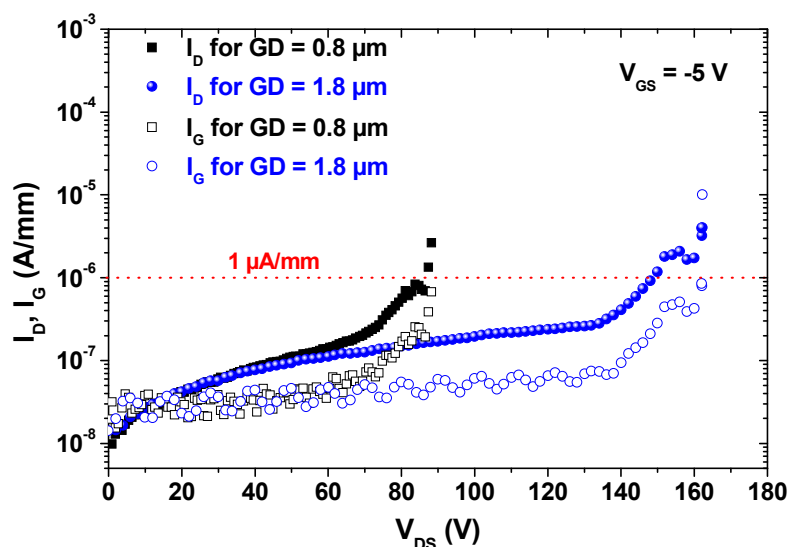
### 3.1. DC Characteristics

Typical output characteristics of  $2 \times 25 \mu\text{m}$  AlN/GaN-on-Si HEMT are shown in Figure 2a. The maximum DC current density at  $V_{\text{GS}} = +2 \text{ V}$  is about  $1 \text{ A/mm}$  with a peak extrinsic transconductance of  $390 \text{ mS/mm}$  at  $V_{\text{DS}} = 4 \text{ V}$ . In Figure 2b, the semi-log scale corresponding transfer characteristics at  $V_{\text{DS}} = 4$  and  $10 \text{ V}$  are plotted. It can be noticed that the transconductance decreases as a function of the drain bias due to the self-heating effect. In spite of a deep sub-micrometer gate length as well as short gate-drain distances and an ultrathin barrier layer, generating an extremely high electric field, a sub-threshold drain leakage current well below  $1 \mu\text{A/mm}$  is reproducibly observed (within the range of several tenths of  $\text{nA/mm}$ ) with no shift of the threshold voltage nor an increase of the leakage current as a function of  $V_{\text{DS}}$ . This clearly shows an optimum electron confinement combined with high material quality and controlled surface parasitic leakage current.



**Figure 2.** (a) DC output  $I_D$ - $V_{DS}$  characteristics of a  $2 \times 25 \mu\text{m}$  AlN/GaN-on-Si HEMT.  $V_{GS}$  swept from  $-2$  up to  $+2$  V in 1 V steps; (b) Transfer characteristics of the  $2 \times 25 \mu\text{m}$  AlN/GaN-on-Si HEMT at various  $V_{DS}$  (4 and 10 V) using  $L_G = 0.12 \mu\text{m}$ .

The benefit of this configuration, enabling us to prevent both short-channel effects and the electron injection into the buffer layers under high electric field, is absolutely obvious in the sub-threshold region and is consequently reflected in the three-terminal breakdown voltage of these devices. Figure 3 indeed shows the off-state characteristics at  $V_{GS} = -5$  V of devices with a gate-to-drain distance of 0.8 and  $1.8 \mu\text{m}$ . It can be noticed that an extremely low leakage current below  $100 \text{ nA/mm}$  is observed up to a high bias, yielding outstanding three-terminal breakdown voltages defined at  $1 \mu\text{A/mm}$  of about 80 V and 160 V, respectively. This translates to a breakdown field ranging from 90 to  $100 \text{ V}/\mu\text{m}$ , which is favorably comparable to typical reported values in the literature for such short RF devices, especially in terms of leakage current level [13].

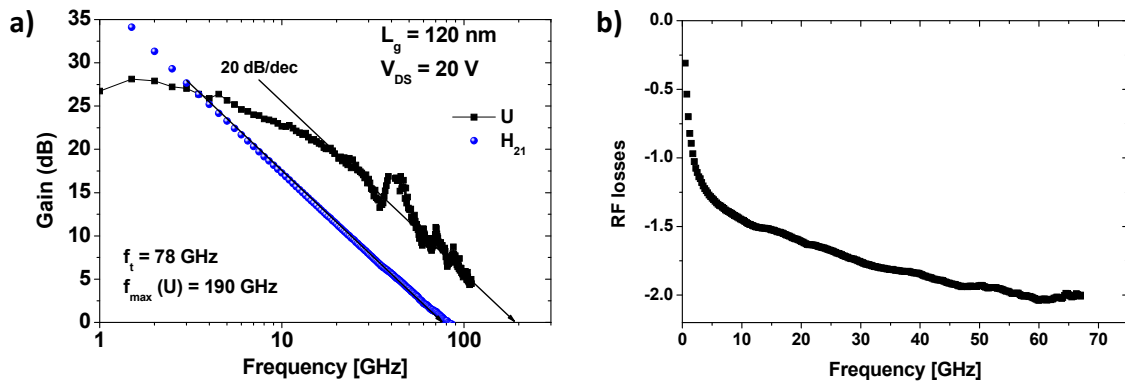


**Figure 3.** Off-state characteristics and gate leakage current at  $V_{GS} = -5$  V of the  $2 \times 25 \mu\text{m}$  AlN/GaN-on-Si HEMTs for gate-drain distances of  $0.8 \mu\text{m}$  (black squares) and  $1.8 \mu\text{m}$  (blue circles).

### 3.2. RF Characteristics

The S-parameters of a  $0.12 \times 50 \mu\text{m}^2$  AlN/GaN-on-Si HEMT were measured from 1 to 110 GHz. A current gain extrinsic cut-off frequency  $f_T = 78$  GHz and a maximum oscillation frequency  $f_{\text{max}} = 190$  GHz (shown in Figure 4a) have been extrapolated from the current gain  $H_{21}$  and the unilateral power gain (U) at  $V_{DS} = 20$  V. The strong reduction of the short-channel effects by using a

short gate-to-channel distance combined with high electron mobility in the two-dimensional electron gas (2DEG) explains the excellent power gain close to 200 GHz. It has to be pointed out that these frequency performances have been achieved despite non-optimized high RF losses of about 2 dB/mm as can be seen in Figure 4b. The RF losses extracted from transmission lines reflect a parasitic conduction at the buffer/Si substrate interface due to the intermixing between the GaN buffer layer and the Si substrate [14].



**Figure 4.** (a) RF performance of the  $0.12 \times 50 \mu\text{m}^2$  AlN/GaN HEMT on silicon substrate at  $V_{\text{DS}} = 20 \text{ V}$ ; (b) RF losses extracted from transmission lines up to 67 GHz.

Further reduction of the contact resistances as well as the RF losses should result in an increase of the extrinsic transconductance and a significant improvement of the frequency performance. The use of sub-100-nm gate lengths in the AlN/GaN DHFET should therefore pave the way for higher frequency operation of GaN-based devices grown on highly resistive Si substrate combined with high power (e.g., high current density and high voltage).

#### 4. Conclusions

We have developed high frequency AlN/GaN HEMTs grown on silicon substrate delivering an outstanding breakdown field close to  $100 \text{ V}/\mu\text{m}$  while using highly scaled dimensions such as sub-10-nm barrier thickness, 120 nm gate length and gate-to-drain distances below  $2 \mu\text{m}$ . This achievement is mainly attributed to the optimization of both material design and processing quality enabling high electron confinement under a high electric field. These data show that millimeter-wave GaN devices operating in the  $K_a$  band and above can operate at unique drain biases above 40 V.

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**Author Contributions:** All authors have participated to the design, the fabrication and the electrical characterization of the presented devices.

**Conflicts of Interest:** The authors declare no conflict of interest.

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