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Abstract

Nano-engineering III-Nitride semiconductors offers a route to further control the material and optoelectronic properties, enabling novel functionalities and applications. Although various lithography techniques are employed to nano-engineer these materials, the scalability and cost of the fabrication process can be an obstacle for manufacturing. In this paper, we report on the use of a fast, robust and flexible emerging patterning technique called Displacement Talbot lithography (DTL), to successfully nano-engineer III-Nitride materials. DTL, along with its combination with a lateral planar displacement (D^2TL), allow the fabrication of numerous periodic nano-patterns with a broad range of filling factors such as nanoholes, nanodots, nanorings and nanolines; all these features being achievable from one single mask. These nano-patterns have been used to create dielectric and metal masks in order to accomplish the following: the selective area growth of InGaN/GaN core-shell nanorods, the top-down plasma etching of III-nitride nanostructures, the top-down sublimation of GaN nanostructures, the hybrid top-down/bottom-up growth of AlN nanorods and GaN nanotubes, and the fabrication of nano-patterned sapphire substrates for AlN growth. Compared to their planar counterparts, these 3D nanostructures enable the reduction or filtering of defects and/or the enhancement of the light extraction, therefore improving the efficiency of the final device. These results, reproducible and achieved on a wafer scale via DTL, could potentially unlock the manufacturing of nano-engineered III-Nitride materials.

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Introduction

III-Nitride semiconductors have a vital place in today's optoelectronic and electronic devices.[1] In particular, III-Nitride-based light emitting diodes (LEDs) and laser diodes (LDs) have allowed efficiency breakthroughs in general illumination,[2,3] which was acknowledge by the Nobel Prize for physics in 2014 to the pioneer researchers Isamu Akasaki, Hiroshi Amano, and Shuji Nakamura "for the invention of efficient blue light-emitting diodes, which have enabled bright and energy-saving white light sources".[4,5]

One key parameter to establish the performance of a LED is the external quantum efficiency (EQE), which represents the ratio of the number of charge carriers injected into the device to the number of photons emitted by the LED. The EQE is often described as the product of the internal quantum efficiency (IQE) and light extraction efficiency (LEE). In III-Nitride materials, where layers are grown on a foreign substrate such as sapphire and silicon, owing to the limited availability and large cost of native substrates, the relatively high densities of defects generated during growth can dramatically impact the IQE. On the other side, the relatively large refractive index of III-Nitride materials seriously limits the amount of light that can be extracted from the LED as most of the photons will be trapped within the structure by total internal reflection. Nano-structuring these materials not only offers a route to improve the crystal quality and increase the light extraction but also facilitate the further control of the material and optoelectronic properties, enabling novel functionalities and applications.[6,7,8,9]

Compared to conventional 2D planar layers, 3D nanostructuring can, for example, reduce the dislocation density,[10,11] relieve the strain,[12] and improve the light extraction[6,8,9]. Nanostructuring can be implemented at various stages of the fabrication process of an LED device: at early stages prior to the growth of III-Nitride layers, after the growth of an LED structure, or even in between.

Patterning of substrates or III-Nitride buffer layers has been widely used in the early stages of the growth to reduce the formation of extended defects or block their propagation. Stripe micro-patterned sapphire and silicon substrates, with or without a dielectric mask, have been successfully exploited to achieve high-quality polar, semi-polar and non-polar layers with a process that is often referred to as 'selective area growth' (SAG) or 'epitaxial lateral overgrowth' (ELO) or a combination of both.[13,14] The geometrical shape of the pattern can also enhance light extraction by scattering or redirecting the light at the roughened substrate/III-nitride interface.[15] Finally, sub-micron-scale nano-patterned

sapphire substrates (nano-PSS) can enhance crystal quality and light extraction,[16] whilst simultaneously reducing the buffer layer thickness with the benefit of further lowering production costs.[17]

Further improvement to enhance light extraction can be accomplished once the LED structure has been grown, either by texturing the surface of a LED,[18,19] shaping the LED chip,[20] or encapsulating the LED chip.[21] Surface texturing helps to break up the guided modes confined within the LED structure by creating a surface that randomizes the propagation of light and increases the chance of photons escaping. Although surface roughening, either on the p-GaN top surface,[18] or at the n-side-up GaN surface,[19] has been successfully applied to increase light extraction, it provides poor control over the direction of the emitted light, resulting in Lambertian radiation patterns. Instead, the use of a periodic pattern provides a route to control the directionality.[22] In particular, photonic crystals, at the surface or embedded within the LEDs can increase the extraction efficiency, improve the directionality and enhance the IQE thanks to the Purcell effect.[23,24] The LED performance and directionality depends on the type, depth, filling factor and pitch of the photonic crystal along with the thickness of the epitaxial layers.[25]

III-Nitride nanorod LEDs are an alternative to reducing the dislocation density and improve light extraction in 2D layers.[7,8,9] III-Nitrides nanostructures can be fabricated via either a top-down or bottom-up approach.[7] While the top-down approach typically involves nanopatterning and subsequent etching,[11,26] the bottom-up growth of nanostructures doesn't necessarily require a post-patterning process.[7,27] However, to control their position, height and size uniformity, but also to reach fairly homogenous optical properties, much efforts have been focusing on the SAG on patterned substrates or templates.[7,28,29]

Therefore, whatever the approach employed to nano-engineer III-Nitride materials, it generally requires a lithography nanopatterning technique; a key point being the capability to create large scale nanopattern to reduce the fabrication cost. Displacement Talbot Lithography (DTL) is a fast and robust emerging patterning technique that can pattern rough and bowed wafers with features down to 100 nm on large areas, e.g. 4-inch wafers.[30] As a nanolithography process, it is much cheaper than electron beam lithography (EBL), and competes with nanoimprint lithography (NIL) and laser interference lithography (IL) as a wafer-scale process. However, it has advantages over both these latter processes, such as a low sensitivity to surface defects of substrate, no lifetime of master, a high system stability etc.., which is particularly interesting for the manufacturing of nano-engineered semiconductors, including III-Nitrides materials. Our recent reports also demonstrate the high flexibility of this technique, especially

when DTL exposures are combined with lateral displacements.[31] However, the few reports on DTL mainly focus on the resist patterning rather than its practical use to nano-engineer materials.[30,32,33]

In this paper, we report on the use of DTL to successfully nano-engineer III-Nitride materials. After introducing the overall fabrication process, the DTL and extended D^2TL nano-patterning capabilities will be presented with the fabrication of nanoholes, nanodots, nanorings and nanolines in positive and/or negative resist. The resist patterns are transferred into dielectric or metal masks by etching or lift-off for use as a mask for bottom-up growth, top-down etching or a combination of both. Examples of such nano-engineering applied to III-nitride materials will be given, such as: the bottom-up selective area growth of InGaN/GaN nanorods, the top down etching of various III-nitride materials such as GaN, AlN and AlGaN based nanoholes, GaN nanolines, GaN and AlN nanorod, axial InGaN/GaN nanotubes, the sublimation of GaN high aspect ratio nanoholes and nanorods, hybrid top-down/bottom-up AlN nanorod and GaN nanotubes. The fabrication of nano-patterned sapphire substrates and successful overgrowth and coalescence of an AlN layer will also be presented. Compared to the planar approach, these 3D nanostructures enable the reduction of defects and/or the enhancement of light extraction, therefore improving the efficiency of the final device.

Results and Discussion

III-nitrides are robust materials that can be difficult to plasma etch. For example, III-nitrides etch at much slower rates than conventional III-V compound semiconductors.[34] They generally require a chlorine-based plasma and in some case high temperatures.[34,35] Therefore photoresists are unsuitable, especially when thinner resists are required to improve the resolution; a necessary requirement for nano-engineering. Instead, the use of a hard mask, either dielectric or metallic is preferred; in particular, a metal mask will be essential when deep etching or high-aspect-ratio nanostructures are desired.[35,36] Moreover, the selective area growth of III-nitride nanostructures requires inert and robust material such as SiN_x and SiO_x.[7,9,10,28] The nanostructured dielectric layer enables diffusion and preferential deposition of species on the III-nitride window. Therefore, depending on the approach: top-down or bottom-up; the fabrication of both dielectric and metal masks are required to successfully nano-engineer III-nitrides. Figure 1 shows schematic outlining the

processing steps for these two mask types.-More specific details of each fabrication step can be found in the Methods section.

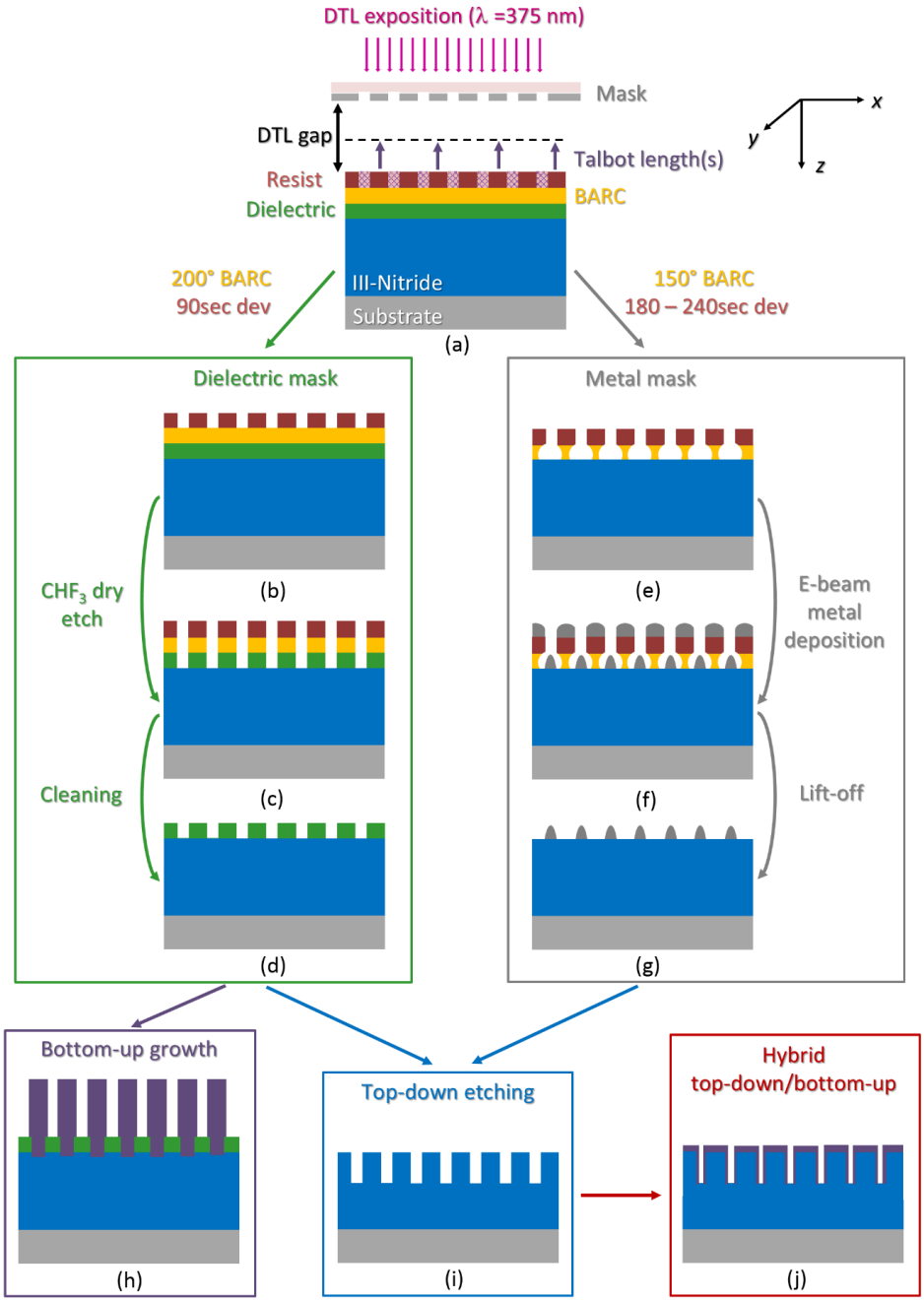

Fig. 1 Schematic of the III-Nitride nano-engineering process via DTL. a Coating of III-Nitride wafer or substrate and DTL exposure of the resist. **b, c, d** For a bottom anti-reflective coating (BARC) layer hard-baked at 200°C, the DTL pattern is first developed, then transferred via dry etching into the BARC and dielectric layer and cleaned. **e, f, g** For a BARC layer soft-baked at 150°C, the DTL pattern is developed and used to create an undercut profile prior to metal evaporation and lift-off. **h** Dielectric mask for bottom-up growth. **i** Dielectric and metal mask for top-down etching. **j** Combination of top-down etching and bottom-up growth.

Displacement Talbot Lithography

The Talbot effect, or self-imaging, is the effect of creating a periodic three-dimensional interference pattern when a periodic mask is illuminated by a coherent light.[37] The interference pattern reproduces itself when *z* is a multiple of the 'Talbot length'. By displacing the wafer along the *z* axis of illumination over integer spatial periods, the low depth of field of conventional Talbot lithography is overcome.[30] Fig. 2a-d displays the experimental pattern achieved for various doses in positive resist for a 1-µm-pitch mask with a hexagonal arrangement of 550 nm diameter holes (Fig. 2f). The nanohole openings increase in diameter from ~225 to ~425 nm with an increase in the exposure dose from 160 to 300 mJ/cm^2. For doses greater than 300 mJ/cm^2, a secondary pattern of holes appears (Fig. 2c) and merge to create a nanoring pattern having an inner diameter of ~ 520 nm and a wall width of ~ 150 nm (Fig. 2d). Alternatively, using a negative resist gives arrays of nanodots (Fig. 2e).

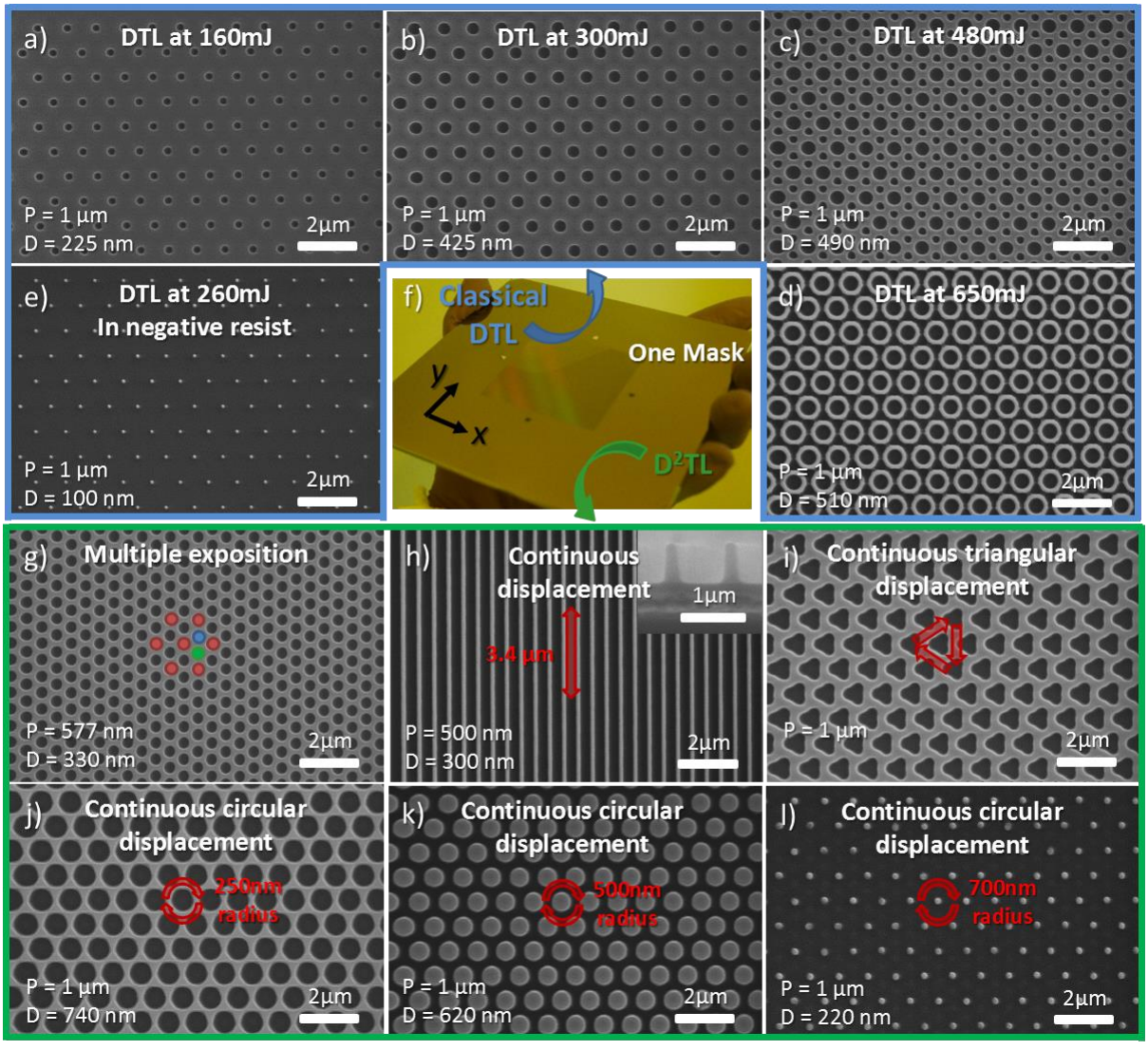

Fig. 2 DTL and D^{2}TL nano-patterns created from a 1 µm pitch 550 nm opening mask. Developed positive photoresist after classical DTL at **a** 160 mJ/cm^2. **b** 300 mJ/cm^2. **c** 480 mJ/cm^2 and **d** 650 mJ/cm^2. Developed negative photoresist after classical DTL at **e** 260 mJ/cm^2. **f** 1 µm pitch 550 nm opening amplitude mask used to produce all the patterns presented in Fig. 2. Developed positive photoresist after D^{2}TL for **g** three exposures, at *x=0*, *y=0*, *x=500nm*, *y=289nm* and *x=500nm*, *y=289nm*. **h** 3.4 µm continuous linear displacement. **i** triangular displacement **j** 250 nm radius circular displacement. **k** 500 nm radius circular displacement. **l** 750 nm radius circular displacement.

Introducing lateral displacements either during a single DTL exposure or between multiple exposures further extends the range of patterns achievable by a single mask. We call this extension 'Double Displacement Talbot lithography' (D^{2}TL).[31] Fig. 2g-l show examples of additional pattern in positive resist from the same mask. A reduction of the pitch from 1 µm to ~577 nm is obtained with multiple exposures. In Fig. 2g the red dots represent the first exposure and the blue and green dots correspond to a second and third exposure. Continuous displacements during a single exposure can form nanogratings (via displacement along the *x*- or *y*-axis (Fig. 2h)), triangular features (via a triangular displacement (Fig. 2i)), or a wider range of circular features than can't be obtained through simple DTL (via circular displacements of different radii (Fig. 2j-l)). The D^{2}TL patterns presented in Fig. 2g-i represent a small sample of the D^{2}TL capabilities, since the technique can also generate periodic arrays of complex features. Further details of D^{2}TL can be found in our recent report.[31]

Therefore, for one mask configuration, a broad variety of features and configurations has been created via DTL and D^{2}TL. Achieving the various patterns presented in Fig. 2 by NIL would requires up to 11 masters. This highlights the flexibility of the technique to pattern large areas with a much lower fabrication cost than that normally associated with nano-patterning.

Dielectric and metal mask for selective area growth and etching

Dielectric and metal masks can be produced from any of the previous nano-patterns presented in Fig. 2 or other configurations of the mask. Fig. 3a-d present various hexagonal array of periodic nanostructures transferred in a dielectric layer via inductively coupled plasma (ICP) etching. Array of nanoholes (Fig. 3a and b), nanorings (Fig. 3c) and nanodots (Fig. 3d) are successfully created on any dielectric layers, up to a thickness of 600-700 nm (Fig. 3d). Alternatively, metal masks are also fabricated via lift-off, as shown in Fig. 1e-g and 3e-i. Compared to dielectric material, metals generally possess a better selectivity to III-nitride, which will facilitate deeper etching into the layer.

As DTL is a non-contact patterning technique, the fabrication of dielectric mask and metal mask is independent of the surface roughness of the III-nitride layer and the wafer bow. In contrast, contact patterning such as NIL can induce serious damage (e.g. cracks or fractures) on bowed and fragile wafers such as GaN on silicon. Hence, DTL provides a robust and reproducible fabrication process for selective area growth and top down etching of III-nitrides at a wafer scale.

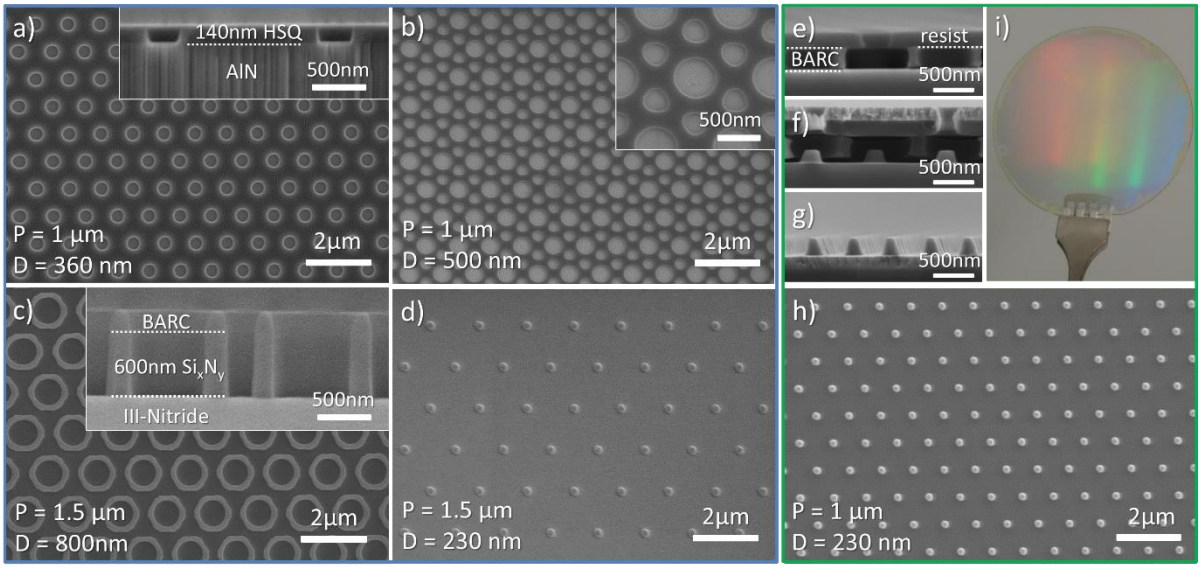

Fig. 3 Dielectric mask and metal mask. a 1 µm pitch nanoholes opening in 140 nm HSQ. **b** Double periodicity of nanoholes opening in 30 nm HSQ, with a primary pattern of 1 µm pitch. **c** 1.5 µm pitch rings in 600 nm SiN_x. **d** 1.5 µm pitch dots in 30 nm HSQ. **e-f** SEM cross-section image after exposure and development of the positive resist, after metal deposition and after lift-off. **h** SEM plan-view image of a hexagonal array of metal dots after lift-off. **i** Photograph of 2-inch GaN template with metal dot array on its surface.

Bottom-up selective area growth

Nanohole openings in a relatively thin dielectric layer is the most common configuration to perform selective area growth of nanostructures such as nanopyramids or nanorods.[7,9,10,28] Fig. 4 displays InGaN/GaN core-shell structures grown by MOVPE on patterned Ga-polar GaN on sapphire template. The initial nano-patterning performed via DTL allowed the successful control of the position, diameter and density of the nanorods while optimized MOVPE growth conditions enabled the vertical growth of nanostructures and additional control on the diameter.[10,38]

The selective area growth of GaN nanorods and InGaN/GaN-based core-shell structures have been widely investigated over the past decades, with some promising results and

properties such as: a low turn on voltage, low series resistance, short carrier lifetime,[39] the potential to achieve monolithic RGB emission[40] and a control over the far-field emission pattern,[41] which is particularly attractive for specific applications such as solid state lighting, visible light communication or µ-LEDs. However, to commercialize these structures, the growth and device fabrication must be performed on a large wafer scale. Many reports employ EBL to create a dielectric mask,[7,9,10,38,40] which, despite the high resolution, often limit the area over which nanostructures can be grown. Alternatively, NIL and IL provide wafer scale nano-patterning with reasonably high resolution.[7,9,28] However, NIL is sensitive to surface defects and the lifetime of master, whilst IL requires a high system stability. Here we demonstrate that DTL can be successfully used for such purpose which could help to further reduce the cost of InGaN/GaN core-shell LEDs enabling manufacturing.

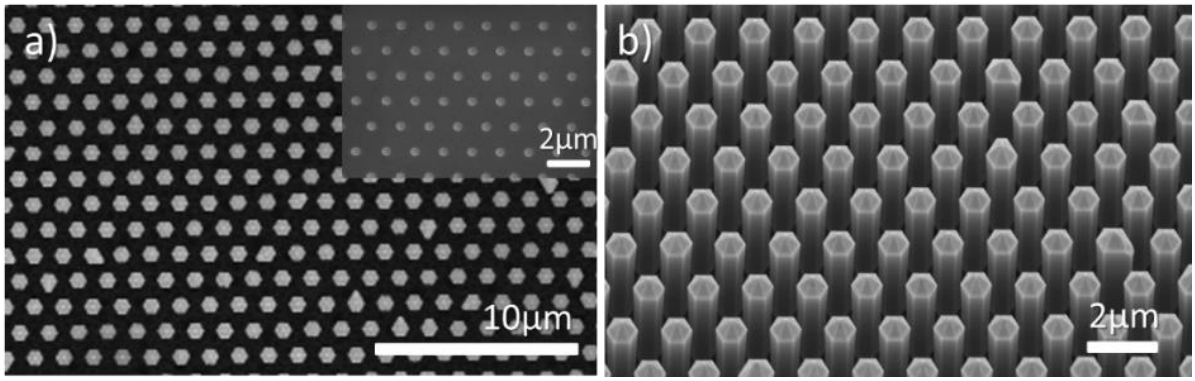

Fig. 4 InGaN/GaN core-shell nanorods. a SEM plan-view image and **b** tilted image of 4.2 µm height 800 nm diameter core-shell structure with three InGaN QWs. The inset in **a** displays the initial dielectric mask composed of 350 nm hole openings in 30 nm HSQ with a 1.5 µm pitch.

Top-down synthesis of nanostructures

III-Nitride dry-etching

From the various DTL nano-patterns presented in Fig. 2, a broad range of III-Nitride nanostructures have been obtained via chlorine-based ICP dry etching. Depending on the application targeted, the thickness, nature and configuration of the mask were optimized to achieve a wide range of periods and aspect ratios. Fig. 5a-c presents arrays of GaN nanoholes, nanolines and nanorods. Fig. 5d-f similarly shows arrays of AlN nanoholes, nanotubes and nanorods. Finally, Fig. 5g-i shows various nano-patterns transferred in III-nitride LED structures to form axial InGaN/GaN nanotubes, p-GaN/AlGaN nanopillars and AlGaN nanoholes with two periodic sizes. Nanostructures with a relatively high aspect ratio can be

achieved, such as those in Fig 5.c, f and g with values of 21.4, 7.8 and 2.2, respectively. Note that a difference in etch rate is commonly observed between III-Nitride materials and explained by the higher binding energy of AlN compared to GaN and InN,[42] which will induce a decrease of the etch rate with the increase in Al content.

A common feature of the nanostructures presented in Fig. 5a-g is the presence of a fairly straight sidewall profile regardless of the nature of the mask or of the III-Nitride material. The sidewall profile of the nanostructures can be tuned by changing the plasma properties such as the pressure, the temperature, the RF power and ICP power. More details on the etching recipes and the impact of the plasma properties can be found in the Method section and previous publications.[35,36,43] It is also possible to further tune the dimensions and profile of the nanostructures by further wet-etching the nanostructure in a KOH-based solution. Fig. 5c shows GaN nanorods before and after wet etching. As already reported in the literature, KOH-based wet etching helps to remove plasma etch damage, improve the sidewall profile and control the geometry.[11,44]

These results also show the robustness of the DTL based fabrication process to high surface roughness such as pits (Fig. 5a and e) or terraces (Fig. 5h). The AlN nanotubes in Fig. 5e were fabricated despite the high roughness of the initial template, as indicated by the tops of the tubes after dry etching and the removal of the etch mask.

There are multiple purposes for creating nanostructures having various dimensions, geometry and filling factor. Firstly, light extraction can be improved by nano-texturing the surface of LEDs with shallow nanostructures. The nano-textured AlGaN based UVB LED surfaces presented in Fig. 5h-l will not only scatter the light and improve light extraction but also reduce the absorption within the thin top p-GaN layer that is commonly needed in UVB LEDs to get a low resistance contact. Secondly, light extraction can also be improved and directionality controlled by creating photonic crystals from dense arrays of nanoholes and nanopillars, even to the extent of achieving lasing.[23,24,45] Indeed, the use of multiple exposures via D^2TL (Fig. 2g) is a promising approach to attain the small pitches required for photonic crystals at short wavelengths on a wafer scale. Thirdly, III-nitride photonic circuits can be created by combining grating couplers comprising dense arrays of nanolines (see inset in Fig. 5b) with other nano/microstructures.[46,47] Fourthly, the emission across the visible or the UV spectrum can be tuned by engineering the strain in an embedded active region through control of the diameter of nanorods.[48] Finally, nanolaser cavities, where the light is confined either between the top and bottom facet or within the circumference of the

structure, can be constructed from high-aspect-ratio nanostructures such as the rods and tubes (Fig. 5c, f and g).[43,44]

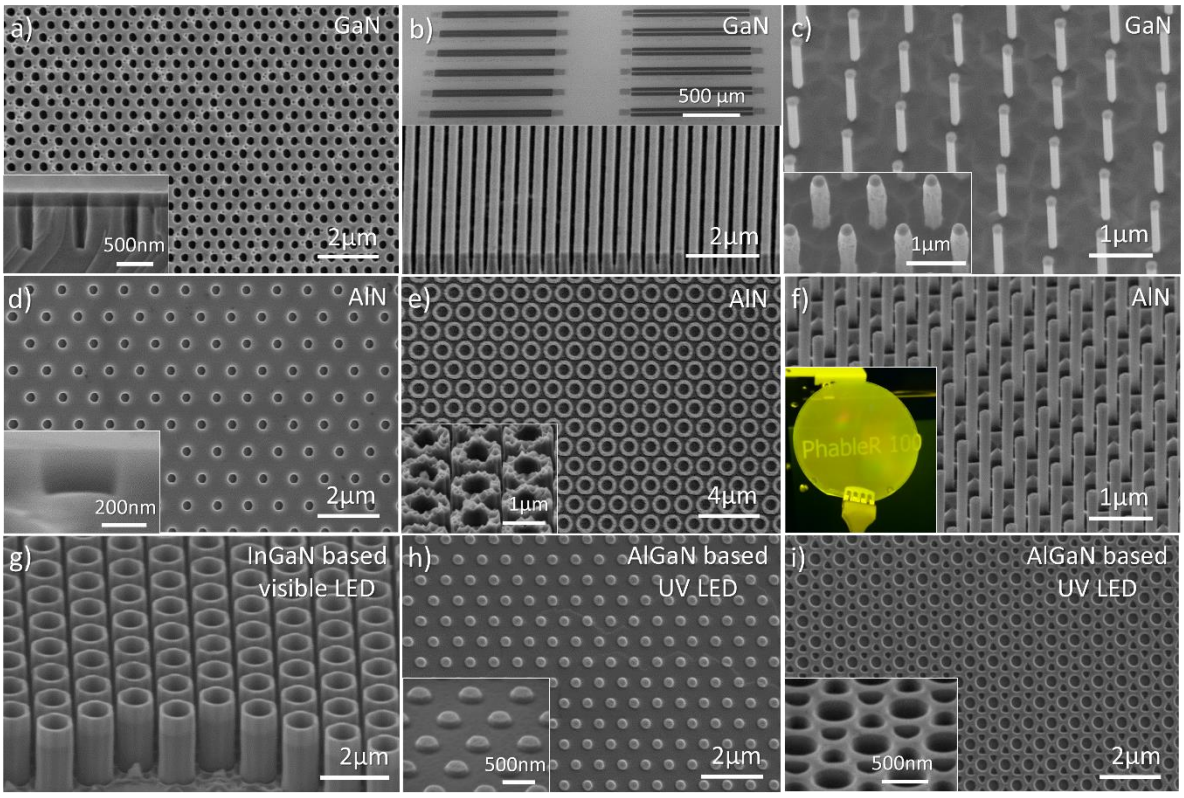

Fig. 5 III-Nitride top-down etched nanostructures a Plan-view SEM image of ~600 nm depth GaN nanoholes. **b** 45° tilt SEM image of ~800 nm depth GaN nanoline and related GaN grating couplers in inset. **c** 10° tilted SEM image of ~3 µm height GaN nanorods after ICP dry etch (inset) and KOH-based wet etch at 60°C. **d** Plan-view SEM image of ~150 nm depth AlN nanoholes. **e** Plan-view SEM image of ~800 nm height AlN nanotubes. **f** 45° tilt SEM image of ~1.8 µm height AlN nanorods after ICP dry etch and AZ400K wet etch at RT and associated photograph of 2-inch AlN nanorod template in inset. **g** 45° tilt SEM image of ~2.4 µm height axial InGaN/GaN nanotube. **h** 45° tilt SEM image of ~100-nm-depth p-GaN/AlGaN nanopillar at the surface of an AlGaN based UV LED. **i** Plan-view SEM image of double periodicity of nanoholes at the surface of an AlGaN based UV LED with a ~250 nm depth.

GaN selective area sublimation

Sublimation has been recently proposed as a simple top-down route to form nanostructures such as nanorods, nanopyramids, InGaN quantum discs or nanoporous material from GaN-based material without introducing the damage that occurs in dry etching.[49,50] By protecting the GaN surface with a thermally resistant dielectric layer and then annealing the sample under vacuum and sufficiently high temperatures, selective area sublimation of GaN can be carried out through the apertures of the mask. Fig. 6 displays top-down selective area sublimation

experiments performed on a Ga-polar GaN on sapphire template with various nano-patterns etched into a 50 nm thick SiN_x mask. After 3 hours of sublimation within a UHV chamber and SiN_x removal in BOE, 1 µm height nanoholes are obtained (Fig. 6a and b) while 4 µm height nanorods are attained after 10 hours. As expected, the initial DTL pattern provides highly-organised nanostructures at a wafer scale (see inset in Fig. 6a). Both the nanoholes and the nanorods show fairly straight sidewall profiles and a vertical to horizontal sublimation rate of 2 to 3% due to the high thermal stability of non-polar GaN planes in vacuum.

By comparing top-down approaches, selective area sublimation provides vertical sidewalls, no etching damage, and a perfect mask selectivity, enabling the formation of high aspect ratio nanoholes or nanorods with a very thin dielectric mask. However, sublimation is sensitive to structural defects,[51] occurs not only vertically but also laterally, and is only suitable for GaN and InGaN materials; not AlGaN with more than 10% Al.[52] Therefore, although promising for photonic applications and the nanostructuring of GaN materials,[50,52,53] ICP dry etching provides more flexibility in terms of what materials can be patterned and the nanostructure profile.

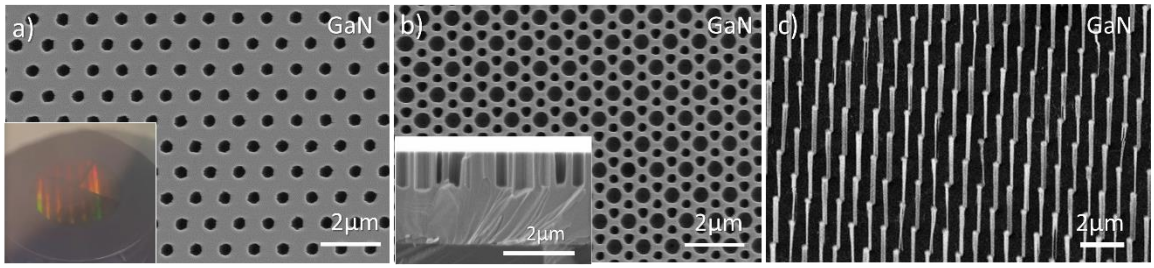

Fig. 6 GaN selective area sublimation a SEM plan-view image of 1 µm height holes in GaN. **b** SEM plan-view and cross-section (inset) images of double periodicity holes in GaN of ~1 µm height **c** SEM tilted image of 4 µm height 100-400 nm diameter GaN nanorods. Inset in Figure 6.a shows a 2-inch GaN wafer during the sublimation process with on configuration of nanohole per quarter.

Combined top-down/bottom-up processing

The hybrid top-down/bottom-up approach combines the fabrication of highly-uniform and organized nanostructures, such as those presented in Figs. 5 and 6, with an additional regrowth step, similar to the selective area growth in Fig. 4. As a function of the growth conditions and the initial configuration and dimensions of the nanostructures, the regrowth of III-nitride material can lead either to the formation of a planar 2D layer or to the formation of 3D nanostructures with well-defined crystallographic facets. The latter is presented in Fig. 7 where images are shown of AlN regrowth performed on AlN etched nanorods (Fig.

7a), and of GaN regrowth on GaN etched nanotubes for two growth conditions (Fig. 7b and c). For some growth conditions,[11,36,54,55] coalescence is inhibited, and straight and smooth non-polar sidewall facets are formed for both GaN and AlN (Fig. 7a and b). For different growth conditions, coalescence is induced, for example to create dense array of reverse pyramids from the tops of GaN nanotubes (Fig. 7c).

As the growth of AlN nanorods by selective area growth has yet to be achieved due to the high sticking coefficient and the low diffusion length of Al atoms,[56] the combination of top-down etching and bottom-up MOVPE growth represents a reliable approach to fabricate uniform and homogenous arrays of AlN nanorods, as shown in Fig. 7a. These are of particular interest for the subsequent growth of deep-UV core-shell structures.[57] The ability to fabricate further geometries, such as nanotubes (Fig. 7b) or reverse nanopyramids (Fig. 7c) opens the possibility to grow active regions such as quantum wells on specific facets or quantum dots in preferential locations. Therefore, compared to conventional MOVPE selective area growth alone, the combination of top-down etching and bottom-up regrowth enables a broader range of nano-light-emitting architectures to be explored.

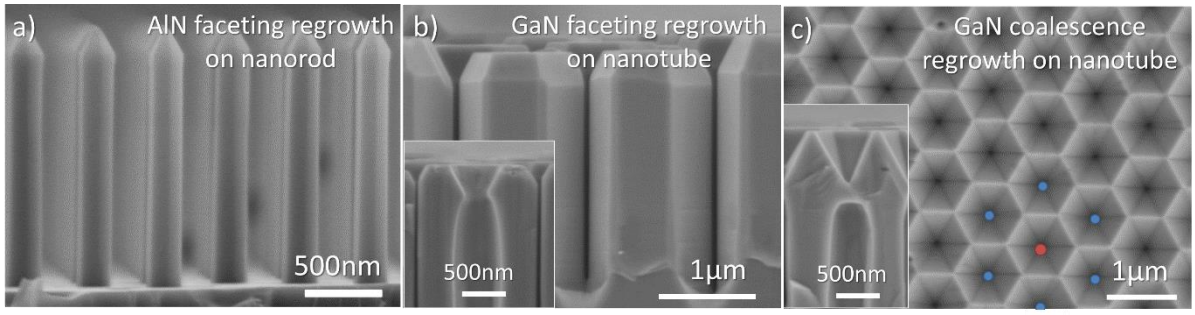

Fig. 7 III-Nitride hybrid top-down/bottom-up nanostructures a SEM cross-section image of AlN nanorods after AlN MOVPE regrowth. **b** SEM cross-section image of GaN nanotubes after GaN MOVPE regrowth. **c** SEM plan-view image of an array of GaN reverse nanopyramids after GaN MOVPE regrowth. Both inset SEM images in b and c show a cleaved cross-section in the middle of the tube.

III-nitride growth can also be performed on nanostructured foreign substrates following the same fabrication process employed for III-nitrides. Nano-patterned sapphire substrates (nPSS) have been obtained on 2-inch wafers either with an array of nanoholes (Fig. 8a) or nanopillars (Fig. 8b). These features are uniform across the 2-inch wafer (Fig. 8.b), with a flat top *c*-plane preserved after fabrication (inset in Fig. 8a and b). Fig. 8c shows the growth and successful

coalescence of AlN layers carried out on the nanopillar-nPSS wafer, following growth conditions previously reported.[17]

Compared to wet etching of sapphire, which is facet dependent and thus limited in depth for small features, the combination of a thick dielectric and/or metal mask with chlorine-based top-down dry etching enable to tune both, the etch depth and sidewall profile. While NIL process become less trivial for thick resist, the use of DTL allows to pattern thick resist at the nanoscale and thus, to create thick SiN_x mask.

By improving the crystal quality of the layers and the light extraction of the final device,[16,17] the nanostructuring of sapphire substrate is of particular interest to boost the efficiency of DUV LEDs.[58] The use of DTL/D^2TL constitutes a reliable and cost effective option to create nPSS with a broad range of configurations.

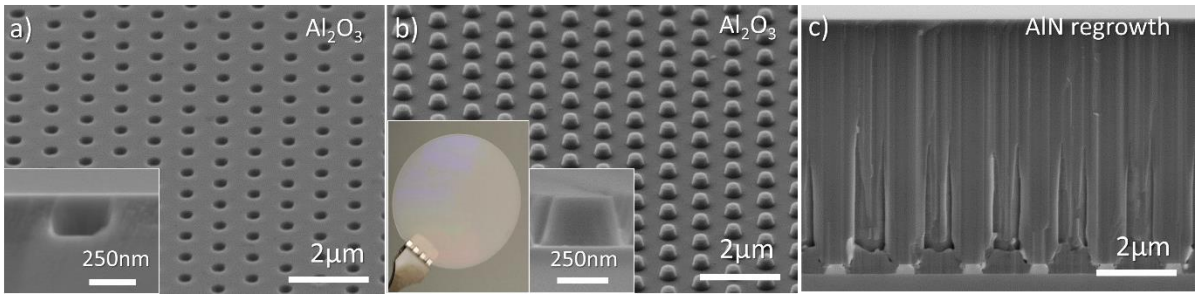

Fig. 8 AlN regrowth on nano patterned sapphire substrate a 45° tilt SEM image of nanoholes in sapphire substrate with in inset a high magnification cross-section image of the Al_2O_3 nanohole. **b** 45° tilt SEM image of nanopillars in sapphire substrate with in inset a photograph of a 2inch nPSS and a high magnification cross-section image of the Al_2O_3 nanopillars. **c** SEM cross-section image of 6 µm thick AlN layer grown on of nanopillars sapphire substrate.

Conclusions

This work shows the high potential of Displacement Talbot Lithography for large scale nano-engineering of III-nitride materials owning to a fast, robust, scalable and highly flexible process. A broad variety of features and configurations has been obtained in positive and negative resist and successfully employed, first, to create dielectric and metal mask and, second, to nano-engineer various III-nitride layers via selective area growth, selective area sublimation, top-down etching and hybrid top-down/bottom-up growth. The use of nanostructures or nano-textured surfaces is the key to achieve higher efficiency of III-Nitride LEDs mainly thanks to defect reduction and light extraction enhancement.

Despite the broad range of configurations and feature sizes already demonstrated in this paper, the capabilities of DTL in terms of resolution can be extended with a shorter

wavelength illumination source. Recently, Eulitha demonstrated wafer-scale sub-wavelength features with a 266 nm source.[33] Therefore, by combining the D^{2}TL approach with a shorter illumination wavelength, low pitches <250 nm could be achieved on a wafer scale, which would be of major interest to create photonic crystals in III-Nitride-based UV LEDs and further improve their efficiency.[58,59]

Materials and methods

Displacement Talbot Lithography Patterning.

All DTL patterning has been performed on 2inch wafers (Figure 1.a). A stack of two layer were spin-coated at 3000 rpm to obtain a ~ 270 nm bottom antireflective coating (BARC) (Wide 30W – Brewer Science) layer thickness, followed by either a layer of high-contrast positive resist (Dow® Ultra-i 123 diluted with Dow® EC11 solvent) or a layer of negative resist (AZ® 15 NXT diluted with AZ® Edge Bead Remover (EBR) solvent with a 7:12 ratio by weight). The baking temperature is a critical parameter for the BARC processing as they determine the rate at which the BARC develops. A bake at 150°C enables a wet-developable process and thus to create an undercut profile (Fig. 1e and 3e). A bake at 200°C fully cures the BARC, making it insoluble in a developer (Fig. 1b). DTL (PhableR 100, Eulitha) was then used to expose the resist with a coherent 375 nm light source with an energy density of 1 mW.cm^{-2} (Fig. 1a). Various masks have been employed: two hexagonal amplitude masks, one with a 1.5 μm pitch with 800 nm diameter circular opening, and another with a 1 μm pitch with 550 nm opening, and two phase mask, one with a 500 nm pitch with 300 nm diameter circular opening, and another with 1 μm pitch with lines spaced by 800 nm with a 62% filling factor. The Talbot length associated with those masks is 8.81 μm, 3.80 μm, 750nm and 3.21 μm, respectively. Details of the calculation can be found in others publications.[30] The gap between the mask and the wafer was set to 150 μm. A Gaussian velocity integration was applied and 8 Talbot lengths travel distance has been chosen to assure a homogenous integration on several Talbot motifs. After a certain exposure time (which defines the exposure dose), the sample was baked for 1 min 30 sec at 120°C on a hot plate. The wafer with a positive resist was developed in MF-CD-26 for 90 to 240 sec (depending on the mask fabrication), the one with a negative resist in AZ 726 for 30 sec. Finally, the wafer was rinsed with deionized water and dried with nitrogen.

Dielectric mask fabrication.

Materials such as hydrogen silsesquioxane (HSQ) and silicon nitride (SiN_x) were used as a dielectric mask. Prior to DTL patterning, HSQ was spin-coated on 2inch wafers at 3000 rpm and baked from 150°C to 450°C in 100°C increments or SiN_x was deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD). The pattern created in the resist by DTL/D^2TL (Fig. 1b and Fig. 2a-l) were transferred into the dielectric material (Fig. 1c and Fig. 3a-d) via an inductively coupled plasma (ICP) dry etch system (Oxford Instruments System 100 Cobra). The experiments were performed with a CHF_3 chemistry of 25 sccm, a temperature set to 20 °C, a pressure of 8 mTorr, 50 RF power and 300 W ICP source power, resulting in a etch rate of ~50 nm/min. The etching time was adjusted as a function of the thickness of the dielectric mask. The resulting transferred pattern was then cleaned in a piranha solution (3:1) and oxygen plasma (Fig. 1d).

Metal mask fabrication.

The undercut profile created in the BARC (cured at 150°C) after exposure and development (Fig. 1e and Fig. 2e) was employed as a lift-off layer. 200 nm Ni layers were deposited via e-beam evaporation to produce metal masks in the circular opening at the surface of the wafer (Fig. 1f and Fig. 2f). Subsequent lift-off was achieved by soaking the wafer in MF-CD-26 developer. Finally, wafers were cleaned in a 2 min reactive-ion etching (RIE) oxygen plasma to remove any BARC residue (Fig. 1g and Fig. 2g-i).

Bottom-up growth of GaN nanorods.

For Blandine.[10,38]

Top-down etching of III-nitride materials.

ICP dry etch system was used to create nanostructures in various materials including GaN, AlN, III-Nitride LEDs structures and sapphire substrates. In the case of III-nitrides, the experiments were performed with a Cl_2/Ar chemistry of 50/10 sccm, a temperature of 150 °C, a pressure set between 9 to 15 mTorr, a RF power set between 80 and 120 W and 800 W ICP source power. More details can be found in previous publications.[11,35,36,43] For sapphire substrate, the experiments were performed with a Cl_2/BCl_3/Ar chemistry of 5/50/5 sccm, a temperature of 5 °C, a pressure of 8 mTorr, 100 W RF power and 600 W ICP source power. Finally, the masks were etched away in aqua-regia solution (HCl:HNO3, 3:1) for metal masks, and in BOE 5:1 for dielectric masks.

Sublimation of III-nitride materials.

For Ben.[49,50]

Hybrid top-down/bottom-up.

The III-nitride bottom-up regrowth was carried out in a 1 x 2" horizontal Aixtron MOVPE reactor. The growth conditions for AlN faceting on nanorod were the following: a temperature of 1100 °C, a pressure of 20 mbar, 10 sccm in TMAl flow rate, 4000 sccm in NH_3 flow rate, and H_2 as the carrier gas. GaN regrowth was performed at a temperature of 920 °C (Fig. 7b) or 820 °C (Fig. 7c), a pressure of 100 mbar, 8 sccm in TMGa flow rate, 2800 sccm in NH_3 flow rate, and H_2 as the carrier gas. More details can be found in previous publications.[11,36,54,55]

AlN overgrowth on nanopillar-nPSS was done in an AIX2400G3HT MOVPE planetary reactor with a capability of 11 x 2-inch wafers with standard TMAl and NH_3 precursors. Pressure was fixed at 50 mbar and H_2 served as carrier gas. A 50 nm thick nucleation layer was deposited at 980 °C with a V/III ratio of 4000. After nucleation, the temperature was increased to 1380 °C with a V/III ratio of 30, followed by a decrease to 1180 °C with the same V/III ratio.

SEM imaging.

Scanning electron microscopy (SEM) was used to monitor the fabrication process and investigate the morphology and dimensions of the structures, using a Hitachi S-4300 SEM.

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Conflicts of Interest

The authors declare that they have no conflict of interest

Author contributions

P.-M.C. conceived the experimental work, supervised by P.A.S. P.-M.C. carried out the DTL patterning, dielectric and metal mask fabrication, ICP dry etching, MOVPE regrowth experiment on etched nanostructures, and related SEM characterization. P.C. carried out the D^2TL patterning. B.D. and S.V. performed the sublimation experiments by MBE and related SEM characteization. B.A. grew the InGaN/GaN core-shell structure via bottom-up MOVPE. S.W. and S.H. overgrew AlN layers on nPSS. J.E. grew the UV LED structure. R.A carried out the fabrication of AlN nanotubes. All of the authors contributed in analysing and writing the results

Supplementary Materials

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