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Maxime Legallais, Thi Thu Thuy Nguyen, Thibault Cazimajou, Mireille Mouis, Tabassom Arjmand, et al.. Role played by the nanowire/nanowire junctions in the electrical properties of semiconductor percolating silicon nanowire networks. *Journal of Applied Physics*, 2020, 128 (20), pp.204501. 10.1063/5.0023322 . hal-03024377

HAL Id: hal-03024377

<https://hal.science/hal-03024377>

Submitted on 25 Nov 2020

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Role played by the nanowire/nanowire junctions in the electrical properties of semiconductor percolating silicon nanowire networks.

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Abstract

In this paper, we highlight the key role played by Si nanowire/nanowire junctions in the electrical performance of field-effect transistors (FETs) based on percolating Si nanowire (SiNW) networks, also called nanonets. Using our original technological process to fabricate simultaneously numerous silicon nanonet-based transistors with variable geometry, we thoroughly investigated in this paper their electrical properties for various channel lengths, from 5 to 100 μ m. Particularly, we evidenced a clear transition in the FET performance, when NW/NW junctions are involved in the conduction path. On one hand, for channel length shorter than that of nanowires (NWs), the devices are called Multiple-Parallel-Channel FETs (MPC-FETs) as NWs directly bridge the channel, and they exhibit poor electrical performance in terms of OFF current, ON-to-OFF ratio and subthreshold slope. On the other hand, for channel length longer than that of nanowires (NWs), the devices are called Nanonet-FETs (NN-FETs) as the current flows through percolating paths made of NWs and NW/NW junctions and the performance are considerably enhanced. By combining our structural knowledge of the material with experimental observations of electrical properties and modelling results, by relying on the percolation theory, the model for electrical transport in polycrystalline silicon and the principle of potential barrier lowering by field effect, we propose the Junction Driven Percolation mechanism. It explains the role played by the nanowire/nanowire junctions in the electrical properties of semiconductor percolating nanowire network and how they drastically enhanced the electrical properties of nanowire-based field-effect transistors despite the disorder introduced by the increasing number of nanowires. As a consequence, by controlling properly the junction interfaces and device geometry for a given NW density, thanks to NW/NW junctions, the NN-based devices are a valuable and promising alternative to improve the electrical performances of NW-based devices for future developments.

Keywords

Polycrystalline silicon nanowire network – junctions – grain boundary – potential energy barrier – field effect transistor – electrical transport – nanonets

I. Introduction

Field effect transistors (FETs) based on a randomly oriented nanostructure networks, called nanonets^{1,2}, have been proposed as an interesting alternative to single nanostructure-based devices. In addition to benefiting from the semiconducting properties of each nanostructure, this network configuration gives additional features such as facility of integration³, mechanical flexibility^{4,5}, optical transparency^{5,6}, fault tolerance and high reproducibility^{1,7}. Moreover, network density and device geometry (length and width) of FETs allow to tune the electrical performances which offers another considerable degree of freedom compared to single nanostructure-based devices^{8,9}. Reported nanonet-based field effect transistors using various nanostructures such as carbon nanotubes^{8,9} (CNTs), zinc oxide nanowires¹⁰⁻¹³ (ZnO NWs) or aligned tin oxide nanowires¹⁴ (SnO₂ NWs) have shown interesting performances in terms of ON current, ON-to-OFF ratio, subthreshold slope and hysteresis. In these particular transistors, current flows through conducting paths that involve nanostructures as well as nanostructure-to-nanostructure junctions.

The percolation theory^{15,16} has been extensively employed to describe the behavior of these nanowire networks. In the literature, the junctions were either assumed non-resistive and then only nanowires were considered^{17,18}; or they were assumed to play an important role in the conduction of the network¹⁷⁻²². Recently, Benda et al²³ proposed a simpler expression to model the effective network resistance using network geometry as well as physical parameters (wire resistivity, wire/wire junctions and metallic electrode/wire junctions). In addition, Vodolazskaya et al²⁴ have also taken into account the effect of tunneling through junctions where the nanowires were made of conductive core and soft shell. To model CNT-based network field effect transistor, Alam and coworkers²⁵⁻²⁷ have introduced a charge-transfer coefficient at the junctions between the tubes. Since then, this charge transfer coefficient was widely used in the literature to explain a large quantity of data arising from CNT-nanonet FET, as reviewed by Rouhi et al⁹. However, although this model is satisfactory at the network scale, some physical phenomena are not taken into account such as CNT surface states, gating effects in metallic CNTs or electrical behavior of tube-to-tube junction resistance. In addition, the Ohmic or Schottky nature of CNT-to-CNT contacts²⁸ is also ignored. However, knowing that a CNT network is composed of four different electrical components –semiconducting and metallic nanotubes, Ohmic and Schottky contacts– it is undoubtedly difficult to explain and model correctly the electrical behavior of this kind of nanonet FETs. Therefore, studying the electrical properties of FETs based on other semiconducting nanostructures may bring new insights in the understanding of these network-based transistors.

In our group, we have developed all the technological bricks necessary for the development of transistors based on silicon nanowire networks whose channel length can vary from a few micrometers to millimeters and whose properties are reproducible and stable even in the air^{3,5,29}. Therefore, we are able to tune the

average number of junctions per percolation path using different channel lengths and thus to gradually increase the number of junctions between source and drain contacts, starting with devices without junctions, to some with a few units and finally some with several dozen of junctions. On one hand, by analyzing experimental results with the help of a Lambert W function-based compact model, we have reported that the variation of Si nanonet-FET electrical parameters with geometry and nanowire density can be explained by the threshold voltage dispersion of individual nanowires³⁰. On the other hand, we have recently shown, via temperature-dependent electrical characterizations, that the low-field effective mobility of Si nanonet-FET increases with temperature^{31,32}. A stronger dependence has been found for long channel (\gg nanowire length) than short channel (shorter or equivalent to nanowire length), which has been explained by a thermally activated behavior resulting from the presence of an energy barrier at NW/NW junctions. A bimodal distribution composed of high barriers of about 40-70 meV and low barriers with a height close to 0eV had been able to provide reasonable agreement with experimental results.³¹

On the basis of statistical electrical characteristics, we highlight in this paper the relationship between the number of junctions along conduction paths, estimated by Monte-Carlo simulations, and the electrical characteristics of Si-NN FETs (ON current, OFF current and subthreshold slope). This new findings in combination with our previous work^{31,32} lead us to suggest a physical model, that we call Junction Driven Percolation, to explain the role of junctions and their major impact on device properties. As a consequence, we demonstrate that by controlling properly junction interfaces and device geometry, it is possible to significantly enhance Si nanonet-FETs electrical performance.

II. Experimental details

A. Device fabrication.

Randomly oriented silicon nanowire networks, called nanonets, were integrated into field effect transistors with a bottom gate configuration through standard optical lithography techniques³. The Vapor-Liquid-Solid³³ method was used for the growth of silicon nanowires (SiNWs). A dewetted gold thin film and silane were used as catalyst and precursor respectively, without intentionally introducing any doping gas. In these growth conditions, SiNWs presented a vertical growth along the $\langle 111 \rangle$ axis and a P-type doping³⁴ in the range of 10^{16} cm^{-3} . Gold catalyst was then etched with a sequence of hydrofluoric acid treatment (HF) followed by gold etchant (KI-I_2 based solution). After SiNW dispersion into deionized water using sonication, the amount of SiNWs in solution was controlled by absorption spectroscopy. The suspension is then diluted to reach an absorption of 0.06 at 400nm ⁷. 10 mL of the colloidal suspension were filtered through a nitrocellulose membrane in order to self-assemble the network on the filter whose diameter is 5cm. Finally, a piece of filter is cut and the nanonet was transferred, by filter dissolution, onto 1×1 cm^2 coupons of heavily doped silicon capped by a 200-nm thick silicon nitride layer. The detailed process can be found in Serre et al⁷. As a result of the process, a homogeneous nanonet of about 7×7 mm^2 with a physical density of 0.23 $\text{NWs} \cdot \mu\text{m}^{-2}$ is present at the surface of the substrate. In order to stabilize the electrical properties in air, SiNW/SiNW

junctions were sintered at low temperature via our previously reported process²⁹. As shown in Ternon et al²⁹, in the absence of oxide shell around SiNWs and for diameter in the tens of nanometers, local atomic diffusion occurs at temperature as low as 400°C resulting in the formation of necks at the NW/NW junctions. This phenomenon is called “sintering”. As a consequence of this sintering, the NN, which was an assembly of discrete NWs after assembly and transfer on the substrate, becomes a polycrystalline material in which the NWs remain monocrystalline and are the grains of the polycrystalline material while the NW/NW junctions are the grain boundaries. To quickly resume the process, the native silicon dioxide was first removed by HF treatment and a 1-minute annealing was immediately performed in nitrogen at 400°C to sinter the NW/NW junctions. Due to air break after annealing, another HF treatment was realized before alumina passivation via the atomic layer deposition method in a Fiji F200 Cambridge Nanotech apparatus. An 8-nm thick layer requiring 80 cycles was deposited at 250°C using trimethylaluminum and water as precursors. This passivation layer significantly enhances the NN-FET electrical performance by improving the Si/alumina interface in comparison with Si/native oxide interface³⁵. Electrical contacts were defined into standard reversal photoresist using Süss Microtec MJB3 apparatus and, then, alumina coating in the photoresist openings was removed with HF treatment. Right after, 100 nm of nickel followed by 50 nm of gold were e-beam evaporated. The source and drain contacts were revealed through a lift-off method. Finally, the samples were annealed at 400°C in nitrogen in order to enhance the electrical contact between the metals and SiNWs via silicidation mechanism³. Although this thermal process is identical to the sintering process, it will have no impact on the junctions. Indeed, during the silicidation, the NN is coated with alumina oxide which prevents surface diffusion of the silicon atoms and thus makes low-temperature sintering impossible²⁹.

B. Morphological characterizations.

The morphological characterizations of Si nanonets and transistors were performed by scanning electron microscopy (SEM) with a Hitachi S4100. The analysis of SEM images was realized with the ImageJ software. Statistics relative to the length and width of NWs (Figure 1) were deduced from the analysis of dozens of SEM images: the length of 312 NWs and the diameter of 75 NWs randomly chosen were measured and compiled in the distribution. As fully detailed in Serre et al. ⁷, the SiNW density in nanonets was assessed by several SEM image analysis from the coverage area, τ , defined as the ratio between the surface covered by NWs and the total surface of the sample. We have shown that this coverage area is proportional to the volume of filtered solution, $V_{filtered}$, following an equation dependent on the population of nanowires, here : $\tau = 0.63 \times V_{filtered}$. Then the physical NW density can be estimated by calculating the ratio between the coverage area and the surface covered by each nanowire, using average diameter, d_{NW} , and length, L_{NW} , of SiNWs (Figure 1): $d = \frac{\tau}{d_{NW}L_{NW}}$. For the NWs used in this study, a filtered volume of 10 mL gives a homogenous density of 0.23 NWs. μm^{-2} .

Figure 1: Statistics relative to (A) the length (L_{SiNWs}) and (B) the diameter (D_{SiNWs}) of SiNWs in nanonet. Both parameters were fitted with a log-normal function. 'N' indicates the number of measured nanowires.

In the frame of the percolation theory, the critical percolation density, d_c , defined as the density at which there is a probability of one half to have at least one percolation path connecting the two electrodes, is an important parameter. According to Li and Zhang³⁶, for a given NW length, ℓ and no length dispersion, the critical percolation density can be calculated as: $d_c = \frac{5.637}{\ell^2}$. Taking into account the average NW length, L_{NW} , the critical percolation density for electrical conduction in our case would be $0.12 \text{ NWs} \cdot \mu\text{m}^{-2}$. According to this value, the nanonets studied in this work are in the percolation regime which extend from the critical density ($0.12 \text{ NWs} \cdot \mu\text{m}^{-2}$) to 5 to 7 times its value (0.6 to $0.84 \text{ NWs} \cdot \mu\text{m}^{-2}$)²⁶. However, one has to take into account two important considerations. First of all, contrary to the modelled case, the experimental population of nanowires is widely dispersed (Figure 1), which has a strong impact on the percolation threshold³⁷. Secondly, there may be a difference between the physical density corresponding to the nanowires actually present on the surface, as described above, and the electrical density corresponding to the nanowires that actually play an electrical role within the network. Indeed, in the case of semiconductor nanowires, we have noticed through the study of percolation that the density was often overestimated due to the fact that some nanowires are too resistive to participate in conduction. As a consequence, for a given physical density, to assess the conduction regime, percolating or ohmic, we rely on the finite size scale relationship according to which the conductance of the nanonet is inversely proportional to the length of the channel at the exponent m , called scaling exponent^{16,25-27}. For high densities, $m = 1$ and the material behaves like a thin film. When $m > 1$, the network is in the percolating regime.

C. Electrical characterizations.

Electrical characterizations were carried out with a Karl Süss probe station controlled by a HP4155A parameter analyzer in ambient dark environment at room temperature. Transfer characteristics were recorded from positive to negative gate voltages with a constant drain voltage of -4V or -1V depending on experiments. As previously reported for bare-SiNWs, transistors displayed p-type operation and were operated from the depletion regime in the OFF state to the accumulation regime in the ON state³.

D. Monte-Carlo Simulations.

Monte-Carlo simulations were carried out on Matlab R2016a to gain information about the percolation paths of one given nanonet. Silicon nanowires were considered as sticks²⁰ and were uniformly oriented and generated within an area defined by the channel length (L_c) and width (W_c). The experimental transistor geometry and nanonet morphology were used. Channel width was set at $200 \mu\text{m}$ while channel length, defined as the distance between source and drain contacts, varied from $5 \mu\text{m}$ to $100 \mu\text{m}$. Sticks were

generated with random position and orientation and their length distribution followed a Gaussian law. As is the case experimentally, the NW length mean value is $6.9 \mu\text{m}$ and the standard deviation $2.8 \mu\text{m}$ and the stick density was set at $0.23 \text{ sticks} \cdot \mu\text{m}^{-2}$. Right after, the location of all stick/stick and stick/contact intersections was calculated through mathematical matrix technique³⁸. Each stick in contact with one or other of the metal electrodes is considered to be the starting point of a potential percolation path. Then, from the coordinates of all intersections, percolating paths from the source to the drain and vice-versa are determined on the basis of Dijkstra's algorithm, which is a usual technique to find out the shortest path from one point to another³⁹. To stick to our experimental assumption that NW/NW junctions are the driving mechanism of the conduction in the network, this algorithm was modified in order to first minimize the number of stick/stick intersections and then minimize the distance traveled (See Supporting Information S1). Thus, for each stick directly contacted to either source or drain, all the possible percolating paths that reach the opposite contact were first determined while minimizing the number of stick/stick intersections. Out of all these possibilities, the shortest one was then extracted (Figure S1). Figure 2 gives an example of a randomly generated nanonet (one iteration) for which all the percolation paths, as previously defined, are highlighted in bold red. For each iteration corresponding to a random realization, the main calculated output parameters were the number of percolating paths, N_{pp} , and for each path k ($k \in [1, N_{pp}]$), the number of stick/stick intersections, N_{ssi}^k , and the length of the path, L_{pp}^k . For short channel length (smaller than the NW length), the number of directly bridging sticks, N_{bs} , was also determined. For each length of channel, the random realization was carried out a number of times, called number of iteration, N_{iter} and ranging from 10 to 100 in order to increase the accuracy of the values found (Table 1). For each length, on one hand, the average number of percolating path, $\langle N_{pp} \rangle$ or the average number of bridging stick, $\langle N_{bs} \rangle$ is calculated on the number of iteration ($N_{iter} \in [10, 100]$, Table 1). On the other hand, the average junction number per path, $\langle N_j \rangle$ and the average length of path, $\langle L_p \rangle$ are calculated by averaging over the total number of paths, N_{pp}^{total} , i.e. $N_{pp}^{total} = \sum_{k=1}^{N_{iter}} N_{pp}^k = N_{iter} \times \langle N_{pp} \rangle$ ($N_{pp}^{total} \in [1\ 895, 17\ 224]$, Table 1). For each geometry, the number of iterations has been chosen so that, for the average junction number, the standard deviation is less than 4% of the mean value.

Figure 2 : Highlighting of the percolation paths (in bold red) for a stick density of $0.15 \text{ sticks} \cdot \mu\text{m}^{-2}$. For reasons of clarity, a density lower than $0.23 \text{ sticks} \cdot \mu\text{m}^{-2}$ has been considered and different scales have been chosen for the ordinate and abscissa, giving the impression of preferential orientation of the sticks. The length of the system is $20 \mu\text{m}$ for a width of $200 \mu\text{m}$.

Table 1: Number of iterations and outputs for the Monte Carlo simulations of the transistor as a function of channel length. The density was $0.23 \text{ sticks} \cdot \mu\text{m}^{-2}$ and the channel width was $200 \mu\text{m}$. For each geometry, the number of iteration has been chosen so that, for the average junction number, the standard deviation is less than 4% of the mean value. NA stand for Not Applicable.

Channel length (μm)	5	10	15	20	30	50	100
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Iteration number (N_{iter})	100	100	100	50	50	50	10
Number of direct bridging NWS, $\langle N_{bs} \rangle$	36.7±4.8	2.3±1.5	0	0	0	0	0
Total number of percolation paths, $N_{pp}^{total} = \sum_{k=1}^{N_{iter}} N_{pp}^k$ $= N_{iter} \times \langle N_{pp} \rangle$	NA	NA	17224	8879	9164	9509	1895
Average junction number per path, $\langle N_j \rangle$	NA	NA	3.8±0.1	5.2±0.2	7.8±0.2	12.9±0.2	25.9±0.3
Average length of percolation path, $\langle L_p \rangle$ (μm)	NA	NA	19.2±0.4	25.5±0.4	37.8±0.5	62.2±0.5	123.7±0.6

E. Finite element modelling.

In order to illustrate the formation of the energy barrier at NW/NW junctions and their dependence with substrate bias (acting as gate bias), we performed simple simulations of a 1D gate/gate dielectric/NW/NW stack which represents the simplest model of one NW/NW junction in the nanonet. This was done by solving Poisson equation using the FlexPDE Finite Element Model (FEM) builder for partial differential equations solution. We considered Boltzmann statistics for the holes. All interfaces were assumed ideal, except for the interface between the two nanowires where a uniform density of interface traps in the bandgap, N_{it} , was assumed. The surface charge at this interface was calculated as:

$$Q_s = q \cdot N_{it} \cdot (\phi_s - \phi_F) \quad (1)$$

where q is the elementary charge, ϕ_F is the difference between Fermi level and intrinsic level in the neutral bulk (function of P-type doping level), and ϕ_s is the surface potential resulting from surface band bending, calculated from the difference between the energy of the intrinsic level at the surface and its value in the neutral bulk (local potential). This charge was accounted for as a discontinuity in the normal component of the electric displacement at the interface. Reader can refer to Supporting Information for details.

III. Results and discussion

As detailed in the previous section, the field effect transistors (FETs) manufactured for this work necessitate only standard and low temperature (<400°C) microelectronic technologies. The integration process consists of six main stages: (i) nanowire synthesis; (ii) nanonet self-assembly; (iii) nanonet transfer on substrate; (iv) NW/NW junction sintering; (v) passivation of the nanonet with alumina; (vi) source and drain contact definition and silicidation. The FETs were designed in the bottom gate configuration. The length of the transistor channel was defined by the distance between source and drain and varied, for this study, between 5 and 100 μm , while the channel width was set at 200 μm . Taking into account SiNW length values, which ranged from 2 μm to 16 μm (Figure 1(A)), with respect to channel length, two kinds of transistors were

obtained. (i) When the inter-electrode distance was smaller than maximum nanowire length, the transistor channel consisted of parallel nanowires and the device was called Multiple-Parallel-Channel FET (MPC-FET) (Figure 3(A)). (ii) For an inter-electrode distance larger than nanowire length, the channel consists of several percolation paths. Each path was made of a series of SiNWs separated by SiNW/SiNW junctions whose number depends on channel length. This type of device was named nanonet-FET (NN-FET) (Figure 3(B)).

MPC- and NN-FET Morphology and Geometry. In Figure 3, scanning electron microscopy images illustrate a typical silicon nanowire network right after transfer (Figure 3(C)) and after its further integration into field effect transistors (Figure 3(D)). In nanonets, the mean length and diameter of the silicon nanowires (SiNWs) are $L_{SiNWs}=6.9 \mu\text{m}$ and $D_{SiNWs}=39 \text{ nm}$, with a standard deviation of $2.8 \mu\text{m}$ and 7 nm , respectively, as shown in Figure 1. All SiNWs are single crystals with $\langle 111 \rangle$ growth direction²⁹ and are laid randomly on the substrate so that the $\langle 111 \rangle$ direction is parallel to the substrate surface. As a result, nanowires are randomly oriented relative to each other. Thus, during the sintering step, which is necessary to stabilize the electrical properties of the network²⁹, there is a crystallographic mismatch at the NW/NW junctions which results in the formation of grain boundaries²⁹. Therefore, a Si nanonet is a polycrystalline silicon network composed of grains –the monocrystalline silicon nanowires– separated by grain boundaries –the SiNW/SiNW junctions. All the nanonets studied in this work exhibit a constant density of $0.23 \text{ NWs} \cdot \mu\text{m}^{-2}$.

Figure 3: (A-B) Schemes of the two possible transistor configurations based on Si nanonet: (A) Multiple-Parallel-Channel FET (MPC-FET) and (B) Nanonet-FET (NN-FET). For MPC-FET, current can flow through SiNWs directly bridging the source and the drain whereas, for NN-FETs, the current must flow via percolating paths that involve SiNWs and SiNW/SiNW junctions. The channel length (L_c), corresponding to the Source-Drain distance, varies from $5 \mu\text{m}$ to $100 \mu\text{m}$ whereas the channel width (W_c) is fixed at $200 \mu\text{m}$. (C) SEM image of a typical Si nanonet elaborated with 10 mL of colloidal SiNW suspension corresponding to a density of $0.23 \text{ NWs} \cdot \mu\text{m}^{-2}$. (D) SEM top-view of Si nanonet field effect transistor after processing. The $200 \mu\text{m} \times 200 \mu\text{m}$ squares correspond to the Source/Drain contact pads.

If we consider the nanowire length dispersion, it is possible to state that a channel length of $5 \mu\text{m}$ is associated with an MPC-FET. Then, for 14% of the NW population (Figure 1(A)), NW length exceeds $10 \mu\text{m}$, so that the devices with $10 \mu\text{m}$ channel lengths will have a high probability of being MPC-FETs but with a reduced number of parallel nanowires. Finally, all the devices with a channel longer than $15 \mu\text{m}$ will be NN-FETs because less than 1% of the NWs are longer than $15 \mu\text{m}$ (Figure 1(A)).

Percolating Channel Modeling. In order to define more precisely the nature and dominant composition of the transistor channels, Monte-Carlo simulations were carried out according to the principle of stick percolation^{15,16,20}. The experimental characteristics of our devices were used to set up the simulations: nanowire length distribution, nanonet density and transistor geometry (fixed width, variable length). For each Monte Carlo-generated nanonet, when they exist, the position of each NW/NW junction was

determined. Likewise, all the percolation paths connecting the source to the drain were defined. Each of these paths was optimized on the basis of two criteria: minimizing first the number of junctions, then the length of the path as described in the experimental section. Finally, for each randomly simulated nanonet, we determined the number of nanowires directly bridging source and drain and the number of junctions per path, which was determined by first minimizing the number of stick/stick intersections and then minimizing the distance traveled. The operation was repeated a sufficient number of times so that the standard deviation on the number of junctions for each channel length was lower than 4% of the average value (Table 1). The average number of junctions per percolation path and the average number of nanowires bridging source and drain are presented in Figure 4 as a function of channel length. As expected, the transistors are MPC-FETs when channel length is 5 and 10 μm with an average of 37 and 2 NWs directly bridging the two electrodes, respectively. Above 15 μm , the transistors are NN-FETs without bridging nanowires and with a number of junctions per percolation path larger than 3 and increasing up to 26 for a 100 μm long channel. In addition, beyond 15 μm , the number of junctions per path exhibits a good linear correlation with channel length despite the large standard deviation of SiNW length (2.8 μm).

Figure 4: Average number of direct bridging SiNWs (left axis) and average junction number per percolating paths ($\langle N_j \rangle$, right axis) as a function of the channel length (L_c) using Monte-Carlo simulations. For all of these simulations, the experimental parameters of the transistor geometry and nanonet morphology were chosen. The channel width was set at 200 μm while the channel length varies from 5 μm to 100 μm . For the nanonet morphology, nanowires are considered as sticks with a length of $6.9 \pm 2.8 \mu\text{m}$ and SiNW density corresponds to $23 \times 10^6 \text{ SiNWs.cm}^{-2}$. Beyond 15 μm , $\langle N_j \rangle$ exhibits a good linear correlation with the channel length despite the high standard deviation of SiNW length (2.8 μm).

MPC-FET and NN-FET Electrical Behavior. Figure 5(A) shows the typical evolution of the transfer characteristics when channel length varies between 5 and 100 μm . In addition to an expected decrease of ON current from about 8 μA down to 20 nA, a surprising and significant diminution of the subthreshold slope and of the OFF current were observed when increasing channel length. To accurately determine the impact of channel length on electrical properties, ON current (defined as I_d at $V_g = -25 \text{ V}$, $V_d = -4 \text{ V}$), OFF current (extracted in the OFF state), subthreshold slope and threshold voltage (extracted by extrapolation in linear region in linear scale) were carefully extracted for approximately seventy transistors. In Figure 5(B), where each characterized transistor was placed in the I_{On}/I_{Off} plane, an interesting trend is observed. First, when channel length varies from 5 μm to 20 μm , the OFF current decreases very strongly over five orders of magnitude while the ON current decreases slightly, which results in a drastic increase in the ON-to-OFF ratio. On the contrary, for channels longer than 30 μm , the OFF current remains stable at values as low as 10^{-13} - 10^{-12} A while the ON current begins to decrease rapidly. Therefore, in terms of ON-to-OFF ratio, an optimum emerges for a channel length of 30 μm , with outstanding values exceeding 10^5 . Similarly from Figure 5(C), a clear improvement in the subthreshold slope is observed when L_c varies from 5 μm to 20 μm down to about

1 V.dec^{-1} for devices longer than $30 \mu\text{m}$. Finally, the threshold voltage increases when L_c raises from 5 to $20 \mu\text{m}$ and then it monotonously decreases when L_c is longer than $20 \mu\text{m}$ (Figure 5(D)). It should be noticed that the values of V_{th} for devices with $L_c = 5 - 10 \mu\text{m}$ should be used with caution as its extraction is highly imprecise due to their weak current modulation as well as their high subthreshold slope. According to these experimental results, channel length drastically impacts the electrical characteristics of FETs and the best performance, in terms of ON-to-OFF ratio and subthreshold slope, were obtained for $30 \mu\text{m}$ -long channel FET for the given NW density and length.

Figure 5: Study of transistor electrical properties for various channel lengths. (A) Typical transfer characteristics from 5 to $100 \mu\text{m}$ at $V_d = -4 \text{ V}$. (B) ON current (I_{on}) as a function of OFF current (I_{off}). The ON current is defined as I_d at $V_g = -25 \text{ V}$, $V_d = -4 \text{ V}$, (C) subthreshold slope (SS) and (D) threshold voltage (V_{th}) for various channel lengths extracted for about seventy transistors. For (B), the ON-to-OFF ratio (I_{on}/I_{off}) is indicated by the dashed lines.

According to these results, the MPC-FETs performance are worse than that of NN-FETs. To better understand such a degradation, single SiNW-FETs have been fabricated for comparison with MPC-FETs and NN-FETs, as displayed in Figure 6. One can notice that the performance of the single NW-FET (Figure 6) are good with ON-to-OFF ratio about 10^4 , an OFF current in 10^{-14} A range and a subthreshold slope of about 210 mV.dec^{-1} . As a consequence, the high OFF current level and the bad subthreshold slope in the MPC-FET (Figure 6) cannot be directly attributed to the individual SiNW properties. Moreover, according to the modelling, the number of direct bridging SiNWs in MPC-FET for the experimental density of $0.23 \text{ NWs.}\mu\text{m}^{-2}$ is about 37 (Figure 4). Then, one has to keep in mind that the NW diameter dispersion is wide (Figure 1) and that it implies a significant variation in nanowire threshold voltage²⁹. As a consequence, the MPC-FETs properties are the results of the superposition of almost 40 NW-FETs in parallel, which contributes to explain the higher I_{on} value for MPC-FET than for single NW-FET, but also the subthreshold slope degradation, as detailed in the last part of the paper. By comparison, the NN-FET performance (Figure 6) with a channel length of $50 \mu\text{m}$ are as interesting as that of the single NW-FET with a channel length of $3 \mu\text{m}$.

Figure 6 : Typical transfer characteristic at $V_d=-1\text{V}$ for Single SiNW-FET with $L_c=3\mu\text{m}$ (black), MPC-FET with $L_c=5\mu\text{m}$ (blue), NN-FET with $L_c=50\mu\text{m}$ (red). Color on-line.

In the literature, similar trends of the ON-to-OFF ratio were observed for field effect transistors made of carbon nanotube (CNTs) networks^{40,41} when the channel length decreases. According to these authors, this trend is linked to the systematic presence of metallic CNTs among the semiconducting CNTs. Indeed, for a given ratio of metallic CNT (typically $<1/3$), the probability to form metallic conducting paths increases when channel length decreases. As a result, a drastic augmentation in the OFF current occurs and therefore a decrease in the ON-to-OFF ratio, just as we observe with our experimental results. Nevertheless, none of the

SiNWs involved in the nanonet studied here is metallic as their non-intentionally P-type doping level³⁴, in the range of 10^{16} at.cm⁻³, is far from the degenerated range⁴². As a consequence, the hypothesis proposed for the CNT case is not applicable to explain the observed degradation when the channel length decreases and other phenomena have to be taken into account. Particularly, thorough studies of silver nanowire²² and CNT^{8,28,43} networks showed that, in case of metallic nanowire network, junctions between nanostructures play an essential role in the network conduction. Indeed, even in low proportion, high resistive junctions may limit the ultimate conduction in the overall network.

As far as we know, no studies of the electrical properties of the silicon NW/NW junctions have been specifically reported in the literature. However, according to our previous reported work²⁹, when NW/NW sintering occurs at 400°C for 1 minute, as done in this work, a neck appears where the two NWs are touching each other and the neck size at the junction is about 10% of the SiNW diameter. Thus, at each junction, the charge carriers cross an area 100 times smaller in section than that of the nanowire. The resistance being inversely proportional to the section, the lineic junction resistance will be thereby at least two orders of magnitude higher than SiNW lineic resistance itself. Moreover, thanks to the HRTEM observations²⁸, we evidenced the presence of crystallographic defects at the junctions, essentially dislocations, which are expected to feature a large density of traps, leading to the formation of energy barriers along the conduction paths. In addition to these purely material considerations, we have recently shown, via temperature electrical characterizations, that the low field effective mobility of Si nanonet-FET increases with the temperature^{31,32}. It has been found that the results can be explained by the presence of energy barriers at NW/NW junctions. Moreover, the observed trends have suggested that these energy barriers might feature a bimodal distribution, with high barriers of about 40-70 meV and low barriers with a height close to 0eV. As a consequence, the role of junctions have to be explored in connection with the studied regime of the FETs, ON state, commutation state and OFF-state.

Experimental investigation of junction contribution in the ON state. The behavior of one particular junction can be investigated with the four-probe technique²². However, such experimental setup gives information about one junction only when hundreds of junctions can be involved in a NN-based FET. The strategy we developed here was to gradually increase the length of the channel FET in the range 5-100 μm so that more and more junctions were involved in conducting paths. According to the work of Alam *et al*²⁵⁻²⁷, the study of the network conductance in the ON state gives information about the electrical properties of junctions with respect to that of nanostructures. Such conductance (G_{On}) is defined as the ratio between the drain current in the ON state (Figure 5(B)) and the drain voltage ($V_d = -4\text{ V}$). For the current extractions in the ON state, a gate voltage of -25 V was chosen as it is far from the typical threshold voltage (0-12V) of our devices (Figure 5(D)). The conductance, depicted in Figure 7 as a function of channel length, exhibits a clear deviation to the main trend when channel length is shorter than the NW length ($L_C \leq 10\mu\text{m}$). According to the Monte-Carlo simulations, which account for the experimental distribution in SiNW length and for FET geometry (Figure 4),

the deviation to the trend corresponds to the involvement of NWs directly bridging the two metallic contacts. Indeed from 5 μm to 10 μm , about 37 to 2 NWs directly bridge the electrodes (MPC-FET) whereas, beyond 15 μm long channel, charge carriers have to cross at least one junction to flow from source to drain (NN-FET).

Figure 7: This figure displays the evolution of the ON conductance, ratio between the ON current at gate voltage of -25V and the drain voltage (-4V), with the channel length. For MPC-FETs (5 and 10 μm) the standard scaling law materialized by dashed line is reported and applies quite well: the conductance is inversely proportional to the channel length. For NN-FETs, as predicted by the percolation theory whereby the conductance is inversely proportional to the channel length at the scaling exponent 'm', the conductance can be well fitted with linear equation beyond 15 μm , giving a conductance exponent of 2.72 and suggesting that the electrical density is closed to the percolation threshold.

According to the percolation theory^{16,25-27}, for NN-FETs, the network conductance can be described by the finite size scale relationship: $G_{On} \propto \frac{1}{L_{SiNWs}} \left(\frac{L_{SiNWs}}{L_c} \right)^m$. L_{SiNWs} represents the nanowire length and m is a percolating parameter, called scaling exponent ($m > 1$), which depends on stick density. For high densities, $m = 1$ and the material behaves like a thin film. When $m > 1$, the network is in the percolating regime. In this frame and according to simulations carried out by Pimparkar and Alam²⁷ for CNT nanonet-based FETs, the scaling law applies with $m = 1$ for MPC-FETs and with $m \geq 1$ for NN-FETs. Moreover, in systems, where the dimensionless charge-transfer coefficient between tubes²⁷ ($R_{NW}/R_{junctions}$) is close to 1, no discontinuity is observed at the transition between short-channel and long-channel devices, whereas in case of low charge transfer coefficient ($< 10^{-1}$), an important discontinuity is noticed. Obviously, the absence of discontinuity in Figure 7 suggests that in the ON-state of the NN-FETs the NW/NW junctions are quite good and allow good conduction. For MPC-FETs (channel length $\leq 10\mu\text{m}$), due to the low number of experimental points, no fit is applied but the standard scaling law according to which the conductance is inversely proportional to the channel length is reported and is in quite good accordance with the experimental results. In contrast, for NN-FETs (channel length $> 10\mu\text{m}$), the material is clearly in the percolating regime with a scaling exponent m equal to 2.72. As a conclusion, we have here the confirmation that, in the percolation regime, once the NN-FETs are in the ON-state, the NW/NW junctions are not a limiting mechanism. The step forward, described in the following, is then to determine the role played by the presence of energy barriers at NW/NW junctions and particularly how they impact the subthreshold slope and the OFF current. At least and as developed below, an important element to understand is whether the junctions are responsible for the better performance of long channel devices (NN-FET) compared to short channel devices (MPC-FET) (Figure 5).

Si nanonet as Si polycrystalline thin film. Because of the sintering step and as shown by our previous microstructural study²⁹, the Si nanonet is in fact a polycrystalline silicon network composed of grains – monocrystalline SiNWs – and grain boundaries – SiNW/SiNW junctions. Therefore, we propose to adapt the

well-known barrier model developed for the electrical transport in polycrystalline silicon^{44,45} to the percolating SiNW network. According to Seto's model⁴⁴, the presence of dangling bonds located at the grain boundaries results in the formation of energy levels in the bandgap, which are capable of trapping and detrapping free carriers. The associated grain boundary charge builds an energy barrier which prevents the injection of low energy carriers from one grain to the other. In addition, for poly-Si field-effect-transistor, it has been shown that^{46,47}: (i) the grain boundary (GB) potential barrier height is modified by the gate bias; (ii) the GB potential barrier helps in the suppression of off-current and in the improvement of subthreshold behavior. More recently, with the same argues, Liu et al⁴⁸ demonstrated that the energetic barriers present at the grain boundaries of printed polycrystalline ZnO nanowires suppress the OFF current in the devices. Keeping in mind that the spatial arrangement of gate, grains and GBs in a nanonet is not the same as in a poly-Si film or in polycrystalline ZnO NWs, and considering the grain boundary height barrier modification by field effect, we propose in the following a physical model to understand the role of the NW/NW junctions in the electrical behavior of Si NN-FETs.

Physical model for Si NN-FET. A full modelling of hole transport through a nanonet and of the role of NW/NW junctions would require quite involved simulation approaches which are beyond the scope of this paper. However, some rough trends can be drawn based on simple considerations. In the following, we will discuss a very simple model for a NW/NW junction in the nanonet, which corresponds to the crossover of two nanowires with substrate voltage control (Figure 8(A)). As for polycrystalline silicon⁴⁴, NW/NW junctions are expected to feature a large density of traps, leading to the formation of energy barriers. With the aim of evidencing rough trends, we used FlexPDE to solve the 1D Poisson equation under the assumption of a uniform density of states N_{it} at the grain boundary. The modelled structure was a typical MIS stack composed of bottom substrate contact, gate dielectric (200-nm thick silicon nitride) and two stacked nanowires separated by a grain boundary (Figure 8(B)). All other interfaces were considered as ideal. The reference potential was taken at flat band (V_{fb}). The diameter of the bottom NW (NW1) was taken equal to the mean experimental value (40 nm) while the diameter of the top nanowire (NW2) was set at 100 nm to reach equilibrium. All details about the equations solved and their limiting conditions are given in Supporting Information S2.

Figure 8: (A) Schematic representation of the crossover between two nanowires, one sectioned along its length (NW1) and the other one across (NW2). Substrate bias acts as a gate bias in this bottom-gate FET configuration. (B) Simplified 1D scheme used to calculate charge and potential distribution at the centerline of NWs crossover. The simulated stack consisted of 200nm Si_3N_4 (gate dielectric), 40nm Si (NW1), 100nm Si (NW2). A density of interface states N_{it} was assumed at the grain boundary between NW1 and NW2. All other interfaces were assumed ideal. Gate voltage (V_g) values are calculated with reference to flat band conditions.

Figure 9 depicts the valence band diagram after 1D Poisson equation resolution (A) without and (B) with a GB interface state density of $5 \times 10^{11} \text{ cm}^{-2} \cdot \text{eV}^{-1}$ for three different values of gate voltages (V_g) which were

taken in depletion regime ($V_g - V_{fb} = 1.73V$), accumulation regime ($V_g - V_{fb} = -1.03V$) and strong accumulation regime ($V_g - V_{fb} = -9.31V$). In the absence of interface states (Figure 9(A)), the GB is ideal and the two NWs act as a single semiconducting region. A classical upward (downward) band bending is observed in accumulation (depletion) regime. With interface states (Figure 9(B)), a potential energy barrier builds up at the GB and the influence of gate voltage on the top nanowire NW2 is mostly screened by interface charge modulation. Barrier height was calculated as the difference between the position of the valence band at the GB which were calculated in the presence and in the absence of interface states. As shown in the inset of Figure 9(B), this barrier height depended on gate voltage, with smaller values in accumulation than in depletion.

Figure 9(B) shows that the crossover between two nanowires is expected to add a potential barrier along current paths in any case, due to the weaker control of the gate on the top nanowire. However, even if hole concentration is smaller at the level of NW2, both nanowires operate in the same regime. The presence of GB traps would add an interesting feature as it builds a depleted region across the current path. Conduction is then primarily limited by the junctions, so that we may define a concept of “Junction Driven Percolation” to describe this system, with a threshold voltage at junctions (V_{th}^j) smaller than that of nanowires (V_{th}^{NW}). In accumulation, ON current should be relatively unaffected by GB traps as long as the barrier height added by GB traps is smaller than thermal voltage^{46,47}. In contrast, the larger barrier in depletion would be in favor of reduced OFF current and steeper subthreshold slope.

Figure 9: Valence band diagrams obtained after the resolution of 1D Poisson equation (A) without and (B) with a GB interface state density (N_{it}) of $5 \times 10^{11} \text{ cm}^{-2} \cdot \text{eV}^{-1}$ for three different conditions: depletion ($V_g - V_{fb} = 1.73V$), accumulation ($V_g - V_{fb} = -1.03V$) and strong accumulation ($V_g - V_{fb} = -9.31V$). Values of energies on the y-axis are provided with the usual sign convention (positive energies upwards for electrons). Holes energies have the opposite sign (positive energies downwards for holes). The inset for (B) represents the evolution of the GB barrier height as a function of $V_g - V_{fb}$, hole convention is used.

For a better understanding of the GB role, we investigated in Figure 10 the influence of (A) interface state density and (B) NW1 diameter on the junction threshold voltage V_{th}^j . V_{th}^j is defined as the voltage below which gate control of NW2 becomes screened by GB traps and potential barrier at the GB reaches its minimum value. On one hand, as expected, in Figure 10(A), the increase in interface state density at GB translates into an elevation of the potential barrier height so that percolation path opening occurs at lower gate voltage impacting the threshold voltage and subthreshold behavior of the NNFET. In our previous experimental work, from temperature measurement of low field effective mobility^{31,32}, we have reported barrier height values in the range of $0.040 - 0.070 \text{ eV}$, which, according to the present simulation (Figure 10(A)), might correspond to an interface state density at the NW/NW junctions in the range $10^{12} - 2 \times 10^{12} \text{ cm}^{-2} \cdot \text{eV}^{-1}$, although this comparison should be taken with much care considering the rough assumptions laying behind the 1D simulation of barrier height done here and the fact that the bimodal distribution of experimental barrier

heights proposed in [32] was only the simplest assumption that was able to fit experimental dependence of I-V characteristics with temperature. Nonetheless 1D simulation can provide information about trends. The impact of NW diameter on the barrier height is shown on Figure 10(B). The increase of the NW1 diameter shifts the curves, and the junction threshold voltage V_{th}^j , towards positive values while the barrier in accumulation regime remains almost constant. As a conclusion, on the basis of the resolution of the 1D Poisson equation, we demonstrate that the junction threshold voltage V_{th}^j is directly linked to interface state density at the GB and to bottom NW diameter. This junction threshold voltage is shifted towards low values when interface state density increases or NW diameter decreases.

Figure 10: Evolution of the GB barrier height as a function of gate voltage for (A) different interface state densities and (B) different NW1 diameters as obtained from numerical finite elements simulations. For (A), the NW1 diameter was set at 40 nm while for (B) interface state density was $10 \times 10^{11} \text{ cm}^{-2} \cdot eV^{-1}$. The junction threshold voltage V_{th}^j corresponding to the barrier lowering is indicated on the curve. V_{th}^j is defined as the voltage below which gate control of NW2 becomes screened by GB traps and potential barrier at the GB reaches its minimum value.

Now that the role of the NW/NW junctions is clearly defined and translated in terms of junction threshold voltage, we can consider a nanonet involving many nanowires and junctions by relying on statistics. First, the nanonet is composed of NWs that exhibit diameter dispersion (Figure 1(B)). Second, because of such NW diameter dispersion, the grain boundaries formed at NW/NW junctions upon sintering²⁹ are not homogenous and the interface state density is different from one junction to another. The first consequence of the NW diameter dispersion is a significant variation in nanowire threshold voltage³⁰. The second consequence, observed in Figure 10, is that the junction threshold voltage (V_{th}^j) is affected by both interface state density and NW diameter. For the sake of simplicity, Gaussian distributions were assumed both for nanowire threshold voltage V_{th}^{NW} (plotted in blue in Figure 11(B)) and for junction threshold voltage V_{th}^j (plotted in red in Figure 11(B)). The reasoning would be the exactly the same with other distributions. In accordance with the above stated arguments, in average, the junction threshold voltage is below that of NW ($\langle V_{th}^j \rangle < \langle V_{th}^{NW} \rangle$), but the two distributions can overlap.

According to the percolation theory, conduction in nanonet occurs through several conduction paths (Figure 2), whose number depends on nanonet density, channel width and length and each of them is composed of $\langle N_j \rangle$ junctions and $\langle N_j \rangle + 1$ NWs (Table 1). On the basis of the Junction Driven Percolation mechanism, when sweeping the gate voltage from the OFF state to the ON state (gate voltage larger to smaller than flat band voltage), each conduction path remains in the OFF state until the junction with the lowest junction threshold voltage in the path turns to the ON-state. Finally, the NN-FET turns from the OFF to the ON state as soon as a first conduction path is turned to the ON-state. As a consequence, when the number of NW involved is sufficiently important to rely on statistics, the NN threshold voltage (V_{th}^{NN}) corresponds to the lower edge of the V_{th}^j distribution, independently of the NW characteristic (purple curve in Figure 11(A)). This has two

important consequences for the electrical performance of the NN-FETs. First, as an NN-FET can turn to the ON-state only if the lowest V_{th}^j from one percolating path has been overcome, an abrupt commutation from the OFF to the ON state is expected, and thereby a good subthreshold slope. Second, such an abrupt commutation is only possible if the behavior relies on statistics, that is to say, if the ratio L_c/L_{SiNWs} is sufficiently large so that numerous NWs and junctions are involved in conduction. However, it is difficult to quantify exactly in terms of probability the limit at which a finite size NN obeys to statistical laws. Therefore, we prefer to rely on our experimental results as we were able to observe this phenomenon (Figure 5).

Indeed, in Figure 5(C) and (D), we observe the decrease of the subthreshold slope and of the threshold voltage when the ratio L_c/L_{SiNWs} is increasing from 2 ($L_{channel}=15\mu m$) to 15 ($L_{channel}=100\mu m$). Thus, as the channel length rises, more and more junctions are involved in each percolation path (Figure 4) and the probability that each path contains a junction with a very low threshold voltage V_{th}^j increases. Consequently, the resulting threshold voltage of the transistor is shifted toward lower values and the subthreshold slope improves.

Figure 11: Schematic representation of the Junction Driven Percolation mechanism for MPC-FET and NN-FET. In panel A, typical experimental output characteristic for MPC-FET and NN-FET were used to illustrate our explanations. Due to SiNW diameter dispersion, Gaussian distributions were assumed for V_{th}^{NW} and V_{th}^j (panel B). As the potential barrier lowering at the junction occurs only once the apparition of hole accumulation in NWs, V_{th}^j is lower than V_{th}^{NW} for P-type doped SiNWs. Therefore, the highest junction potential barrier of each percolating path, thereby the lowest V_{th}^j , will limit the conduction in the network. This limitation results in low OFF current and steep transistor commutation for NN-FET (panel A, purple triangles). On the contrary, for MPC-FET, conduction is driven by direct bridging SiNWs. Due to V_{th}^{NW} dispersion, each bridging SiNW progressively turns ON when sweeping the gate voltage from highly positive down to negative values. MPC-FETs display thus high OFF current and poor commutation (panel A, dark blue squares). V_{th}^{NN} and V_{th}^{MPC} are the resulting threshold voltages for NN-FET and MPC-FET, respectively.

MPC- versus NN-FETs. With the help of this physical model for nanonets, we can now interpret the substantial differences of electrical performances between MPC-FETs and NN-FETs (Figure 5) in terms of absence or presence of NW/NW junctions, respectively. In the schematic representation in Figure 11(A) are reported the typical transfer characteristics for an MPC-FET (dark blue line and square) and an NN-FET (purple line and triangles) with respect to illustrative Gaussian distributions for the NW and junction threshold voltages.

For the MPC-FETs, current flows directly from the source to the drain via several bridging SiNWs and no junction is involved in the conduction. Due to the SiNW threshold voltage dispersion³⁰, each SiNW contributing to the conduction commutes from the OFF to the ON state for different gate voltages (Figure 11(B)). First, as soon as one bridging SiNW is turned ON, current can flow between the contacts and the current increases meaningfully. As a consequence, the MPC-FET electrical characteristic arises from the superposition of the electrical characteristic of each SiNW bridging the source and the drain. Thus, when sweeping the gate voltage from highly positive down to negative voltage, the progressive commutation of

each SiNW from the OFF to the ON state drastically degrades the subthreshold slope of the MPC-FET. Finally, the MPC-FET is fully ON, when the last NW is turned ON.

By contrast, for the NN-FETs, SiNW/SiNW junctions are the key element that governs the conduction by the previously described limiting mechanism (Junction Driven Percolation). As stated above, the current cannot flow through a given percolation path until all the junction barriers have been lowered, which results in a significantly lower OFF current than for the MPC-FETs (Figure 11), a better subthreshold slope and a lower threshold gate voltage, provided that enough nanowires are involved in each conduction path and that the nanonet's behavior follows statistical laws, that is to say, the NN is large enough to involve numerous NWs and junctions. In our experimental conditions, it seems that a channel length of 30 μm is needed to fulfil this condition.

To sum up, our conduction model, the Junction Driven Percolation, that combines the percolation theory^{15,16}, the concept of polycrystalline silicon electrical transport⁴⁴ and the principle of potential barrier lowering by field effect⁴⁶ is well suited to explain the much better electrical performance of the NN-FETs compared to the MPC-FETs, including the better OFF state and the improved subthreshold slope (Figure 5).

Optimum in the electrical performances of NN-FETs. In Figure 5, we experimentally observed that an optimum channel length emerges in terms of ON-to-OFF ratio and subthreshold slope at 30 μm . For the shorter NN-FETs, only few SiNW/SiNW junctions are involved in each conducting path: as shown in the Monte-Carlo simulations (Figure 4), 4 to 5 junctions are typically involved in each conduction path for a channel length of about 15 to 20 μm . From a statistical point of view, such a small number of junctions does not allow to cover uniformly the whole V_{th}^j distribution (Figure 11) and hence does not guarantee that the lower edge of the Gaussian distribution is represented. As a consequence, the Junction Driven Percolation mechanism is not fully operational, which results only in a small reduction of the OFF current and of the subthreshold slope. On the other hand, by increasing channel length, the number of junctions within each percolation path rises (Figure 4). As a result, the Gaussian distribution of V_{th}^j can be covered more uniformly and the probability of finding, in each percolation path, a junction with the lowest junction threshold voltage of the Gaussian distribution increases. According to the experimental results (Figure 5), 30 μm is the minimal channel length necessary to stabilize the OFF current at a very low value (10^{-13} - 10^{-12} A) and to meet the most abrupt subthreshold slope, around 1V.dec^{-1} (Figure 5(B) and (C)). So, according to the Monte-Carlo simulations (Figure 4), a minimum of 8 SiNW/SiNW junctions is required to ensure statistically a low V_{th}^j in each percolation path and to fully benefit from the Junction Driven Percolation mechanism. However, beside this beneficial effect of the increasing number of junctions in the percolation paths, according to the percolation theory and the scaling law, the ON current decreases quickly when channel length increases (Figure 7). The combination of these two opposite effects results in the existence of an optimal channel length for a given channel width and a given nanowire density, leading to best performance for the nanonet based

transistor. We are currently exploring the role of nanowire density and our initial results suggest that the optimal channel length strongly depends on the NW density and increases with it. Moreover, based on our simulations, we can also assume that the optimal channel length depends on the NW length.

Conclusions

Using our original technological process to fabricate long-channel silicon nanonet-based transistors, we thoroughly investigated in this paper their electrical properties for various channel lengths. A strong correlation between channel length and transistor parameters (OFF current, ON current, ON-to-OFF ratio and subthreshold slope) were highlighted. According to these results, we experimentally showed that nanowire/nanowire junctions play a fundamental role in the electrical conduction of the overall network through a limiting mechanism. On the basis of the percolation theory^{15,16} combined with a model for electrical transport adapted from that in polycrystalline silicon⁴⁴ and with the principle of potential barrier lowering by field effect⁴⁶, we proposed the Junction Driven Percolation mechanism in which each junction is considered as a potential barrier that can be lowered by field effect.

Using this approach, we suggest that the significant enhancement and stabilization of electrical performance observed experimentally with channel length increase are directly linked to the nanowire/nanowire junctions. On the basis of this model and of our experimental evidences, we show that junctions play a key role in the behavior of transistors as they improve significantly the electrical performances by minimizing and stabilizing the OFF current as well as the subthreshold slope. As a consequence, by controlling properly the junction interfaces and device geometry, Si nanonet-FET electrical properties can be significantly enhanced. NW/NW junctions can be seen as a promising alternative to improve the electrical performances of NW-based devices provided that enough nanowires and junction are involved in each conduction path and that the nanonet behavior follows statistical laws. On the basis of this work, the impact of the SiNW density on the FET electrical performance will be investigated.

Supplementary Material

The online version of this article contains supplementary material about the percolation path determination in the Monte-Carlo simulations and that gives Details on FEM simulation used for 1D Poisson equation for Fig. 9 and Fig. 10 in paragraph « Physical model for Si NN-FET ».

Acknowledgments

This work has received funding from the EU H2020 RIA project Nanonets2Sense under grant agreement n°688329. This work was partly supported by the French RENATECH network. This work has received funding from the EU H2020 ERA-NET project Convergence. This work benefited from the facilities and expertise of the OPE)N(RA characterization platform of FMNT (FR 2542, fmnt.fr) supported by CNRS, Grenoble INP and UGA and PTA (Upstream Technological Platform), cooperated by CNRS Renatech and CEA Grenoble, France.. The authors want to thank Maryline Bawedin (IMEP-LaHC) for fruitful discussion.

Data availability statements

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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PLEASE CITE THIS ARTICLE AS DOI: 10.1063/1.50023322

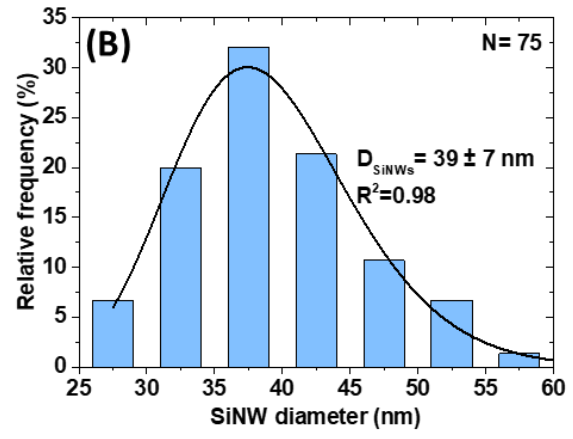
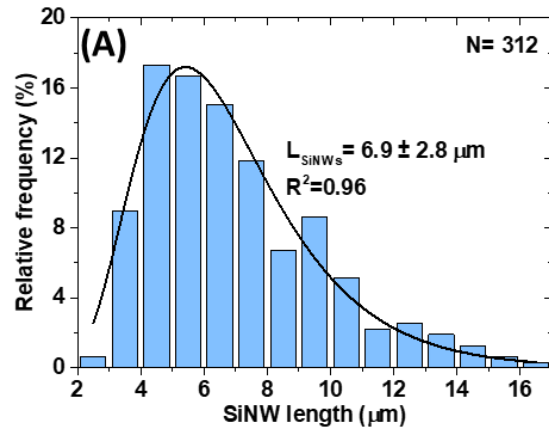
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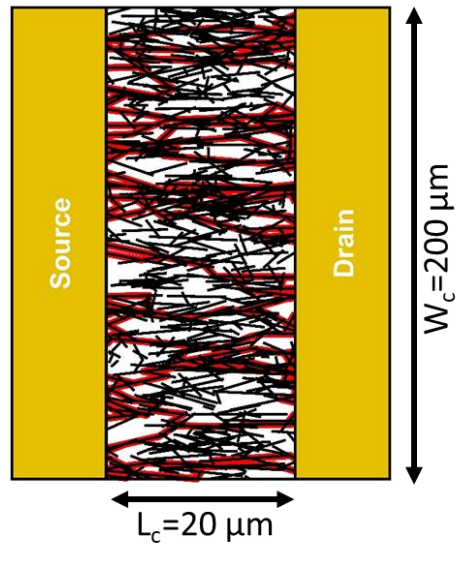
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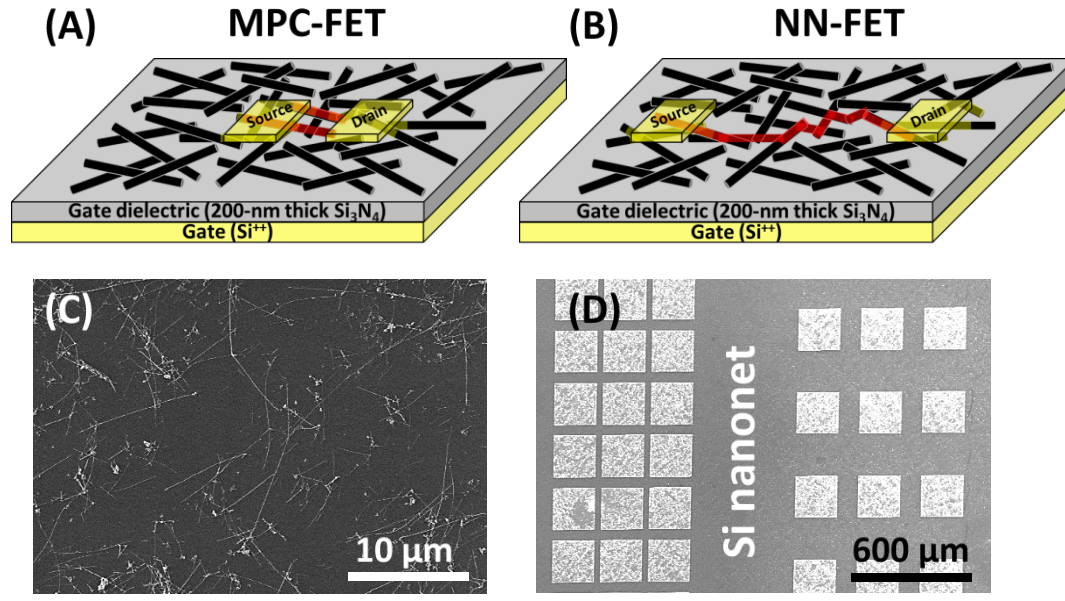
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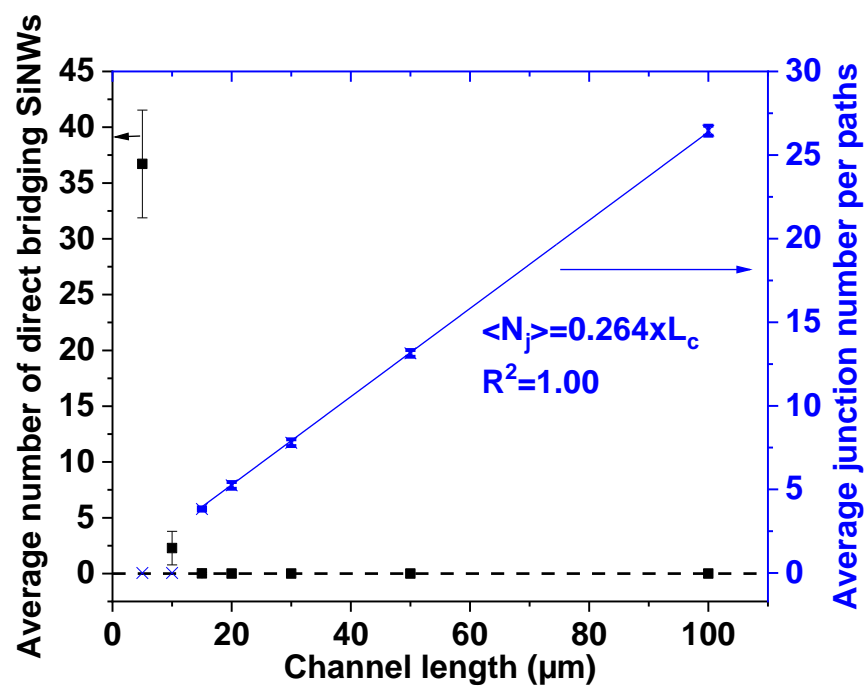
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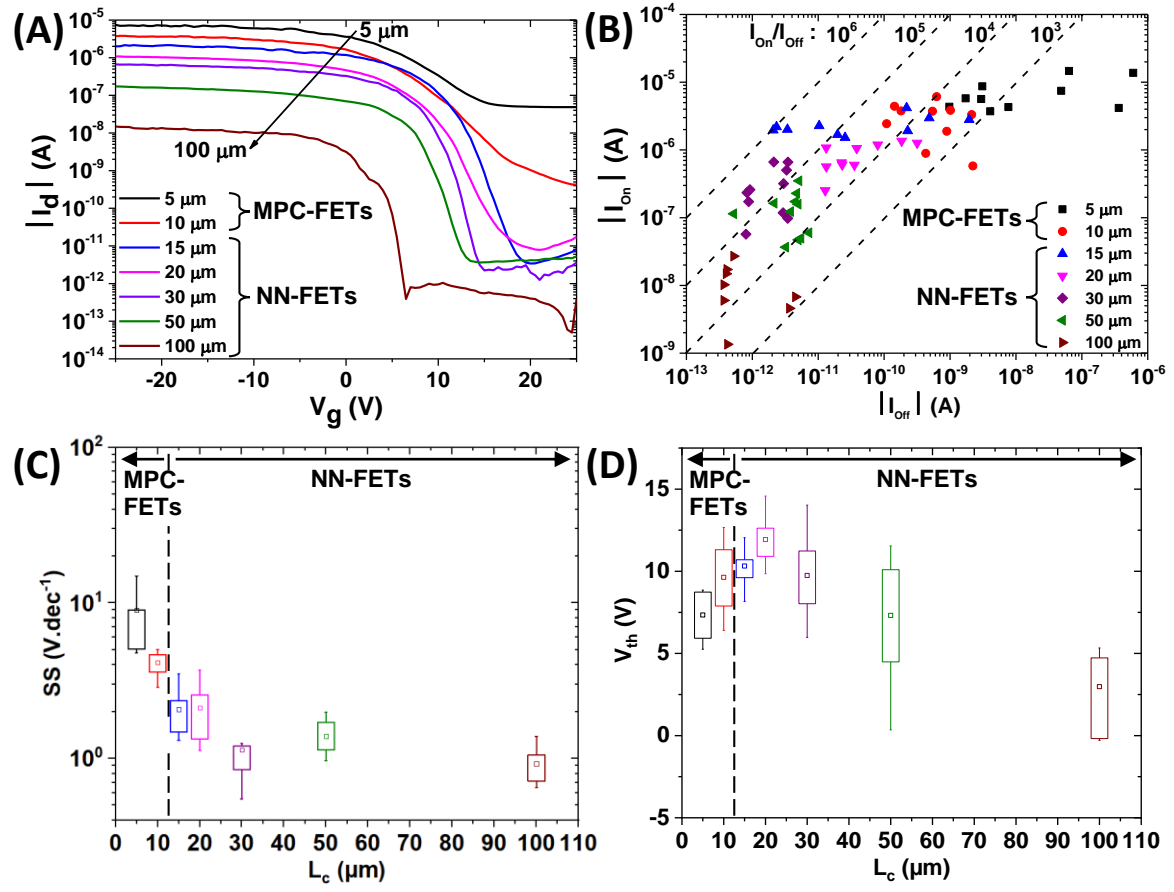
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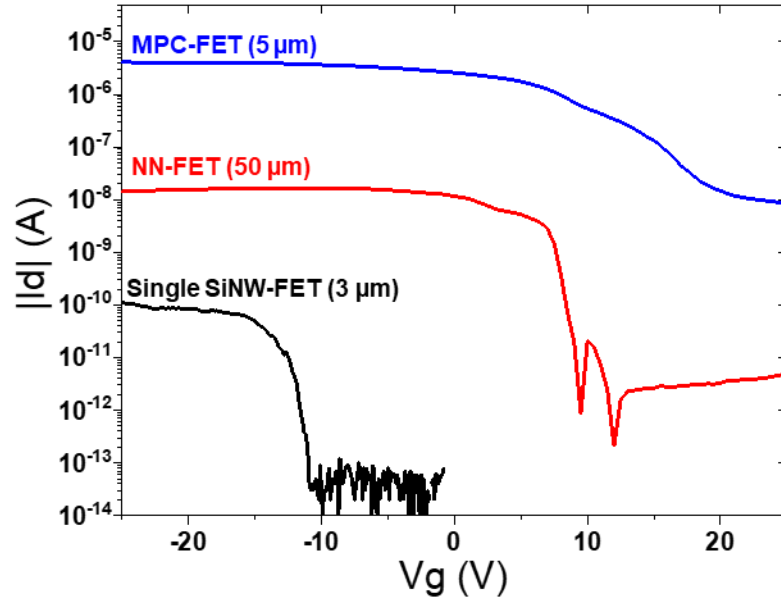
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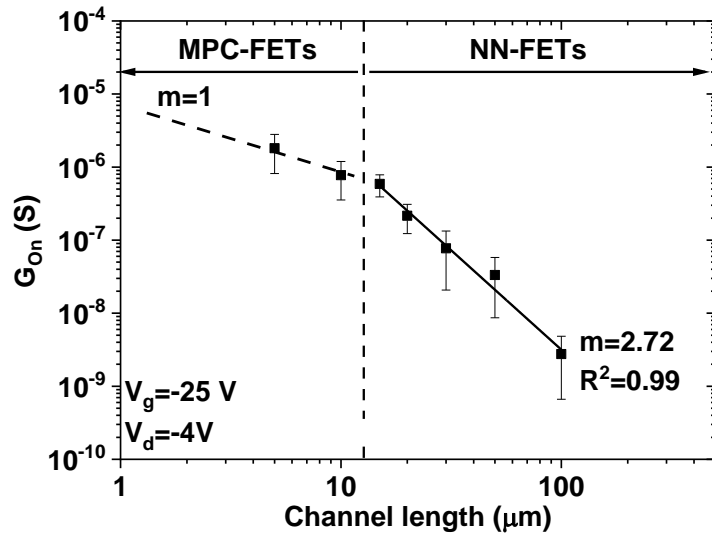
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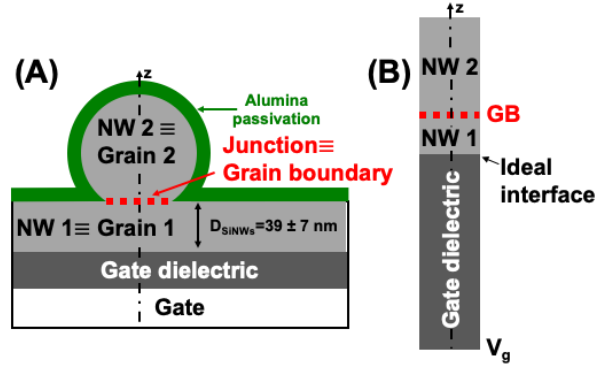
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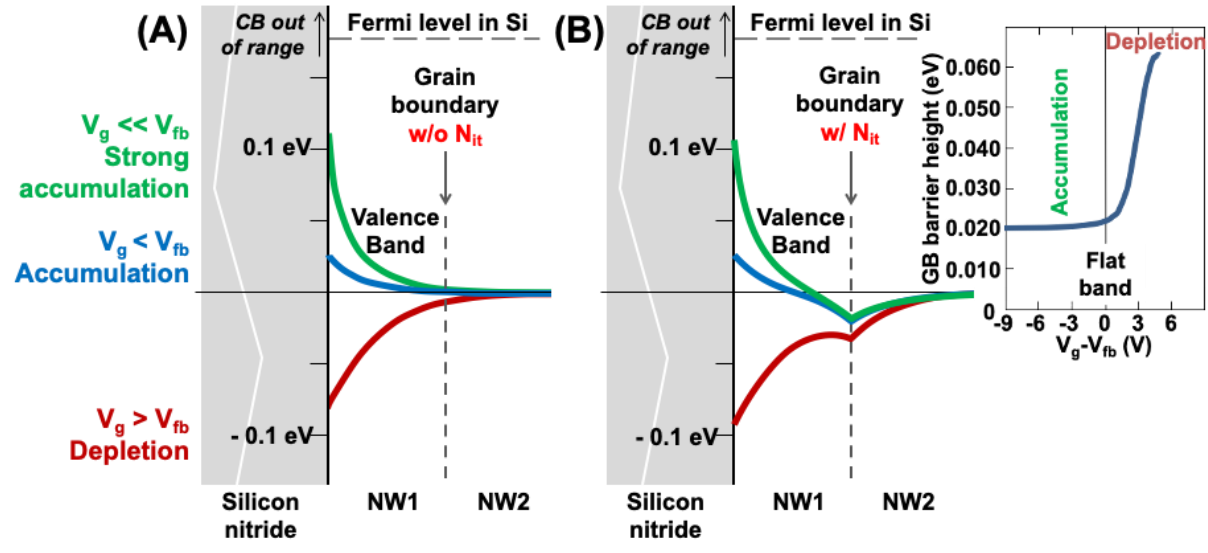
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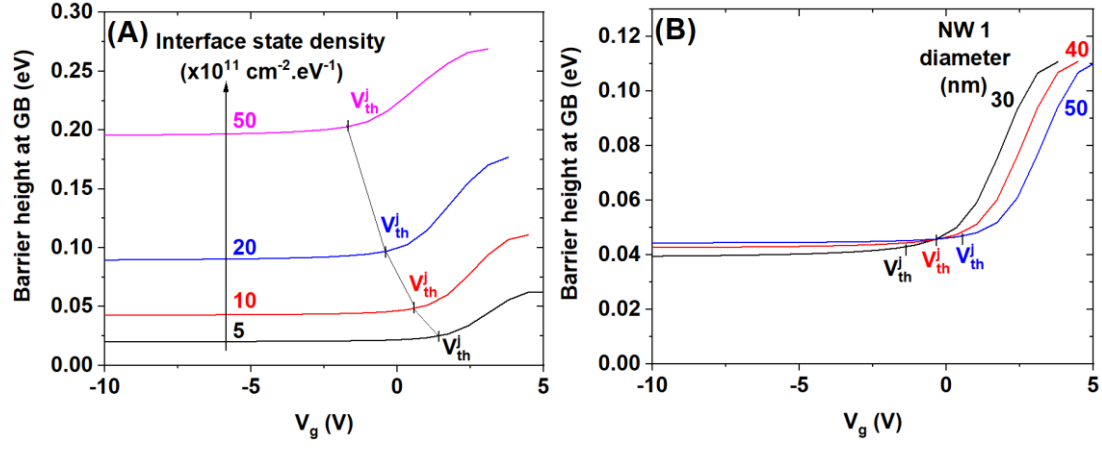
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