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High temperature operation of a monolithic bidirectional diamond switch

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Abstract

We report the 250 °C operation of a diamond-based monolithic bidirectional switch. A normally-ON double gate deep depletion MOSFET was fabricated with a 400 nm p-type channel with a boron doping of [N_A-N_D]= 2.3×10^{17} cm^{-3} and an Al_2O_3 gate oxide thickness of 50 nm. The I^{st} and IIIrd quadrants transistor characteristics are successfully measured by controlling the channel conductivity with both gates separately, with a clear ON and OFF state. A threshold voltage around 35 V is obtained with a low minimum gate leakage current of 1.00×10^{-4} mA/mm at a gate-source bias $V_{GS} = 50$ V. The bidirectional switch is then obtained by operating the MOSFET in the I^{st} quadrant of each gate setup. This first proof of concept offers a reverse conducting and reverse blocking diamond MOSFET, with only one drift region layer.

1 Introduction

The use of wide bandgap semiconductor material is of high interest for power electronics applications, which requires devices able to withstand both large current densities and large electric

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fields. Diamond meets these requirements thanks to its attractive physical properties, particularly its high breakdown field (up to more than 10 MV/cm) and superior thermal conductivity (22 W/cm.K). A focus is made on high temperature and high blocking voltage applications in which it is considered that diamond has the greatest potential[1]. In recent years diamond based power MOSFETs have been demonstrated[2]–[7], mostly relying on the surface transfer doping effect[8] (HFET) due to their relative ease of fabrication compared to the more standard MOSFET architectures (which require both p-type and n-type doping in the same device). Complementary to these structures a bulk conduction diamond MOSFET was recently introduced, the diamond deep depletion MOSFETs (D3MOSFET), to take full advantage of the diamond bulk properties[9]–[11]. Such diamond MOSFETs devices have been shown to exhibit a diode-like reverse conduction[12], but no reverse blocking capability, similar to SiC JFETs or GaN HEMTs[13], [14].

In several applications (e.g. matrix converters, multi-level converters, AC/AC converters), reverse conducting (RC) and reverse blocking (RB) power devices, also known as bidirectional power transistors, with the lowest on-state resistance are required. In this context, monolithic bidirectional power devices have been previously demonstrated[15]–[20], and we report here the first monolithic bidirectional diamond power FET (RC+RB) based on the D3MOSFET design. In the view of limiting the on-state resistance of the bidirectional diamond MOSFET, only one drift region is proposed with two isolated gates. Its high temperature operation and low specific on-state resistance is demonstrated in this article.

2 Device structure, fabrication and experimental method

The sample consists of a 400 nm boron-doped p-type layer grown by microwave plasma assisted CVD, on a 4×4 mm^2 High Pressure High Temperature (HPHT) Nitrogen-doped electrically insulating diamond substrate (fig 1). This p-layer is used for the drift region of the bidirectional P-MOSFET, since boron doping is the best option for volume conduction in diamond (activation energy of boron is 0.38 eV, doping dependent, and a hole mobility up to 2000 cm^2·V^{-1}·s^{-1}). The doping level of the p-type layer was measured to be [N_A-N_D]= $2.3 \times 10^{17} \pm 0.5 \times 10^{17}$ cm^{-3} by capacitance voltage measurements on MOS capacitors fabricated on the same sample. This was performed at temperatures ranging from room temperature to 250 °C, with an AC signal amplitude of 30 mV and a frequency carefully chosen to avoid frequency dependent effects. This

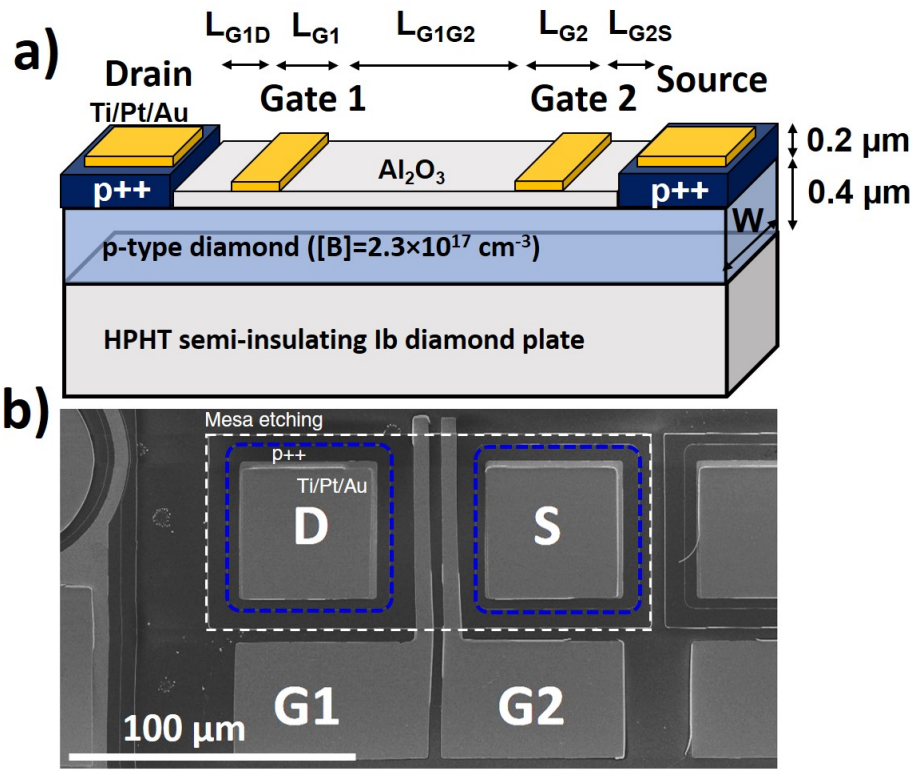

Figure 1: a) Schematic representation of the double gate lateral p-type D3MOSFET at left, the 0.2 μm selectively grown heavily boron doped layer ([B] $> 5\times10^{20}$ cm^{-3}) is deposited on top of a boron doped layer ([N_A-N_D]= 2.3×10^{17} cm^{-3}) with thickness of 0.4 μm. The metallic contacts all consist of a Titanium/Platinum/Gold (30 nm/20 nm/30 nm) stack. b) SEM top view of one of the fabricated device.

high doping range for the drift region was chosen to demonstrate a high electric field and a high current capability with diamond FETs as previously demonstrated in[12]. To lower the contact resistances, a 200 nm of highly boron-doped ([B]$> 4\times10^{20}$ cm^{-3}) diamond is selectively grown at the source and drain contacts. A Titanium/Platinum/Gold (30 nm/20 nm/30 nm) stack is then deposited by electron beam evaporation and annealed for 30 min at 500 °C in high vacuum condition ($< 10^{-7}$ mBar) to form the drain and source contacts. In order to limit the gate surface required, reducing the risk of critical failure and lowering the leakage current, a mesa structure has been designed; A reactive ion etching of O_2 plasma is used to etch down to the insulating diamond substrate around devices, as depicted in fig 1a). After an UV ozone treatment to saturate the diamond surface with oxygen bonds, the 50 nm Al_2O_3 gate oxide layer was deposited following the process detailed by T. T. Pham et al. [21] to decrease the interface state density. The Savannah 100 deposition system from Cambridge NanoTech was used with a deposition temperature of 380 °C, followed by a 30 min annealing at 500 °C. Finally, the Titanium/Platinum/Gold (30 nm/20 nm/30 nm) gate metal stack is deposited by electron

beam evaporation. Elementary p-type D3MOSFETs with only one gate were also fabricated on the same diamond substrate, which showed a normally-on behavior, with a threshold voltage of +35V and a low gate leakage of 10nA/mm under a high electric field of more than 6MV/cm both in diamond and gate oxide [12] .

The measured MOSFET dimensions are $L_{G1D} = 4$ μm, $L_{G1} = L_{G2} = 2$ μm, $L_{G1G2} = L_{G2S} = 5$ μm and a width of $W = 60$ μm. They can ideally be further reduced but were chosen towards a first proof of concept and related to lithography and fabrication limitations. Considering the measured doping level of [N_A-N_D]= 2.3×10^{17} cm^{-3}, the drift lengths should ideally not exceed 2 μm[22]. A dual channel keithley 2612 sourcemeter was used to characterize the Ist and IIIrd quadrant transistor characteristic of each setups, depicted in fig 2a) and b). To achieve a bidirectional switch, the device is always operated in the Ist quadrant of the setup A or B depending of the bias sign applied between the ohmic contacts. In setup A, the gate 2 voltage controls the channel conductivity (transistor forward bias) while the drain and gate 1 are set at the same bias. The gate to drain distance is then L_{G1G2}+L_{G1}+L_{G1D} and the depleted region below the gate 1 remains small as the drain to gate 1 potential difference is small. The setup B simply corresponds to the symmetrical case (transistor reverse bias). In this study, the switch between the two setups is performed manually to avoid the need of an external gate driver, the quasi-static bidirectional switch device characteristic is then reconstructed from both setups characteristics.

3 Results and discussion

Both setups transistor characteristics at 250 °C are shown in fig. 2d) and e). The on and off state are obtained in the Ist quadrant for a negative drain-source bias $V_{DS} < 0$ V (p-type MOSFET). The IIIrd quadrant characteristic has been successfully measured with the two gate setup, exhibiting the distinctive reopening of the channel in a diode-like behaviour. The bidirectional switch characteristic is shown in fig. 2f), obtained with the Ist quadrant of each setups.

The minimum 250 °C on-state resistance is measured at 159 mΩ.cm^2 and 152 mΩ.cm^2 in setup A and B respectively, in the same order of magnitude than reported values on H-terminated MOSFETs, with a threshold of around 35 V (fig. 2c)). The on-state resistance is partially limited by the well known presence of a Fermi level pinning, at the oxygen-terminated diamond and oxide

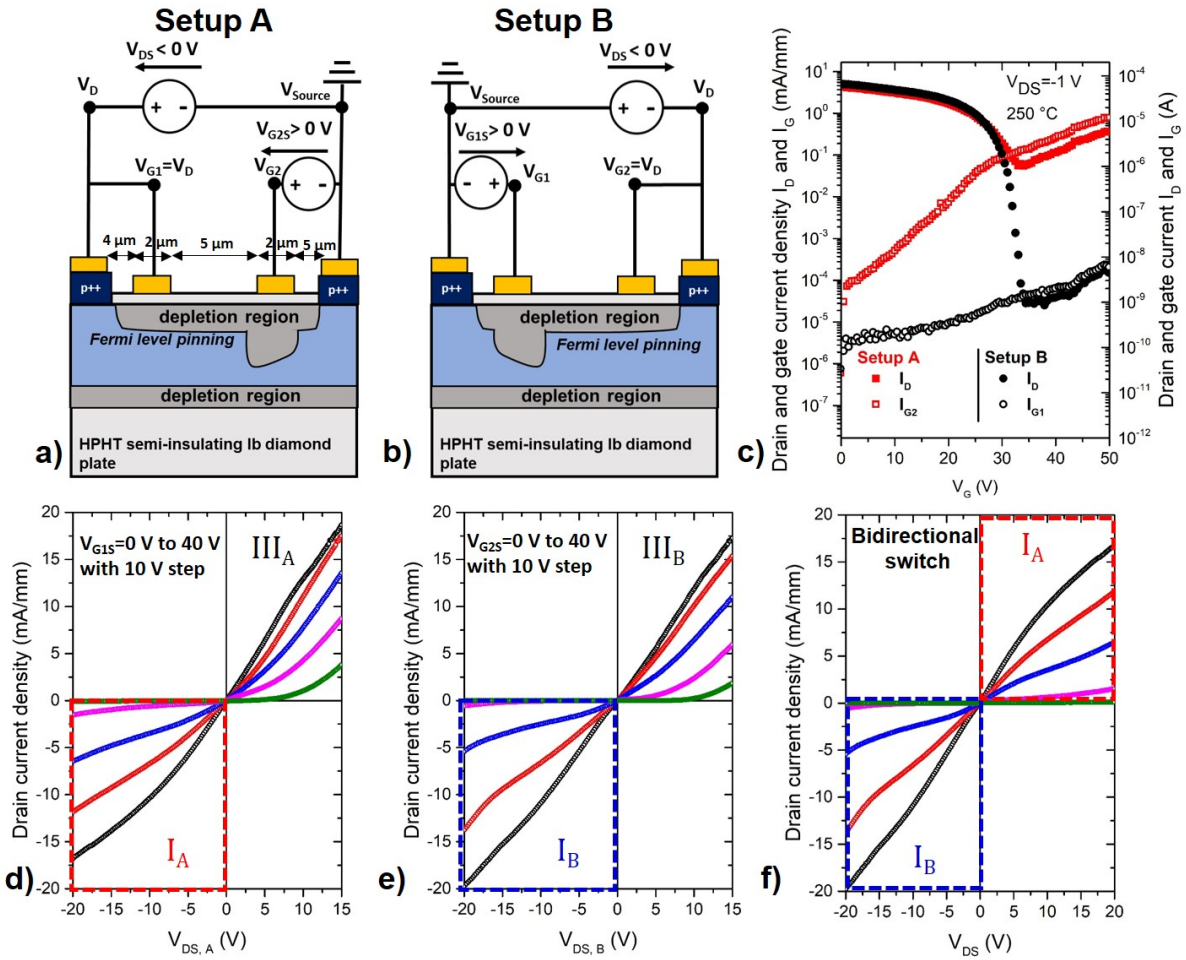

Figure 2: Schematic representation of the double gate lateral D3MOSFET in a) the setup A and b) the setup B. When one of the gate is controlled, the other one is shorted with the closest ohmic contact. Because the experimental set-up is limited to 4 probes, the substrate is left floating. c) Measured transfer characteristics of setup A (red) and B (black), both the drain current I_D and gate leakage current I_G are plotted in full and open symbols respectively. d) Measured transistor characteristic at 250 °C in the setup A and e) the setup B. f) The I^{st} quadrant of both setups are then use to reconstruct the transistor characteristic of the bidirectional double gate lateral D3MOSFET.

interface[9], [21], [23], [24], accounting for an uncontrolled depleted layer at the diamond/oxide interface. This is also complemented by the probable existence of a depletion layer at the nitrogen-doped diamond substrate and the boron-doped layer. Both of these effects reduce the effective conductive channel thickness. Moreover as stated already, the device's drift and channel length are oversized due to fabrication limitations, resulting in a larger on-state resistance.

Leakage current, shown in fig. 2c), was found to be greatly varying from one gate to the other by orders of magnitude. In the case presented here, at 250 °C gate 1 and gate 2 exhibit at a gate-source voltage $V_{GS} = 50$ V a leakage current of $I_G1 = 0.217$ mA/mm and $I_G2 = 1.00 \times 10^{-4}$

mA/mm respectively. At least one of the gates in all the measured transistors exhibited a large leakage current. This prevented us from probing the off-state blocking capabilities of the device, a moderately high drain bias ($|V_{DS}| > 50$ V) invariably caused the presence of a large gate current in the same order of magnitude than the on state drain current, eventually leading to a non-reversible breaking of the oxide. The leakage mechanism has previously been reported to be traps to traps hopping in bulk oxide with interface/valence band recombination[24]. Applying a large gate bias, causing the presence of a large electric field in the oxide, may promote the bulk oxide trap formation, reducing the energy barrier between hopping sites as their average distance reduces. Controlling this trap density to a sufficiently low value even after several measurement cycles is of great importance to achieve a reliable high breakdown device. This could be achieved (i) by using a field plate architecture, reducing the well known electric field crowding effect, especially detrimental in 2D lateral devices. And (ii) by achieving a better control of the lithography and lift-off process, to reduce the roughness at the gate metal edge that is causing large local electric field crowding effects[25]. MOSFETs with a corbino geometry have been tried to avoid the presence of corners. But the lift-off process was found to be more challenging and no devices could be obtained. Given that diamond MOSFET devices are yet not optimized, the breakdown is usually not limited by intrinsic diamond properties, but rather by imperfections of the process, the oxide layer or in the diamond crystalline structure. In a single gate design with very similar sample characteristics, it has been shown that a blocking voltage of 200 V [9] and a critical field greater than 5.4 MV/cm [12] can be achieved. This is about twice larger than the critical field of SiC or GaN devices, without the use of electric field relaxation features to improve the breakdown. Optimized diamond devices could significantly improve the high power switch devices.

4 Perspectives

The fig. 3 shows the calculated 1D lateral static performances of a lateral bulk conduction diamond device with and without a recess gates design, in comparison to the measured device and reported values of bidirectional GaN HEMTs, bidirectional vertical 4H-SiC MOSFET and IGBT. A doping level dependant ideal breakdown and hole mobility with no compensation are assumed. The gate lengths and gate to source lengths are fixed at 1 μm. Thanks to its higher critical field, it is expected that diamond could reach higher breakdown voltages than GaN

HEMT devices, in the order of a few kV, with low R_{ON}, either with a bulk or surface conduction. Lateral diamond devices could achieve similar performances than bidirectional vertical 4H-SiC devices at large blocking voltages, especially at high temperature. This is particularly valuable given the complex fabrication process of vertical bidirectional devices. Further reduction of the on state resistance could be achieved by operating in enhancement mode, either by accumulating holes at the MOS interface with a negative gate bias (p-type) or at zero gate bias thanks to the surface transfer doping effect. Similarly to what had been demonstrated with GaN and 4H-SiC, comparatively to the use of 2 devices, bidirectional switches offers a lower R_{ON}, a smaller device area, no additional voltage drop in any operating quadrant (i.e. no diode-like voltage drop), smaller commutation loops thanks to monolithic integration and an optimal packaging with all power and driving electrodes on one side, and a thermal interface at the backside (for a lateral design).

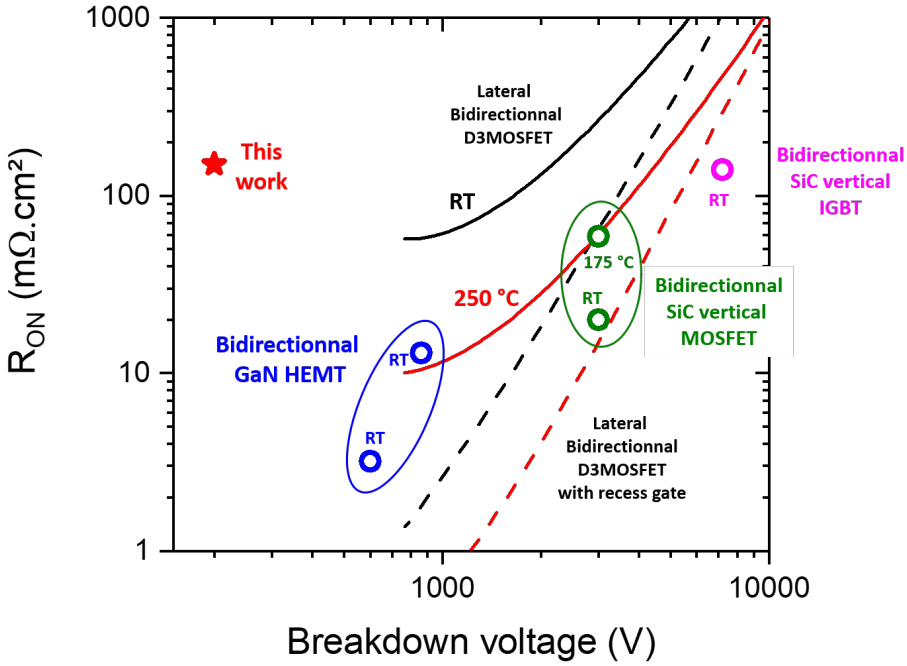

Figure 3: Measured R_{ON} as function of breakdown voltage of the fabricated diamond MOSFET and other reported wide band gap bidirectional devices from [15]–[17], [19]. The lines represent the calculated ideal characteristics at RT and 250 °C of the bidirectional lateral D3MOSFET device with gate lengths and gate to source lengths of 1 μm and optimized drift lengths. The dashed lines correspond to a more optimized recess gate design.

5 Conclusion

High temperature operation of a diamond-based monolithic bidirectional power switch based on a double gate diamond deep depletion MOSFET is demonstrated in this work. The low resistivity of diamond at high temperature allows to reach a current density of 20 mA/mm at $V_{DS} = -20$ V, despite the design being oversized on purpose to facilitate its fabrication. The high leakage current that may occur in one or both of the gates made impossible to measure the off state blocking voltage, but single gate breakdown measurements were previously reported with a blocking voltage up to -200 V and a critical field of at least 5.4 MV/cm. Lateral diamond bidirectional devices could be an attractive solution for high breakdown (> 1kV) and high temperature applications.

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