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Silicon Test Structures Design for Sub-THz and THz Measurements

Marco Cabbia, *Student Member, IEEE*, Chandan Yadav, *Member, IEEE*, Marina Deng, *Member, IEEE*, Sébastien Fregonese, Magali De Matos and Thomas Zimmer, *Senior Member, IEEE*

Abstract—In this paper, we present on-wafer TRL-calibrated measurements of silicon test structures fabricated using STMicroelectronics' B55 technology up to 500 GHz. The structures are fabricated in two subsequent runs and the respective structure in each run has a different design. The improvements in the test structures layout design are presented on the terminal capacitances of “open-M1”, which is an important test structure for the de-embedding of the transistor accesses. The improvements are examined using HFSS electromagnetic (EM) simulations, including the RF probe models and the neighboring structures.

Index Terms—TRL Calibration; Characterization; EM Simulation; HFSS; THz; Test Structures.

I. INTRODUCTION

IN order to provide cost-effective and compact terahertz (THz) and sub-THz electronic systems for various applications in the millimeter wave and sub-millimeter wave ranges, integrated circuits (ICs) based on silicon-germanium heterojunction bipolar transistor (SiGe HBTs) are gaining much attention for their compelling compatibility with silicon very large scale integration (VLSI) technologies. The advances in silicon process technology and improved figures of merit of SiGe HBTs (f_T/f_{max} of 505/720 GHz, respectively) [1] outperform CMOS transistors, offering higher power densities and better analog performance, and promise to make this technology a viable option for ultra-high-speed wireless communications, satellites, industrial sensors, automotive radars, person scanning for security, medical imaging, etc. [2]–[6].

To ensure a successful design of a high frequency electronic circuit, it is crucial to provide an accurate compact model description of the active (i.e. HBTs) and passive elements (capacitances, inductances, resistances, etc.) based on experimental data. At frequencies beyond 110 GHz, that is a particularly troublesome requirement to satisfy due to the parasitic electrical contributions of the measurement set-up and external environment. For this reason, current researches focus on calibration and de-embedding techniques to obtain accurate measurements to extract correct model parameters [7]–[9].

The calibration algorithms such as TRL, mTRL, LRM, LRRM, SOLT, etc. are usually followed by a de-embedding step, which should be accurate and not introduce additional errors [10]–[12]. For practical reasons, calibrations on Impedance Standard Substrate (ISS) combined with open-short de-embedding are commonly used in industry, even though they lack of accuracy at higher frequencies [13]. For

frequencies above 110 GHz, it has been shown that on-wafer calibration is the main method of choice compared to conventional off-wafer calibration [7], [14]. For this reason, on-wafer TRL (Thru-Reflect-Line) calibration has been chosen for this work: it is well suited to measurements at sub-millimeter wavelengths generated by probes with small pitch, since it relies on transmission lines rather than lumped elements, which cannot be considered as non-distributed elements at such high frequencies [15].

A limitation for the use of TRL is that, in real-world applications, the structures are positioned in a wafer side by side, with small spacing between each element, in order to save space. The effect of the coupling due to the adjacent structures on the measurements of the device-under-test (DUT) is therefore non-negligible [16]–[19], and may result in some artifacts such as resonances (dips and oscillations) in the calibrated S-parameters of the DUT. Thus, it is crucial to reduce the impact of such coupling as well as the probe-to-probe crosstalk and the coupling between probes and the back-end-of-line (BEOL) environment, eventually providing a reliable guide to test structure layout designers.

In the following sections, we will first present a discussion about the technology used to fabricate the test structures of the two separate runs, a description of the layout design of each run including the differences between them, and the methodology to validate the measurements through EM simulation models in detail. Next, the topic will focus on a comparison between the measurements and the EM simulation results of the capacitances of a relevant test structure, open-M1. To provide a better insight on the different behaviors of the two fabrication runs, the layout design used in a previous run will be suitably modified to reflect the design of the newest run, and will be simulated with and without neighboring structures. The electric field contours of both designs will be shown to observe the physical phenomena taking place in different layout configurations.

II. STRUCTURES AND METHODOLOGY

A. On-Wafer Calibration Standards

For the on-wafer TRL calibration, the test structures and HBTs have been designed [20] and fabricated with STMicroelectronics BiCMOS 55-nm (B55) technology [21]. All the structures lay on a silicon substrate and consist of 8 metal layers (M1-M8) and corresponding vias in the BEOL (Fig. 1). On top of M8, which is used for the microstrip line design, aluminum ground-signal-ground (G-S-G) contact pads are realized. In addition to the on-wafer TRL calibration

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Fig. 1. Cross-sectional side view of a transmission line of fabricated on-wafer TRL calibration kit where dielectric constants levels used in simulation are shown (Run-2). The G-S-G RF pad configuration at M8 is shown in orange, with signal trace in the center. The ground plane is at M1.

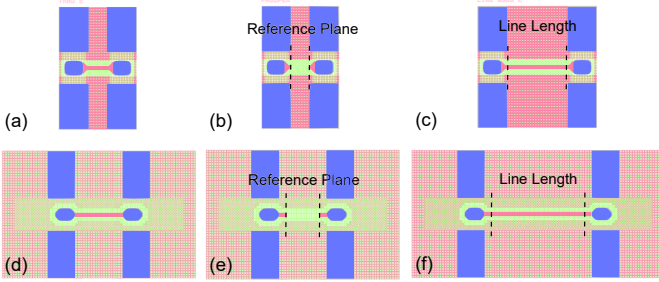


Fig. 2. Top view of the on-wafer TRL calibration test structures. Run-1&2, respectively: (a),(d) thru, (b),(e) pad-open, (c),(f) line 500 GHz. In pad-open, post-calibration reference planes are shown with black dashed line.

kit described in [20] (labelled “Run-1” from now on), a new mask with the same layer sequence but a different layer layout has also been designed and fabricated (labelled “Run-2”). The on-wafer TRL calibration standards ‘thru’, ‘reflect’ and ‘lines’ of Run-1 and 2 are shown in panels (a)-(f) of Fig. 2, respectively. In both runs, two lines are used in the on-wafer TRL calibration up to 500 GHz where the longer line is named ‘line 110 GHz’ and shorter line is named ‘line 500 GHz’, with a range of validity from 20 GHz to 500 GHz. The dimensions of each line and thru for both runs are listed in Table I. In the on-wafer TRL calibration for each run, ‘line 110 GHz’ is used up to 110 GHz while ‘line 500 GHz’ is used in the 140-500 GHz range. For the reflect standard, a structure called ‘pad-open’ acts as an open circuit at the RF pads’ plane, thus providing high reflection for the incident waves. Moreover, to perform an impedance correction, one extra ‘pad-load’ structure consisting of two loads at port-1 and port-2, including pads and M8 access line, is considered. After performing the on-wafer TRL calibration, the reference plane is set after the RF pads at the edge of the access line, as shown in Fig. 2(b) and Fig. 2(e) on the pad-open. In addition to the on-wafer TRL calibration kit structures, two test structures are dedicated to the de-embedding of the transistor accesses. These two test structures are called open-M1 and short-M1 and, as their names suggest, they provide an open/short circuit at the contact plane at M1, with the same access design as the transistor. They are representative because of their elaborate BEOL and importance in the transistor measurements, thus the former is chosen as our DUT (Fig. 3-4).

B. Differences Between Run-1 & Run-2

Giving more insight on the masks, we can list the following differences:

- Run-1 presents a 10- μm -thick silicon dioxide (SiO_2) “ring” extending from the silicon substrate to the top

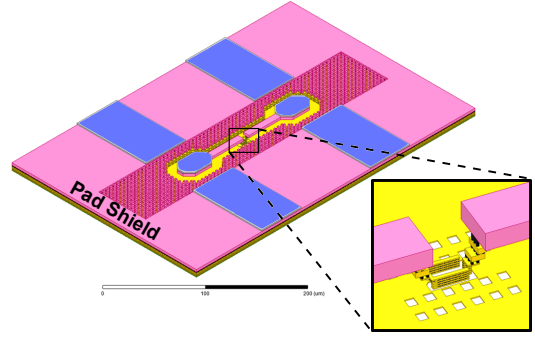


Fig. 3. Open-M1 3D model (Run-2) for transistor de-embedding. From access lines in M8 (pink), metals (yellow) alternate with vias (black) down to M1, where an open circuit is located (see detail). The “pad shield” is located at the back of the RF pads and pointed out explicitly. The shades in a darker tone of pink are small cubic “dummy” structures, that have been added to respect the density rules.

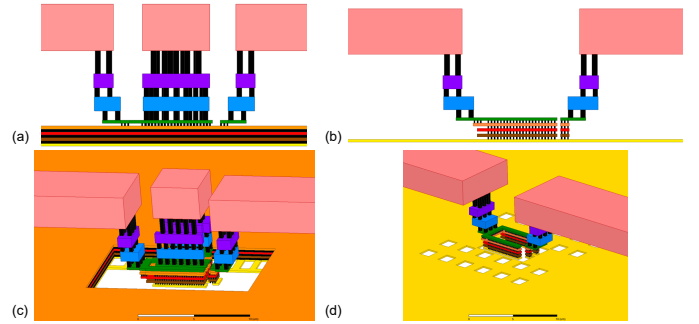


Fig. 4. Open-M1 structure for transistor de-embedding. Cross section details from Run-1 (a) and Run-2 (b) show metal layers from M1 (yellow) to M8 (pink) in color, while vias are in black. Ground plane is up to M4 (Run-1) or M1 (Run-2). Dimetric 3D details from Run-1 (c) and Run-2 (d) are also shown. At M1 a space between port-1 and 2 contacts provides an open circuit. In Run-1, the M8 cubic connection bridges the emitter contact (not visible due to perspective) to the M1-M4 ground plane.

of M8 and surrounding all the test structures for an electrical isolation [20]: this element was needed to make Run-1 compliant to process design rules, while maintaining a proper distance between structures. In [22], it is indicated as a “rule of thumb” to avoid the use of slots in microstrip grounds for calibration structures, since they may generate excess coupling between structures. However, this recommendation has not been studied in detail by simulation with probe models, as it will be done in the following. Moreover, oftentimes this advice does not seem to be taken in the industrial environment;

- in Run-1, the ground plane extends from M1 to M4, while in Run-2, the ground is provided by M1 only (Fig. 4);
- the microstrip line realized on the top metal layer (M8) is 5.8/7.7 μm thick in Run-1/Run-2, and its distance to

TABLE I. Dimensions of thru and lines in each run.

Test Structure Name	Run-1	Run-2
Thru	35 μm	65 μm
Line 110 GHz	365 μm	595 μm
Line 500 GHz	115 μm	185 μm

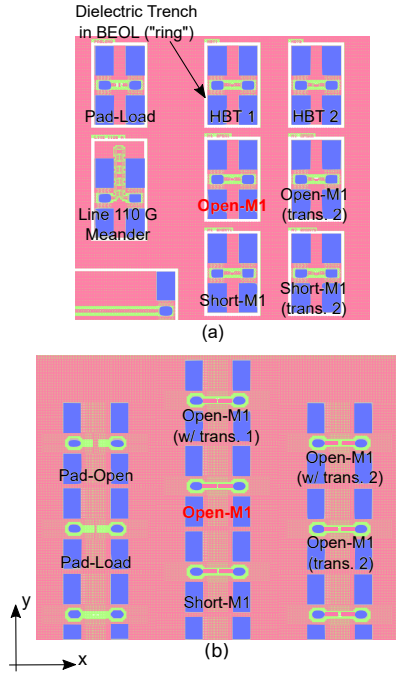


Fig. 5. Top layout view of the open-M1 (DUT: name in red) surrounded by its neighbors in Run-1 (a) and Run-2 (b). The same test structures of the central column are repeated at the right for another transistor (with different emitter size).

the ground plane is $4.9/5.6 \mu\text{m}$;

- the RF pads are designed to have compatibility for either 50- or $100\text{-}\mu\text{m}$ pitch probes. The associated access lines after the RF signal pads are $4/15 \mu\text{m}$, for Run-1 and Run-2, respectively. The signal pads are 14% longer in Run-2 than Run-1, but 7% narrower and the signal-ground pad gaps are respectively $16/20 \mu\text{m}$. The edge-to-edge distance between the closest signal pads of two adjacent structures is $120/210 \mu\text{m}$ in the x direction and $248/245 \mu\text{m}$ in the y direction. Also, the edge-to-edge distance between the closest ground pads of two adjacent structures is $172/180 \mu\text{m}$ in the x direction and $45/15 \mu\text{m}$ in the y direction. The RF pads have surface areas of $35 \times 27 \mu\text{m}^2$ and $40 \times 25 \mu\text{m}^2$;
- the characteristic impedance is corrected to approximately 50Ω in both designs.

Two important additions on the Run-2 layout (see Fig. 3):

- 1) a particular shielding behind the signal pads [23], [24];
- 2) a M1-to-M8 ground volume that connects all the ground pads together and is seen at M8 as a boundless plane.

We call this novel layout “continuous ground plane” to stress on its ubiquity among the structures on the die, its intent being to reduce the probe-to-substrate EM coupling and coupling with neighbors. In Fig. 5, we show a top view of a portion of the wafer where the test structures layout is visible. In this picture, the open-M1 structures for Run-1 (Fig. 5(a)) and Run-2 (Fig. 5(b)) are surrounded by their respective neighbors (the “oxide ring” is visible in white in Fig. 5(a)). For Run-1, the structures are aligned in columns and rows. Structures in Run-2 are placed differently: a particular design in staggered rows is used in order to reduce EM coupling between the RF probes and the adjacent structures.

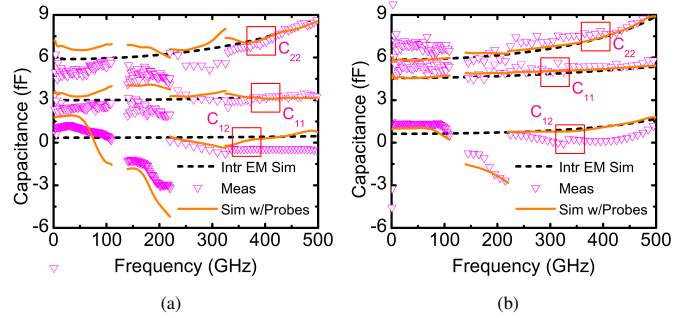


Fig. 6. All the capacitances measurement, intrinsic HFSS and complete structure simulations of the open-M1 for both Run-1 and 2. These capacitances are related to port-1 (C_{11}), port-2 (C_{22}), and the coupling capacitance between the port-1 and port-2 (C_{12}).

C. EM Simulation Procedure

Calibration methods and de-embedding techniques are indispensable tools to remove the parasitic contributions from measurement data; nevertheless, the associated error models only approximately represent the true environment. Consequently, electromagnetic (EM) simulations are carried out in Ansoft’s High-Frequency Structure Simulator (HFSS) as part of the analysis of layouts and measurement verification. After creation of the 3D models of each structure, simulation is carried out much like described in [24]. Thanks to the optical microscope imaging, several G-S-G probe models replicating the GGB@Picoprobe RF probes with a $50/100 \mu\text{m}$ pitch for each band up to 500 GHz have been designed in HFSS [25].

D. Measurement Setup

Four sets of measurements have been carried out to cover the whole spectrum up to 500 GHz. In the 1-110 GHz frequency range, measurements are performed with an Agilent E8361A Vector Network Analyzer (VNA), with an extender (N5260-60003) in the 67-110 GHz range; 140-220 GHz, 220-325 GHz and 330-500 GHz measurements were performed with a ZVA24 VNA from Rhode & Schwartz with Rhode & Schwartz extenders (ZC220, ZC330, and ZC500, respectively). The RF probes used in measurement are from Picoprobe, with $50 \mu\text{m}$ pitch, except for Run-2 in 1-110 GHz band measurements where Picoprobe probes with $100 \mu\text{m}$ pitch are used. The on-wafer TRL calibration is performed using raw measurement data of the DUT, open-M1, provided by the VNA, where the TRL calibration with impedance correction has been applied [26], [27], setting the reference plane at the end of the small access lines after the pad (see in Fig. 2(b)).

III. RESULTS AND DISCUSSION

A. Open-M1 up to 500 GHz – Run-1 vs. Run-2

In Fig. 6, all the capacitances of open-M1 are shown for both Run-1 and 2: they are related to port-1 (C_{11}), port-2 (C_{22}), and the coupling capacitance between the port-1 & 2 (C_{12}). The measurements are very well replicated by simulation. It is worth noticing that particularly at very high frequency, the measurements and the corresponding simulations with probes follow the intrinsic simulation, thus confirming the

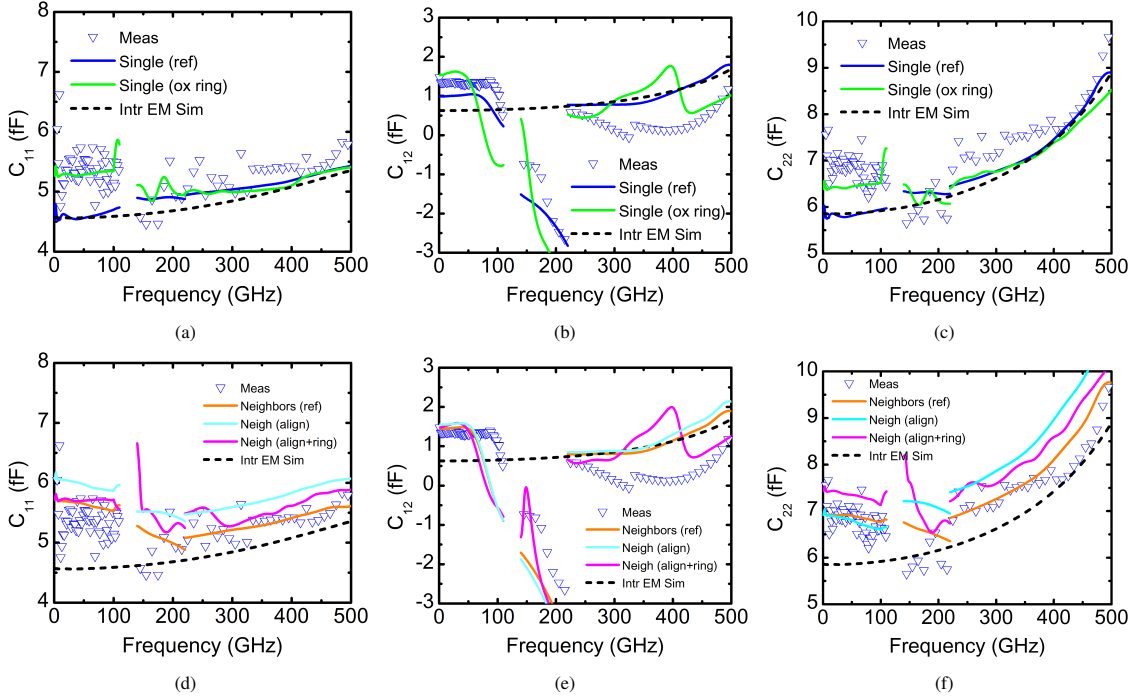


Fig. 7. Run-2 measurement vs. simulation. Single structure with and without SiO₂ ring (from (a) to (c)), DUT with neighbors (adjacent structures) in the actual “staggered row” configuration, with aligned neighbors, and in a “pseudo Run-1” configuration (aligned structures with a 10 μm SiO₂ ring around them).

efficiency of the on-wafer TRL calibration. Overall, the Run-2 measurements appear to be more consistent and have very good band-to-band continuity; the lower capacitance at port-1, which is, for that matter, predicted by the intrinsic simulation, is due to the smaller metallic M1 layer surface and the higher distance between the base metal contact and ground. In the 140-220 GHz band, though, both the measurement and the simulation with probes diverge from the trend indicated by the intrinsic simulation, particularly the port-to-port capacitance (C_{12}), which becomes clearly nonphysical. This fact may be traced back to the port-1 to port-2 crosstalk between the two RF probes due to their design [28]. It has been showed that a coplanar probe with a much simpler design does not present this behavior in this band [24]. We can also clearly see that values of open-M1 turn out to be generally positive for Run-2 (except in the 140-220 GHz range), while Run-1 measured values become negative from 240 GHz on. This more physical behavior with respect to Run-1 can be attributed to a different configuration of each of the BEOL layers and the continuous ground plane, which provides a different environment around the DUT, more distance from the neighboring structures and less coupling through the pad shield.

B. EM Simulation – Run-2 vs. Altered Run-2

To further investigate the influence of the DUT environment, we consider altered versions of the reference Run-2 layout. By this, we mean to alter the Run-2 design to match the default Run-1 design by introducing spot modifications in order to eventually understand and compare the layout impact. Any direct comparison, though, would be pointless, since the layout of each layer of the BEOL has deeply changed from Run-1 to 2. We study the capacitances of the following configurations:

- “Single”: In Fig. 7(a)-7(c), all the structures (DUT and calibration standard ‘thru’, ‘pad-open’ and ‘line 110/500 GHz’) have first been simulated as isolated structures laying on planes emulating infinite dielectric layers and ground. The DUT, open-M1, is subsequently calibrated with the corresponding isolated calibration standards. We consider two different configurations:
 - “Ref”: the reference, where each Run-2 isolated structures are modelled;
 - “Ox ring”: the altered version, where a 10-μm SiO₂ ring surrounds each isolated structure, much like in Run-1, and the pad shield is removed.
- “Neighbors” (for short, “Neigh”): In Fig. 7(d)-7(f), all the structures have been simulated with their actual corresponding adjacent structures (just the closest neighbors are taken into account, as the electromagnetic impact of more distant structures on the DUT would be negligible), and capacitances of open-M1 are shown. The pad-to-pad distance between each DUT and its neighbors is brought to the same as Run-1 (45 μm). Two different configurations are considered for these plots too:
 - “Ref”: the reference, where every Run-2 structure is not surrounded by any ideal infinite plane of dielectric and metal, but by its actual neighbors, in their actual position, as they are on the wafer;
 - “Align” and “Align+ring”: the altered version, where the neighbors are also present but are aligned in columns and rows. For simplicity, the common chosen neighbor is only one: pad-open, since this structure has proved to be more prone to EM coupling, thus representing a “worst case” situation. In “Align+ring”, the oxide ring is added, like in Run-1: therefore, this

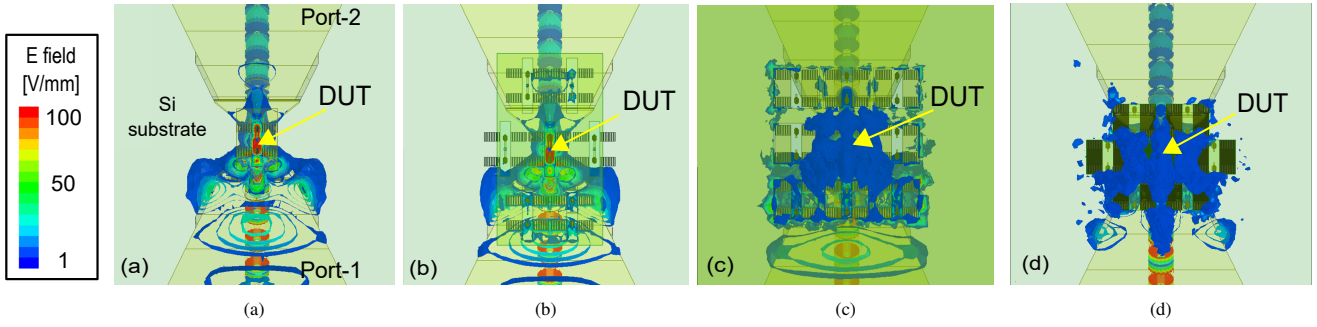


Fig. 8. HFSS-simulated electric field contour (back view) for DUT transistor-open at 500 GHz: single structure (a), neighbors (b), aligned neighbors with oxide ring (c), and neighbors in a more dense configuration (no continuous ground plane) (d).

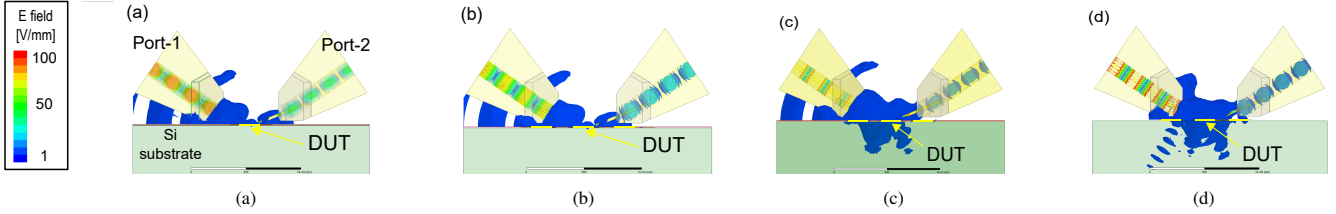


Fig. 9. HFSS-simulated electric field contour (side view) for DUT transistor-open at 500 GHz: single structure (a), neighbors (b), aligned neighbors with oxide ring (c), and neighbors in a more dense configuration (no continuous ground plane) (d).

represents a “pseudo Run-1” case.

From Fig. 7(a)-7(c), the effect of the oxide ring is visible. Overall, the curves show small fluctuations around the reference (mostly on C_{12}), and larger deviation from the intrinsic curves at low frequency. In Fig. 7(d)-7(f), the contribution of neighbors is also considered. As we can see, the curves representing the reference case with neighbors, the orange curves in Fig. 7(d)-7(f), keep close to measurements, as expected, but the curves in the case with no neighbors (blue curves in Fig. 7(a)-7(c)), do not deviate considerably: in fact, they differ less than 1 fF all over the spectrum, except in the 1 – 110 GHz band, where deviation slightly exceeds this value. This important result yields to the conclusion that by the optimized design of Run-2, the impact of the neighbors is considerably reduced. Also, this fact makes us confident on the use of “single” structures instead of models with adjacent structures around them for EM simulations, which greatly reduces simulation time and complexity. The alteration of the neighboring environment specified in Fig. 7(d)-7(f) by the light blue and pink curves also provides some interesting insights. If we first consider the case where the structures have just been aligned (“align”), capacitances C_{11} and C_{22} keep above the reference configuration (“ref”) in all the considered frequency spectrum; the coupling is reduced thanks to the pad shielding and the staggered configuration. Note that, on the other hand, C_{12} is only very moderately affected. The addition of the oxide ring (“align+ring”) disturbs the trends of the port capacitances generating a small ripple, but more strongly the trend of C_{12} , which is similar in shape to C_{12} in the case of a single structure with oxide ring (Fig. 7(a)-7(c)). Therefore, on C_{12} the effect of the alignment is negligible compared to the one produced by the oxide ring while, on the contrary, closer and aligned neighbors affect more the capacitances between the ports and the substrate, with an additional capacitance adding up to the one which is already present (offset on C_{11} and C_{22}).

We observe now the electric field 3D contour obtained by HFSS. In the backside view of the DUT and its neighbors (Fig. 8), we see the E-field concentrating on the DUT and beneath the probe corresponding to port-1, where the field is excited, and the most intense E-field is efficiently confined inside the space created by the pad shield. The field contour has the same shape either with or without the presence of adjacent structures (Fig. 8(a), 8(b)). When the dielectric ring is present (Fig. 8(c)), the E-field is heavily affected. The intensity of the field increases around the DUT and below the excitation probe and we can clearly see the field densifying around every adjacent structure. In Fig. 9, the penetration inside the silicon substrate is well depicted. Where no oxide ring is present (Fig. 9(a) and Fig. 9(b)), the E-field is only slightly visible in the substrate region below the DUT. Also, no difference can be noticed in the field shape when the neighbors are considered, thanks to the continuous ground plane. On the other hand, when aligned neighbors are in place (Fig. 9(c)), the field is free to couple below the DUT with all the neighbors through the rings.

Fig. 8(d), 9(d) introduce yet another configuration. This aims to represent a more dense layout design approach of test structures: the neighbors in this case are in staggered row but no continuous ground plane is present. In fact, no metal volume is connecting the structures, which are only surrounded by the dielectric. Also, their mutual distance is even more reduced, in order to create the most compact design: the area occupancy is reduced of a quarter. The electric field in Fig. 8(d) consequently scatters and permeates all the neighboring structures more intensely than in Fig. 9(c). Fig. 9(d), on the other hand, shows that the probe-to-substrate coupling is reduced (since no metal is under the probe), but the field uncontrollably propagates through the lossy silicon substrate; however, while the coupling can be removed by calibration, the dispersion of the field in the substrate is harder

to correct, making it more prone to measurement errors.

IV. CONCLUSION

In this work, we presented S-parameters measurements of a test structure creating an open circuit at M1 up to 500 GHz fabricated in two separate runs using the STMicroelectronics' B55 technology. The comprehensive EM simulation analysis is presented to analyze the measurement data behavior. The impact of the layout design improvements of Run-2, the so-called continuous ground plane, is highlighted on the open-M1 characteristics through measurement and EM simulation analysis. Shielding structure, staggered row placement and removing the dielectric ring result in a more confined energy flow and avoiding all artifacts on any capacitance, as confirmed by simulation of the altered Run-2 layout. Also, the electric field contour reinforces our motivation in the use of the boundless ground plane, whereas a widespread approach leads to uncontrolled coupling with neighbors and the substrate. It is worth to point out that the presented results are valid not only for the particular case of open-M1, but for any test structure with similar layout design and neighbors displacement.

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