Strain evolution of SiGe-on-insulator obtained by the Ge-condensation technique

Victor Boureau, Shay Reboh, Daniel Benoit, Martin Hÿtch, Alain Claverie

APL Materials

Strain evolution of SiGe-on-insulator obtained by the Ge-condensation technique

Cite as: APL Mater. 7, 041120 (2019); https://doi.org/10.1063/1.5088441
Submitted: 10 January 2019 . Accepted: 03 April 2019 . Published Online: 30 April 2019

Victor Boureau, Shay Reboh, Daniel Benoit, Martin Hÿtch, and Alain Claverie

Strain evolution of SiGe-on-insulator obtained by the Ge-condensation technique

Cite as: APL Mater. 7, 041120 (2019); doi: 10.1063/1.5088441
Submitted: 10 January 2019 • Accepted: 3 April 2019 •
Published Online: 30 April 2019

Victor Boureau,[1,2] Shay Reboh,[3] Daniel Benoit,[2] Martin Hÿtch,[1] and Alain Claverie[1,a)]

AFFILIATIONS

[1]CEMES-CNRS, 29 Rue Jeanne Marvig, 31055 Toulouse, France
[2]STMicroelectronics, 850 Rue Jean Monnet, 38926 Crolles Cedex, France
[3]Université Grenoble Alpes, CEA, LETI, 38000 Grenoble, France

[a)]**Author to whom correspondence should be addressed:** alain.claverie@cemes.fr

ABSTRACT

Compressively strained SiGe-On-Insulator (SGOI) made by the Ge-condensation technique is used as a performance booster for ultrathin fully depleted silicon-on-insulator transistor technology. Here, we report on the evolution of the compressive strain in the SiGe film along the formation of local SGOI. For this, experimental maps of lattice strain with nanometer spatial resolution have been obtained by dark-field electron holography and compared to results from numerical models describing the mechanics of the structures. In particular, we report on unexpected strain evolutions when the top semiconductor layer is patterned to fabricate the shallow trench isolations that separate the Si nMOS from the SiGe pMOS areas. Dramatic and long-range relaxation of the compressive SiGe layers occurs, while no extended defects are formed in the crystal. The phenomenon involves relative horizontal displacements between the SiGe layer and the underlying Buried Oxide (BOX). We suggest that the Ge-enrichment of the layer close to this interface by the Ge-condensation technique modifies the SiGe/BOX interface and that strain relaxation results from the propagation of some interfacial defects from the edge to the center of the structure, driven by the shear stress at the interface.

The engineering of the elastic strains in the channel of Complementary Metal-Oxide-Semiconductor (CMOS) transistors is being used to boost the performance of microelectronics devices.[1] Tensile strain increases electron mobility, while compression of the lattice improves hole mobility.[2] Different strategies have been adopted to manipulate locally the mechanical strain during the fabrication of transistors, such as the introduction of lattice mismatched strained sources and drains[3] and of stressed Contact Etch Stop Layers (CESL).[4] Alternatively, prestrained semiconductor substrates have been adopted, in particular in Fully Depleted Silicon-On-Insulator (FD-SOI) technology.[5] The co-integration of Si channels for nMOS and compressively strained SiGe channels for pMOS transistors is obtained through the local transformation of the top-Si layer into SiGe via the Ge-condensation technique.[6,7] The process starts with the epitaxy of a SiGe layer on top of the Si film from the Silicon-On-Insulator (SOI) areas designated for pMOS transistors. The oxidation of this SiGe layer consumes preferentially Si atoms, while Ge atoms are injected into the Si underlayer.[8] During this process, the initial Si layer is thus progressively enriched with Ge, while the resulting oxide can be removed at the end. A particularity of this process is that, when processing full wafers, the formed SiGe crystal keeps the same in-plane lattice parameter than the original Si. Hence, this layer is found under biaxial compressive strain and defines a compressive SiGe-On-Insulator (c-SGOI) structure.[9,10]

In this work, we study the evolution of strain of initially compressive SiGe-On-Insulator layers fabricated using the Ge-condensation technique along the fabrication route leading to the formation of high mobility channels for ultrathin FD-SOI p-type devices. For this, we have combined experimental lattice strain maps obtained using a sophisticate Transmission Electron Microscopy (TEM) technique providing nanometer spatial resolution and numerical models describing the mechanics of the structures. In particular, we report on some unexpected and dramatic strain evolutions of the SiGe layer when the top semiconductor layer is patterned to fabricate the Shallow Trench Isolations (STI) needed to electrically separate the p from the nMOS transistors. Indeed, long-range elastic relaxation of the c-SGOI is observed, which involves nonelastic relative horizontal displacements along

the interface between the SiGe layer and the underlying Buried Oxide (BOX). These results are discussed and enlighten the degradation of the mechanical properties of the SiGe/BOX interface formed by the Ge-condensation technique. Finally, a phenomenological relaxation mechanism is proposed.

The investigated structures were fabricated in a state-of-the-art 300 mm technology semiconductor facility using SOI wafers with a 11 nm thick top-Si layer and a 20 nm thick BOX. Figure 1 summarizes the fabrication process of the samples, detailed as follows. The Ge-condensation process starts by masking the nMOS regions. In the foreseen pMOS regions, 8.5 nm of epitaxial $Si_{0.75}Ge_{0.25}$ is epitaxially grown by Rapid Thermal Chemical Vapor Deposition (RT-CVD). A first oxidation process is carried out by Rapid Thermal Oxidation (RTO) at 1100 °C during 45 s to obtain a 13 nm thick SiGe layer with a Ge concentration varying linearly from 27 at. % at the top to 5 at. % at the interface with the BOX.[11] Sample A (depicted in Fig. 1) is taken at this step to obtain information on the strain distribution close to the vertical interface separating the original SOI (nMOS masked area) and the SGOI (pMOS area). The wafer is then furnace annealed under oxidizing atmosphere at 800 °C for 1h30, reducing further the thickness of the SiGe film down to 9 nm. This process causes a pileup of Ge to a concentration of 50 at. % below the oxide/SiGe interface.[11,12] For the fabrication of STI, a hard mask is deposited over the whole wafer. It consists of a 50 nm thick SiN layer deposited by Low Pressure CVD (LP-CVD) at 780 °C onto an ultrathin SiO_2 layer. The intrinsic stress of the SiN layer, measured by wafer bow on dedicated Si wafers, is of 1.2 GPa.[13] The mask is then opened at the edge of the SOI/SGOI interface, in the SOI region, and shallow trenches are fabricated by dry etching and filled with SiO_2 by Subatmospheric CVD (SA-CVD). Sample B (depicted in Fig. 1) is taken at this step to measure the strains in the SiGe layer, close to the STI edge. The fabrication goes on by annealing the wafers under N_2 at 1050 °C for 30 min to densify the STI oxide. The densification is expected to generate a tensile stress of the order of 130 MPa in the oxide.[14] This thermal budget also promotes Ge diffusion and leads to the homogenization of the Ge concentration across the SiGe layer at about 22 at. %.[11] After that, the SiN mask is removed by Chemical Mechanical Planarization (CMP) followed by selective chemical etching. Sample C is taken at this step and depicted in Fig. 1.

To image and map the strains in the structures, we have used Dark-Field Electron Holography (DFEH).[15] The experiments were performed on a Hitachi HF-3300 transmission electron microscope operating at 300 kV. The equipment is specifically designed for holography,[16] equipped with a cold-field emission source, an imaging aberration corrector (CEOS B-COR[17]), a dedicated Lorentz mode position of the sample holder above the objective lens, a multiple biprism system,[18] and a 4k CCD camera. The holograms were recorded using ⟨220⟩ and ⟨004⟩ diffracted beams, 10 s exposure time, and 1.0 nm fringe spacing. Strain and rotation maps were reconstructed with a spatial resolution of 3 nm using HoloDark plugin[19] for DigitalMicrograph. All strain values are given relatively to the reference unstrained Si lattice from the substrate under the BOX. The SOI substrates we have studied show an initial miscut[20] (or tilt angle) of +0.4°. In the conventions used here, layer rotation values smaller than the miscut define clockwise rotations. The TEM specimens were prepared by Focused Ion Beam (FIB)[21] using a dual-beam FEI Helios 600i.

Numerical models describing the mechanics of the structures, using the Finite Element Method (FEM), were built on COMSOL Multiphysics software with the structural mechanics module. The elastic constants of SiGe are obtained by combining the ones of Si and Ge[22] according to Vegard's law. The SiO_2 and SiN are described as isotropic materials of Young modulus of 70 GPa and 280 GPa and Poisson coefficients of 0.17 and 0.23, respectively. Above 960 °C,[23] the SiO_2 is modeled assuming a Maxwell viscoelastic behavior.[24] The lattice parameter of SiGe is obtained using the relation $a_{SiGe}(Å) = 5.431 + 0.20x_{Ge} + 0.027x_{Ge}^2$, x_{Ge} being the atomic concentration of Ge.[25] For instance, $Si_{0.78}Ge_{0.22}$ has a lattice difference of 0.83% relatively to relaxed Si. Hence, in our convention, a fully relaxed $Si_{0.78}Ge_{0.22}$ is characterized by a strain value of +0.83% and

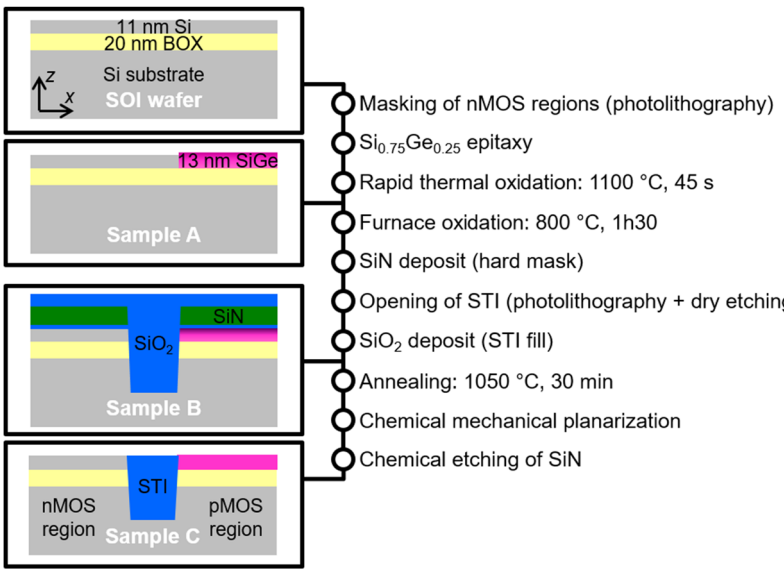

FIG. 1. Flow chart summarizing the fabrication of the samples. The schematic of each sample is detailed.

a fully (compressively) strained SiGe is characterized by an in-plane strain ε_{xx} = 0%, i.e., when its in-plane lattice parameter is the same as the one associated with the relaxed Si reference. Samples to be observed by TEM are thinned by FIB down to about 90 nm. Thus, they suffer some elastic relaxation close to the two free surfaces. FEM is used to calculate the strain of the sample using 2D models in two extreme cases, assuming either a fully relaxed infinitely thin lamella ("plane stress" approximation, σ_{iy} = 0 GPa with i = x, y, z; y being the thinning direction and z being the normal to the wafer surface) or a bulk sample ("plane strain" approximation, ε_{iy} = 0 with i = x, y, z).[26] Strain values obtained from these two models never differ by more than 0.03%, i.e., below the precision of the DFEH measurement. For this reason, experimental DFEH mappings well reproduce the actual strain fields which reside in the structure before thinning. The sequence of fabrication steps is implemented by using the results of a model step as inputs for the subsequent one.

In Fig. 2, we display the results we have obtained on sample A, i.e., after the Ge-condensation process, in the region where the Si and SiGe layers coexist and intersect.

Figures 2(a) and 2(d) show the experimental mappings of the in-plane component of strain ε_{xx} and of the lattice rotation R_{xz} obtained by DFEH. Figures 2(b) and 2(e) show the mappings obtained with the model. Strain and rotation profiles from left to right along the layers can be extracted from these mappings and used to compare the results. This is done in Figs. 2(c) and 2(f). Overall, the good fitting obtained shows that the mechanics of the structure is well described by the model. Close to the vertical SOI/SGOI interface, the SiGe has an in-plane lattice 0.4% larger than the unstrained Si reference. The top-Si film is compressively strained by −0.4%. The rotation map in Fig. 2(d) evidences a large anticlockwise rotation of the tip of the SiGe film to a maximum of 1.4°, while the tip of the Si film rotates clockwise down to 0.0°. Close to the SOI/SGOI interface, the elastic energy contained in the SiGe film drives the re-equilibrium of the mechanical stresses. The SiGe layer partially relaxes its in-plane compressive strain, and the resulting film displacement laterally compresses the Si layer. This lateral pressure induces the large downward bending of the tip of the SiGe film. The observed redistribution of strain involves quite large displacements of the layers in the horizontal direction, of 1 nm on the left at the SOI/SGOI interface. They are rendered possible by the viscous flow of the BOX taking place during the high temperature RTO step leading to the Ge-enrichment.

Figures 3(a) and 3(e) show the experimental mappings of the in-plane component of strain ε_{xx} and of the lattice rotation R_{xz} obtained by DFEH on the SiGe side of sample B, i.e., after STI etching and filling. The corresponding profiles obtained along the layers are shown in Figs. 3(d) and 3(h).

The map of ε_{xx} exhibits a peak value of 1.1% at the edge with the STI (from 0.4% before STI fabrication), showing that the SiGe layer is now almost fully relaxed in this region. This strain smoothly decreases down to 0.0%, the value expected for a fully compressively strained layer, at a distance of about 300 nm away from the STI edge. The rotation map shows an anticlockwise rotation of the layer of 0.8° at this STI edge which rapidly turns into a large clockwise rotation with a peak value of −0.4° at a distance of about 50 nm from the STI edge and from where it slowly decreases down to the value of 0.4° which characterizes the miscut angle.

Results from our FEM model are shown in Figs. 3(b) and 3(f), while the corresponding profiles are plotted in Figs. 3(d) and 3(h), respectively. This model predicts an in-plane strain component ε_{xx} of about 0.6% close to the STI edge, falling down to below 0.1% at a distance of 50 nm from it, at strong contrast with the experimental results. In other words, the FEM model strongly underestimates the amount and lateral extension of the relaxation of the compressive SiGe layer in the vicinity of the STI edge. The relatively high lattice rotations R_{xz} observed in Fig. 3(e) close to the edge of the STI and the inversion of the rotation at around 50 nm from the edge are also not reproduced by the model [Fig. 3(f)]. Instead, the

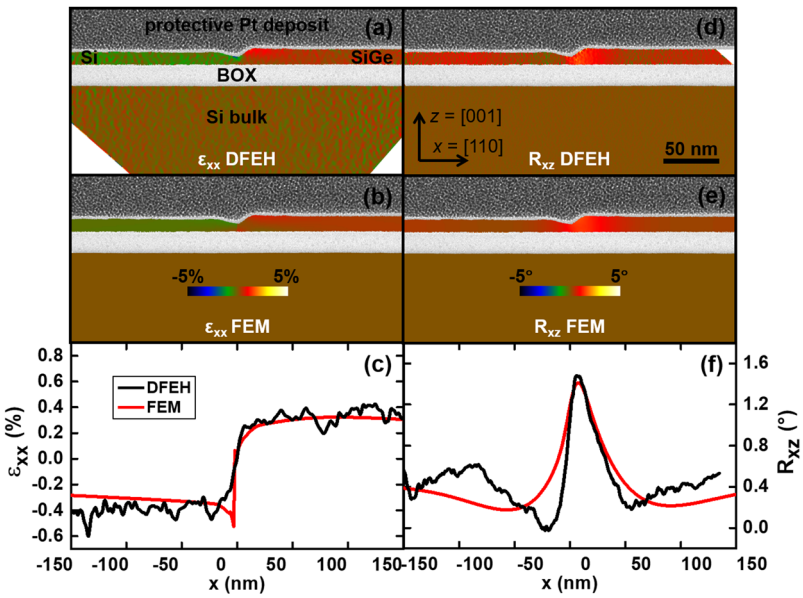

FIG. 2. In-plane strain maps of sample A measured by (a) DFEH and (b) simulated by FEM. (c) In-plane strain profiles extracted within the thin layer. Rotation maps of sample A measured by (d) DFEH and (e) simulated by the FEM model. (f) Rotation profiles extracted within the thin layer. The colored strain and rotation maps originating from the crystalline parts of the sample are encrusted in the bright-field TEM images showing the amorphous regions in gray, to help the reader.

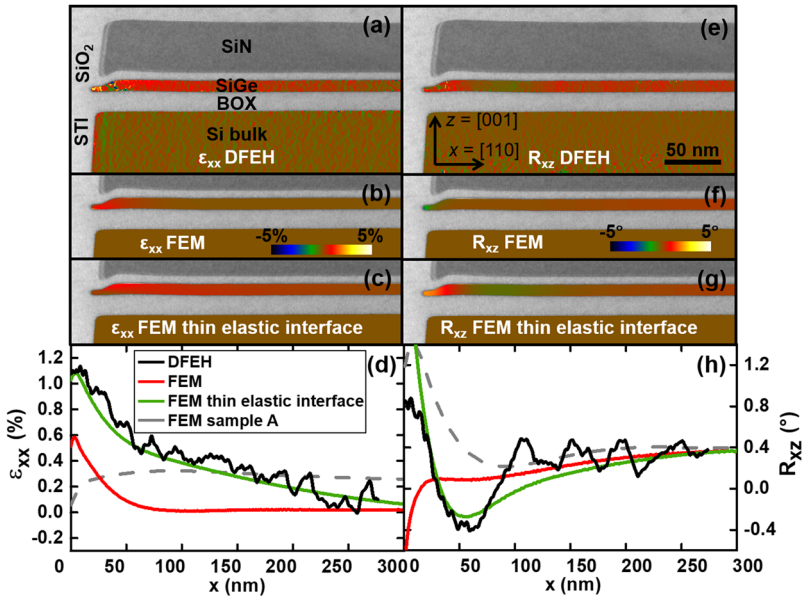

FIG. 3. In-plane strain maps of sample B measured by (a) DFEH and simulated by (b) *FEM* and (c) *FEM thin elastic interface* models. (d) In-plane strain profiles extracted within the SiGe layer and reported from the preceding state. Rotation maps of sample B measured by (e) DFEH and simulated by (f) *FEM* and (g) *FEM thin elastic interface* models. (h) Rotation profiles extracted within the SiGe layer and reported from the preceding state. The colored strain and rotation maps originating from the crystalline parts of the sample are encrusted in the bright-field TEM images showing the amorphous regions in gray, to help the reader.

model predicts rather clockwise rotations of the layer at the STI edge.

It is important to note that this strain relaxation is not associated with the formation of any detectable extended defect in the SiGe crystal and thus cannot be associated with the plastic relaxation of this layer. To address this issue, we have modified our model. As the processes carried out after sample A involve only relatively low temperatures, some viscous behavior of the BOX is unlikely to have influenced the strain state of the SiGe layer. Instead, we suggest that the strain redistribution observed in sample B results from relative displacements between the SiGe and BOX materials, at the interface.[27,28] We have thus decoupled in the model the displacements between the two sides of the SiGe/BOX interface. A thin elastic layer boundary approach is used, where the two boundary planes of each material defining the interface are now linked by elastic forces of equal amplitudes but of opposite directions and proportional to the relative displacement they suffer at this point. It is introduced in the FEM model using the following expression:

$$\sigma_{\vec{n},\vec{t}} = -k_{\vec{n},\vec{t}} \cdot \left(u^{+}_{\vec{n},\vec{t}} - u^{-}_{\vec{n},\vec{t}}\right),$$

where σ is the stress of the thin elastic layer, $k_{\vec{t}}$ (respectively $k_{\vec{n}}$) is the tangential (respectively normal) stiffness constants per unit area of the thin elastic layer, and $u^{+} - u^{-}$ describes the relative displacement of the materials between both sides of the interface. Main characteristics of the experimental results can be reproduced using this model we have named "*FEM thin elastic interface*". The agreement between experimental results and simulations can be rendered excellent, provided the tangential and normal stiffness constants per unit area of the thin elastic layer located at the SiGe/BOX interface are properly adjusted. Figures 3(c) and 3(g) show the results obtained with $k_t = 1 \times 10^{16}$ N m^{-3} and $k_n = 3 \times 10^{16}$ N m^{-3}. Moreover, this description of this interface can also simulate the rotation characteristics we have observed [Fig. 3(h)]. Indeed, the tensile SiN layer deposited onto the compressive SiGe layer defines a bilayer structure which can now efficiently release stress by generating a clockwise rotation of the system from 25 nm to 200 nm from the STI edge. The *FEM thin elastic interface* model well reproduces the larger strain relaxation of the SiGe layer measured in the vicinity of the STI [Fig. 3(d)]. Finally, it is interesting to note that this model predicts that the relaxation of the SiGe layer produces a horizontal displacement toward the STI trench with a maximum value of 0.8 nm at the STI edge.

Sample C is obtained after STI annealing at 1050 °C for 30 min, i.e., after the highest thermal budget the wafer has received, followed by CMP processing and SiN hard mask removal. It is important to remind that following this high temperature annealing, the SiGe composition is constant over the layer depth and equal to 22 at. %.

The experimental ε_{xx} map [Fig. 4(a)] and the associated profile in Fig. 4(d) show that the $Si_{0.78}Ge_{0.22}$ layer is fully relaxed close to the STI edge (ε_{xx} = 0.8%) and stays highly relaxed up to 300 nm from this edge (ε_{xx} is still 0.6%). The rotation map shown in Fig. 4(e) and the associated profile [Fig. 4(h)] still show a large anticlockwise rotation of 1.2° at the STI edge, an inversion to clockwise rotation at a distance of 70 nm from it and a slow return to the miscut angle of 0.4° at larger distances. These experimental results evidence a further and significant strain relaxation of the SiGe layer following this last processing step. As shown in Figs. 4(b) and 4(f), the regular FEM model falls short on simulating this behavior. Although the viscous flow of the BOX (BOX creeping[29]) was allowed in the model, the predicted elastic relaxation of the SiGe layer is by far underestimated. In the light of these comparisons, it becomes clear that, again, the experimental results cannot be explained without allowing large relative displacements along the SiGe/BOX interface. For this reason, we have used our *FEM thin elastic interface* model. Figure 4(c) and the corresponding profile in Fig. 4(d) show that excellent agreement between this model and the experimental results can be obtained by keeping the same normal interface stiffness constant $k_n = 3 \times 10^{16}$ N m^{-3} than previously used but

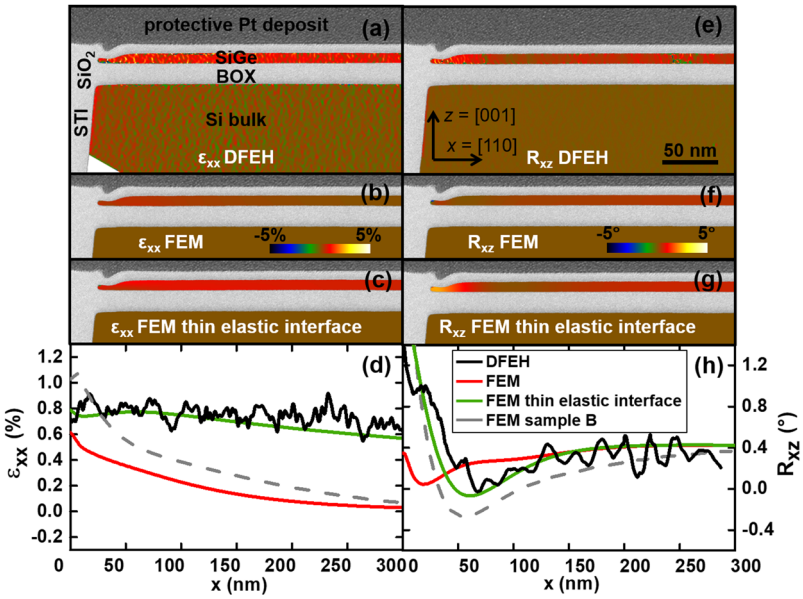

FIG. 4. In-plane strain maps of sample C measured by (a) DFEH and simulated by (b) *FEM* and (c) *FEM thin elastic interface* models. (d) In-plane strain profiles extracted within the SiGe layer and reported from the preceding state. Rotation maps of sample C measured by (e) DFEH and simulated by (f) *FEM* and (g) *FEM thin elastic interface* models. (h) Rotation profiles extracted within the SiGe layer and reported from the preceding state. The colored strain and rotation maps originating from the crystalline parts of the sample are encrusted in the bright-field TEM images showing the amorphous regions in gray, to help the reader.

further reducing the tangential interface stiffness constant down to $k_t = 2 \times 10^{15}$ N m^{-3}. In this case, the relaxation of the SiGe layer induces a horizontal displacement with a maximum value of 3.8 nm at the STI edge.

This denotes a further degradation of the SiGe/BOX interface during this process step. Since we do not expect that the planarization itself, carried out at room temperature, may have affected the interface, we believe that this loosening of the SiGe/BOX interface properties must be put in relation with the Ge-enrichment of the SiGe layer at the interface (from 5 to 22 at. %) resulting from the high temperature annealing used to densify the STI oxide. The large relaxation of the SiGe layer we have evidenced after this step can now be understood as resulting from the removing of the tensile SiN hard mask. Indeed, this thick layer hosting a high elastic energy density (+0.13 J m^{-2}) was maintaining the underneath SiGe layer (hosting itself an elastic energy density of −0.05 J m^{-2}) under compressive stress.

Finally, we need to discuss some mechanism able to explain the SGOI film over-relaxation we have evidenced during the STI fabrication. We have seen that such relaxations typically involve horizontal displacements of several atomic bond lengths close to the STI edge. Thus, this behavior must rely on some nonelastic micromechanisms. Since the relaxations are observed in the vicinity of trenches, we infer that they result from the production of successive elementary relative horizontal displacements of the film over the SiGe/BOX interface, from the STI edge toward the center of the structure. Since we have not observed any delamination or cracking of this interface, we further infer that these relative displacements are produced by the propagation of some interfacial defects that allow the dynamic reconstruction of the interface. Indeed, following STI formation, some dramatic shear stress is generated at the very edge of the STI and is maximum at the SiGe/BOX interface. We suggest that the reduction in this shear stress provides the driving force for the nucleation and/or propagation of such defects. Initially maximum at the STI edge, the shear stress propagates along the interface as the film incrementally slips from the edge and thus decreases in intensity until it reaches a distance from the edge where the elastic shear energy is not sufficient to sustain the defect propagation mechanism. From this region inwards, the system again behaves elastically. Finally, within this scenario, the k_t values needed in the model to simulate the experimental results only reflect the intensity of the interfacial shear stress needed to propagate the defect responsible for relaxation along the interface. The ability of this interface to sustain more or less easily such a mechanism for stress relaxation must be related to the evolution of the SiGe layer composition and structure during Ge-enrichment and diffusion. As k_t decreases when the Ge concentration at the interface increases, we suggest that the SiGe/BOX interface is somehow modified by the continuous arrival of Ge atoms, during the Ge-enrichment and homogenization steps, both processes occurring at high temperature.

In summary, we have studied the evolution of strain in c-SGOI layers fabricated locally onto SOI wafers by the Ge-condensation technique. We show that, at first, BOX creeping, i.e., the viscous flow of SiO_2 at high temperature, allows the redistribution of strain in the vicinity of the vertical interface separating the Si from the SiGe top layers. Furthermore, when the STI trench is etched between the two layers, the initially compressive SiGe layer anomalously relaxes by allowing some relative displacement between the SiGe layer and the BOX in the interface plane. The structure first reacts to the stress exerted by the tensile SiN hard mask but relaxes over long distances when this mask is removed. We have also noticed that this degradation of the mechanical properties of the SiGe/BOX interface increases as the concentration of Ge in the region close to this interface increases, at least when activate through diffusion at high temperature.

We have proposed a mechanism where the relative displacements of the SiGe layer and the BOX are rendered possible by the propagation of defects at the interface. These defects, which

probably nucleate close to the STI edge where the shear stress is maximum, further propagate from the edge to center of the structure, in the opposite direction to the displacements of the SiGe layer, driven by the shear stress. The nature and microscopic structure of this defect cannot be elucidated from our studies and thus remains elusive. However, the Ge-enrichment technique used to transform the top-Si layer into a SiGe layer is pointed out to generate the modifications of the structure of the interface at the origin of the mechanical degradations we have evidenced.

This work was part of the "nanoStress" project and funded by Minefi under the Nano 2017 Program. We also acknowledge the financial support from the European Union (No. 312483-ESTEEM2) and from the French National Research Agency under the program "Investissement d'Avenir" (No. ANR-10-38-01-EQPX.) to access to the Hitachi "I2TEM" and FIB facility.

REFERENCES

[1] Y. Song, H. Zhou, Q. Xu, J. Luo, H. Yin, J. Yan, and H. Zhong, J. Electron. Mater. **40**, 1584 (2011).
[2] Y. Sun, S. E. Thompson, and T. Nishida, J. Appl. Phys. **101**, 104503 (2007).
[3] Y.-C. Yeo, Semicond. Sci. Technol. **22**, S177 (2007).
[4] R. Thomas, D. Benoit, A. Pofelski, L. Clement, P. Morin, D. Cooper, and F. Bertin, ECS Trans. **50**, 241 (2013).
[5] O. Weber, E. Josse, J. Mazurier, N. Degors, S. Chhun, P. Maury, S. Lagrasta, D. Barge, J. P. Manceau, and M. Haond, in *2015 Symposium on VLSI Technology* (VLSI Technology, 2015), pp. T168–T169.
[6] T. Tezuka, N. Sugiyama, T. Mizuno, M. Suzuki, and S. Takagi, Jpn. J. Appl. Phys. **40**, 2866 (2001).
[7] T. Tezuka, S. Nakaharai, Y. Moriyama, N. Sugiyama, and S. Takagi, IEEE Electron Device Lett. **26**, 243 (2005).
[8] F. K. LeGoues, R. Rosenberg, and B. S. Meyerson, Appl. Phys. Lett. **54**, 644 (1989).
[9] B. Vincent, J.-F. Damlencourt, V. Delaye, R. Gassilloud, L. Clavelier, and Y. Morand, Appl. Phys. Lett. **90**, 074101 (2007).
[10] L. Souriau, G. Wang, R. Loo, M. Caymax, M. Meuris, M. M. Heyns, and W. Vandervorst, ECS Trans. **25**, 363 (2009).
[11] V. Boureau, D. Benoit, B. Warot, M. Hÿtch, and A. Claverie, Mater. Sci. Semicond. Process. **42**, 251 (2016).
[12] E. Long, A. Galeckas, A. Yu Kuznetsov, A. Ronda, L. Favre, I. Berbezier, and H. H. Radamson, J. Appl. Phys. **113**, 104310 (2013).
[13] P. Morin, G. Raymond, D. Benoit, P. Maury, and R. Beneyton, Appl. Surf. Sci. **260**, 69 (2012).
[14] A. T. Tilke, C. Stapelmann, M. Eller, K. H. Bach, R. Hampp, R. Lindsay, R. Conti, W. Wille, R. Jaiswal, M. Galiano, and A. Jain, IEEE Trans. Semicond. Manuf. **20**, 59 (2007).
[15] M. Hÿtch, F. Houdellier, F. Hüe, and E. Snoeck, Nature **453**, 1086 (2008).
[16] E. Snoeck, F. Houdellier, Y. Taniguch, A. Masseboeuf, C. Gatel, J. Nicolai, and M. Hÿtch, Microsc. Microanal. **20**, 932 (2014).
[17] H. Müller, I. Maßmann, S. Uhlemann, P. Hartel, J. Zach, and M. Haider, Nucl. Instrum. Methods Phys. Res., Sect. A **645**, 20 (2011).
[18] K. Harada, A. Tonomura, Y. Togawa, T. Akashi, and T. Matsuda, Appl. Phys. Lett. **84**, 3229 (2004).
[19] M. J. Hÿtch, C. Gatel, and K. Ishizuka, *HoloDark Phase* (HREM Research, 2010).
[20] F. Fournel, H. Moriceau, B. Aspar, K. Rousseau, J. Eymery, J.-L. Rouvière, and N. Magnea, Appl. Phys. Lett. **80**, 793 (2002).
[21] L. A. Giannuzzi and F. A. Stevie, *Introduction to Focused Ion Beams: Instrumentation, Theory, Techniques and Practice* (Springer Science & Business Media, 2006).
[22] J. J. Wortman and R. A. Evans, J. Appl. Phys. **36**, 153 (1965).
[23] E. P. EerNisse, Appl. Phys. Lett. **30**, 290 (1977).
[24] E. A. Irene, E. Tierney, and J. Angilello, J. Electrochem. Soc. **129**, 2594 (1982).
[25] J. Dismukes, L. Ekstrom, and R. Paff, J. Phys. Chem. **68**, 3021 (1964).
[26] J. Barber, *Elasticity*, 3rd ed. (Springer, 2010).
[27] V. Boureau, "Déformations introduites lors de la fabrication de transistors FDSOI : Une contribution de l'holographie électronique en champ sombre," Ph.D. thesis, Université de Toulouse, 2016.
[28] S. Reboh, R. Coquand, S. Barraud, N. Loubet, N. Bernier, G. Audoit, J.-L. Rouviere, E. Augendre, J. Li, J. Gaudiello, N. Gambacorti, T. Yamashita, and O. Faynot, Appl. Phys. Lett. **112**, 051901 (2018).
[29] R. Berthelon, F. Andrieu, B. Mathieu, D. Dutartre, C. L. Royer, M. Vinet, and A. Claverie, in *2018 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS)* (IEEE, 2017), pp. 91–94.