From 1.8V to 0.19V voltage bias on analog spiking neuron in 28nm UTBB FD-SOI technology

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***Abstract*—The emergence of new hardware-oriented algorithms for convolutional neural networks (CNNs) or spiking neural networks (SNNs) used for efficient data interpretation, made neuromorphic computing a very promising solution. SNNs are very attractive due to their particularly low power consumption. This paper presents a comprehensive analysis of an analog spiking neuron designed in 28 nm UTBB FD-SOI CMOS technology from STMicroelectronics. Thick oxide MOS transistors with regular VT are selected to perform a low power design enhanced by using sub-threshold bias. The neuron operation is presented and analyzed through SPICE simulations performed at 0.7 V nominal voltage bias. Several parameters control the shape of the neuron response, such as: the synaptic excitation, the spike duration, and the refractory period. The neuron under study was fabricated and characterized for bias voltages ranging from 1.8 V standard bias to the measured limit of 0.19 V. The full functionality of the analog spiking neuron in FD-SOI is demonstrated.**

Keywords—artificial neuron, spiking neural network, low power

I. Introduction

Analog based neuromorphic circuits, such as analog SNNs are bio-inspired and show great potential to provide energy-efficient data-centric computing solutions. This has led to massive research efforts being directed on one side towards brain-inspired learning algorithms that can be performed by these structures and on the other side towards the actual hardware design and the optimal implementation of SNNs [1-2]. In this context, the paper is focused on a low power, analog spiking neuron circuit design. It is implemented and validated in in 28 nm ultra-thin body and buried oxide (UTBB) FD-SOI with High-K metal gate. Fig. 1a depicts the original design which is the efficient and robust Axon-Hillock circuit [3-5], where Cmem is the membrane capacitor, Vmem is the membrane potential, and the four current sources are used to control the behavior of the neuron, i.e., the width of the emitted spike, the duration of the refraction period and membrane leakage. The fourth current source represents the input received from the corresponding synapses. Fig. 1b illustrates the typical temporal response of the membrane potential (Vmem). Here, the linear integration, spike duration and refractory period are highlighted. The purpose of this work is to implement a more power efficient spiking neuron, while properly controlling its behavior thanks to few available design parameters. One way to achieve low power consumption is to perform neuron operation in the subthreshold regime. This study has been performed on standard 28 nm FD-SOI design kit, with regular design/layout, and explores deep sub-threshold responses.

II. Analog Spiking Neuron Design & Simulations

In this section, we introduce an optimized analog neuron design and its custom layout based on CMOS transistors with thick oxide and regular threshold voltage (V_T). Fig. 2 depicts the circuit schematics, the circuit layout, and the evaluation of area consumption per neuron sub-functionality. In the circuit schematic, five regions are highlighted: the synapse region, generating the synaptic current, the leak region that generates and controls the membrane leakage current, the out region containing the output buffer chain, the refraction region ensuring the neuron compliance to the refraction period, and finally the Axon-Hillock region that performs the core functions of the neuron, i.e., integration and comparison. The refraction region is an add-on which produce a clear delimitation at the end of the refraction period. The circuit uses VDD, Gnd to bias the design in the 1.8 ÷ 0.19 V voltage range; Vin is the input signal (synaptic excitation); Vout is the output signal; Vtrefra controls the duration of the refractory period; Vtspike controls the spike duration; Vleak controls the

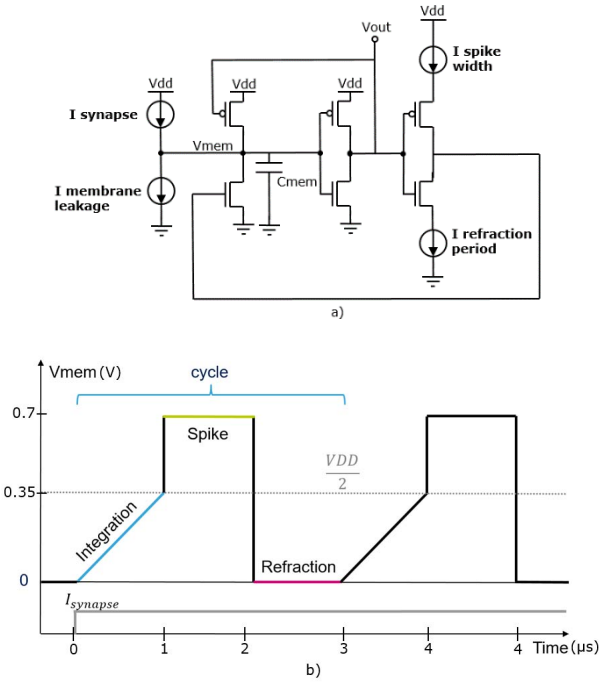


Fig. 1. Example of Axon-Hillock a) schematic and b) typical time response of V_{mem}

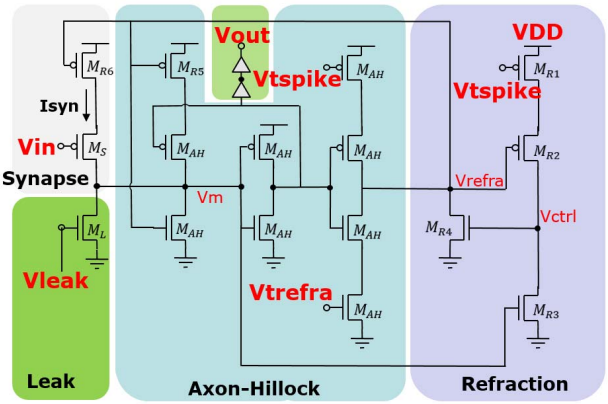
the neuron membrane leakage; Vm is the neuron membrane potential; Vrefra is an integrating node used for spike and refraction duration; Vctrl is a control signal to end the refraction period. It should be noted that the membrane capacitance (Cmem) is not explicitly shown in the schematic in Fig. 2a. This is because its functionality is performed by the lumped parasitic capacitance at node Vm and as such, Cmem is evaluated as being 1.44 fF. The circuit design is initially performed at 0.7 V supply voltage and the integration duration of 1 µs, followed by 1 µs spike width and the duration of the refractory period of 1µs (i.e., the whole neuron cycle completes in 3 x 1 µs, see Fig. 1b). To validate the functionality of the proposed neuron design, SPICE simulations were performed until deep subthreshold regime, expressed by bias voltage lower than 0,7 V down to the 0.19 V limit at room temperature and on typical process corner. Fig. 3 reports the temporal response for relevant nodes of the proposed neuron design. It should be noted that the circuit behaves in agreement with its specifications. The spike energy has been computed and is equal to 8 fJ for 141 fW static power at nominal bias 0.7 V on VDD for the neuron without the output buffers. For this structure, Monte Carlo simulations are performed to give an idea of the robustness of the design. Fig. 4 depicts the responses dispersion in agreement with design specifications. It appears that the relative standard deviation of cycle duration is 55%.

III. Analog Spiking Neuron Silicon Demonstrator

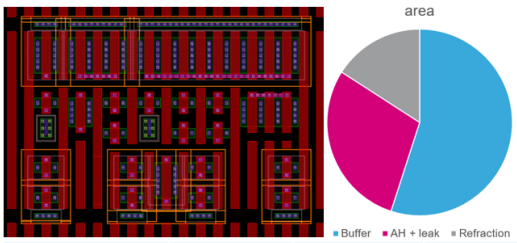
The above simulation results obtained on 28 nm FD-SOI standard transistors and topology validate the design functionality. Therefore, the above-described circuit has been fabricated in an effort to fully demonstrate and characterize the neuron functionality. The characterization of the silicon sample is presented in the next section.

A. Static analysis – Static power characterisation

To evaluate static power consumption the synaptic excitation current is set to null and the membrane leakage to maximum, in order to make sure that no integration would occur on the neuron membrane. Therefore, no spikes are produced at the output of the circuit. Static power is deduced from the average current measurement with B1517A Source Measurement Unit (SMU) on a semiconductor device parameter analyzer Keysight B1500A. All measurements are done at room temperature with the following voltage values: Vtspike = Vtrefra = VDD / 2, Vleak = Vin = VDD. Table I reports the measured static current and static power consumption (last two columns) at different supply voltages (second column) for the proposed neuron design. The static current drawn by separate regions of the circuit is also listed in the table, for example, the synaptic excitation branch in the third column, the core Axon-Hillock branch in the fourth column and the refraction branch in the fifth column. The static current of all the output buffers is not considered here and the power estimation represents only the neuron consumption. We observe a measured static power consumption two decades higher than in simulation for the 0.7 V nominal bias voltage. With this bias condition, the simulation model has lower accuracy (pA value) and the current is shifted by 2 decades compared to transistor characterization, the trends should remain correct, therefore the results are pertinent and can be considered valid for functional validation. Static power consumption spans from 11.3 pW for the minimal bias voltage of 0.2 V up to 188 nW for the maximum bias of 1.8 V.



a)



Part	transistor	Area (µm²)	Area (%)
Buffer out	6	6.15	55
AH + Leak	10	3.25	29
Refraction	6	1.78	15.9
Total transistor	22	11.18	NA
Total cell	NA	16.1	NA
occupation	NA	70 %	NA

b)

Fig. 2. Standard design in 28 nm FD-SOI with a) schematic b) layout and area cost.

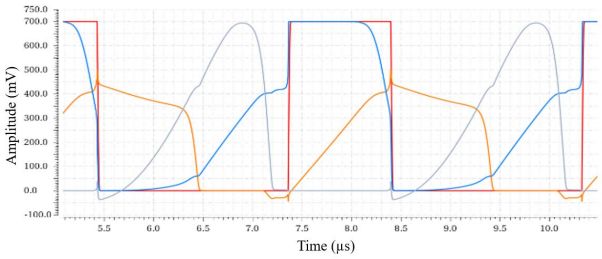


Fig. 3. Typical time simulations in 3 x 1 µs period with nodes tracking, Vout (red), Vrefra (orange), Vm (blue) and Vctrl (grey).

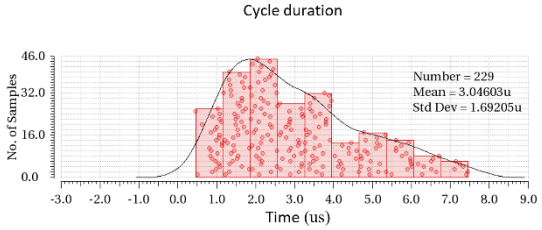


Fig. 4. Typical Monte Carlo simulations in 3 x 1 µs period for global and local process variations.

B. Dynamic analysis

1) Neuron characterization in nominal voltage (0.7 V)

The exploration has been performed at nominal voltage of 0.7 V VDD bias with a sweep of Vin down to 0.2 V. Dynamic

power is deduced from the average current measurement with B1517A SMU on a Keysight B1500A. The spike frequency has been observed with an oscilloscope HAMEG HMO 1522 (150MHz/2GSa). All measurements are done at room temperature with biases as follows: Vtspike = Vtrefra = VDD / 2; Vleak = 0 V. Table II reports the measured values of the power consumption and the spike frequency, shown in columns four and five, for a constant supply voltage of 0.7 V and various values of the synaptic excitation (first column). A maximum spiking frequency of 1.06 MHz is observed for a synaptic excitation of 0.4 V and lower. At this bias, the measured energy per spike is 9 fJ which is 1 fJ higher than the simulation prediction. It should be noted that the spiking frequency is relatively constant for synaptic excitation lower than 0.4 V and it diminishes for larger values of the Vin. The frequency of spike is below the limits of our experimental setup for a synaptic excitation of 0.7 V. It should also be noted that the dynamic power consumption is not negligible, the data showing dynamic power consumption being two decades higher than the static power measurement for the same values of Vin and VDD (see Table I). Fig. 5 depicts the temporal response for a nominal VDD of 0.7 V and a Vin bias of 0.45 V. It can be observed that the measured spikes do not reproduce the square shape observed during SPICE simulations. As in our measures, we have tried without success a scope probe to reduce the output capacitance of the measurement setup, we deduce that there is at least one internal node with slow response that may experience some process dispersion. Process dispersion can be mitigated by applying in-house specific robust design and back-bias techniques to center the design. Nevertheless, this prototype demonstrates expected functionality.

TABLE I. MEASUREMENT RESULTS OF NEURON STATIC POWER CONSUMPTION (WITHOUT THE OUTPUT BUFFERS).

Data type	Supply voltage (V)	Supply current (A)				Static power (W)
		Synapse	*Axon-Hillock*	*Refraction*	*Total*	
M[a]	0.2	1.16 E-11	3.25 E-11	1.25 E-11	5.66 E-11	1.13 E-11
M	0.5	1.24 E-11	3.63 E-11	1.32 E-11	6.19 E-11	3.10 E-11
S[b]	0.7	5.50 E-14	1.32 E-13	1.50 E-14	2.02 E-13	1.41 E-13
M	0.7	1.30 E-11	3.90 E-11	1.40 E-11	6.60 E-11	4.62 E-11
M	1	1.37 E-11	4.21 E-11	1.44 E-11	7.02 E-11	7.02 E-11
M	1.4	2.16 E-09	3.90 E-09	1.88 E-09	7.94 E-09	1.11 E-08
M	1.8	2.71 E-08	5.22 E-08	2.54 E-08	1.05 E-07	1.88 E-07

[a] Measurement

[b] Simulation

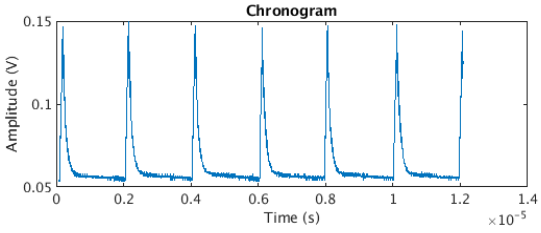


Fig. 5. Measured temporal response of the circuit under nominal VDD bias of 0.7 V.

TABLE II. MEASUREMENT RESULTS OF SPIKE FREQUENCY AND POWER CONSUMPTION FOR DIFFERENT VIN BIAS (SYNAPTIC EXCITATION).

Vin (V)	Supply voltage (V)	Spiking frequency (Hz)	Average power (W)	Energy per spike (J)
0.2	0.7	1.05 E+06	7.30 E-09	6.95 E-15
0.3		1.05 E+06	9.30 E-09	8.86 E-15
0.4		1.06 E+06	9.50 E-09	8.96 E-15
0.5		1.65 E+05	9.00 E-09	5.45 E-14
0.6		7.20 E+03	6.90 E-09	9.58 E-13
0.7		NA	4.80 E-09	NA

2) Neuron characterization in very deep sub-threshold

Further measurements have been performed to characterize the dynamic behavior of the circuit in very deep subthreshold regime. To that end, the spiking frequency and the power consumption have been measured for different values of the supply voltage VDD (lower than VT = 0.65 V down to 0.19 V) and of the synaptic excitation Vin. The results are summarized in Table III. For each VDD value, the Vin has been generated accordingly. We observe a measurement limit at the voltage bias VDD of 0.19 V. The minimum measured power dissipation is observed for a VDD of 0.19 V and Vin of 0.1 V is of 11 pW. This set-up generates spikes at a frequency of 2 kHz and the associated energy per spike is 5.5 fJ. The minimum measured energy per spike is of 2.86 fJ for biases of 0.5 V VDD and 0.1 V Vin which generates spikes at a frequency of 103 kHz for a power consumption of 295 pW. Fig. 6 shows the neuron output temporal response for the biases VDD=0.19 V and Vin=0.17 V, illustrating the functionality of the circuit in deep sub-threshold.

3) Neuron characterization above the theshold voltage

The exploration of neuron functionality has been performed in higher voltage regime as well. For doing this, we have measured the spike frequency and the power consumption for higher than nominal VDD, that is to say up to 1.8 V and using a sweep of Vin bias (synaptic excitation). Tab.4 reports results of power and frequency of spike measurement for higher than nominal VDD biases. The maximal power dissipation measured was of 11.7 µW for a VDD of 1.8 V and Vin of 1.55 V which produce spikes at the frequency of 410 kHz and an associated energy per spike of 28.5 pJ. Fig. 7 reports the neuron output temporal response for the biases VDD= 1.8 V and Vin =1.55 V illustrating the functionality of the circuit above the threshold.

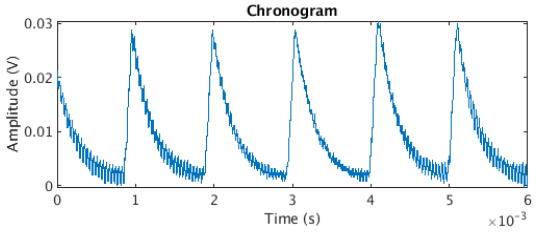


Fig. 6. Measured temporal response of the circuit under nominal VDD bias of 0.19 V.

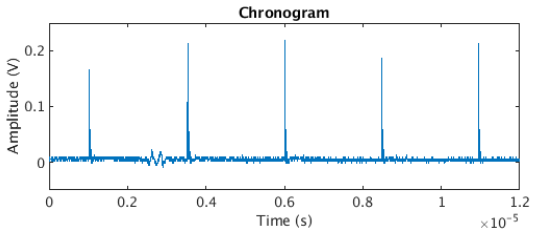


Fig. 7. Measured temporal response of the circuit under nominal VDD bias of 1.8 V.

TABLE III. EASUREMENT RESULTS OF SPIKE FREQUENCY AND POWER CONSUMPTION FOR LOWER THAN NOMINAL VDD BIAS AND DIFFERENT VIN BIAS (SYNAPTIC EXCITATION).

Vin (V)	Supply voltage (V)	Spiking frequency (Hz)	Average power (W)	Energy per spike (J)
0.1	0.5	1.03 E+05	2.95 E-10	2.86 E-15
0.2		1.02 E+05	3.05 E-10	2.99 E-15
0.3		9.30 E+04	3.63 E-10	3.90 E-15
0.4		9.00 E+03	1.73 E-10	1.92 E-14
0.5		4.70 E+02	1.25 E-10	2.66 E-13
0.15	0.2	1.40 E+03	1.22 E-11	8.70 E-15
0.17		1.09 E+03	1.23 E-11	1.13 E-14
0.18		9.25 E+02	1.23 E-11	1.32 E-14
0.19		8.00 E+02	1.17 E-11	1.46 E-14
0.2		6.30 E+02	1.20 E-11	1.90 E-14
0.1	0.19	2.00 E+03	1.10 E-11	5.50 E-15
0.17		1.15 E+03	1.17 E-11	1.02 E-14
0.19		1.00 E+03	1.13 E-11	1.13 E-14

TABLE IV. MEASUREMENT RESULTS OF SPIKE FREQUENCY AND POWER CONSUMPTION FOR HIGHER THAN NOMINAL VDD BIAS AND A CONSTANT VIN BIAS (SYNAPTIC EXCITATION).

Vin (V)	Supply voltage (V)	Spiking frequency (Hz)	Average power (W)	Energy per spike (J)
0.75	1	6.47 E+05	1.48 E-0.7	2.29 E-13
0.95	1.2	4.61 E+0.5	6.98 E-0.7	1.51 E-12
1.15	1.4	4.71 E+0.5	2.36 E-0.6	5.01 E-12
1.35	1.6	4.40 E+0.5	5.80 E-0.6	1.32 E-11
1.55	1.8	4.10 E+0.4	1.17 E-0.5	2.85 E-11

IV. CONCLUSION

In this study, we have presented the design, its characterization and corresponding silicon measurements of a 28 nm UTBB FD-SOI analog spiking neuron based on Axon-Hillock approach. The design allows to control the membrane leakage, the synaptic excitation, the spike duration and the refractory period. The design is designed at 0.7 V. However, the applied voltage range has been set in the [1.8 V – 0.19 V] interval and show correct functionality. SPICE simulations demonstrate good responses of the spiking neuron and Monte Carlo simulations give the dispersion range of time responses. The silicon demonstrator proofs the full range of bias voltage of the design. It appears two-decade shift in current between simulation and measurements due to the complexity of the calibration in deep sub threshold.

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