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Mokhtar Aly, Samir Kouro, Thierry Meynard. Topology and Voltage Balance of Series-Connected T-type Inverter for Medium-Voltage Drive Applications. 2020 IEEE 11th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Sep 2020, Dubrovnik, Croatia. pp.154-158, 10.1109/PEDG48541.2020.9244333 . hal-02999719

HAL Id: hal-02999719

<https://hal.science/hal-02999719>

Submitted on 2 Dec 2020

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Topology and Voltage Balance of Series-Connected T-type Inverter for Medium-Voltage Drive Applications

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Abstract—The three-level T-type multilevel inverter has proven itself as a promising, highly-efficient, and low-switch-count topology. This paper presents a new topology configuration using series connected T-type multilevel inverters for medium-voltage applications. The proposed topology utilizes the series connection of low power T-type modules to enable medium-voltage operation. The proposed topology is modular, highly efficient, less complex, and with lower component count, compared to other topologies with the same number of levels and voltage operating range. In addition, a simple level-shifted pulse width modulation (LSPWM) method is proposed for achieving voltage balance between the de-link capacitors. The results show the effectiveness of the proposed topology and the proposed LS-PWM method for medium-voltage applications. Moreover, the proposed topology has been compared with the existing medium-voltage converter topologies in the literature.

Index Terms—Level shifted pulse width modulation, mediumvoltage drives, multilevel inverter, T-type inverter.

I. INTRODUCTION

The superior performance and wider applicability of multilevel inverters (MLIs) have made them favorable over conventional two-level inverters for an increasing number of applications [1], [2]. The improved power quality, reduced common mode voltages, and higher efficiency represent the main benefits of utilizing MLIs in medium-voltage applications [3], [4]. The power quality improves with the increase of the number of the output voltage levels. However, increasing the number of levels in the output voltage results in increasing the number of required components. This in turn can impose complexities to other system components such as input transformer design, modulation and controller, capacitor voltage balance, and even increase the system costs [5], [6].

Several MLI topologies have found industrial application in high-power medium-voltage (HP-MV) drive systems, such as cascaded H-bridge (CHB), neutral point clamped (NPC), active NPC (ANPC), flying capacitor (FC), and modular multilevel converters (MMCs), among others [7]-[12]. Moreover, there are several extensions of these basic structures to develop hybrid MLI topologies [5], [13].

The CHB and the MMCs present a modular solutions. However, for medium-voltage applications the circulating current problems, complex control, and sensitivity to passive elements mismatch represent the main drawbacks of MMCs [14], [15]. This has hindered the applicability of MMC for medium-voltage drives applications, and has been only used in practice for high-voltage DC transmission applications. On the other hand, CHB topologies suffer from the high number of required isolated de sources based on complex zig-zag transformers [16], and although they have been successfully used in medium-voltage drives, the lack of a real backto-hack regenerative option (a few manufacturers offer an active-front-end based on two-level three phase voltage source inverters instead of passive diode rectifiers) have restricted their application mainly to pumps, fans and other standard medium-voltage drives.

NPC based topologies have been presented in the literature with five and seven level output voltages [8], [9], [17]. However, they lack of modularity and require a high number of components due to the necessary clamping diodes, which increase the cost and reduce the efficiency of the system. Capacitor voltage balance also becomes an issue for NPCs with more than three levels when using passive front ends. Improving on the NPCs, several active NPC (ANPC) topologies have been proposed in the literature for mediumvoltage applications [18], [19]. ANPC-based topologies are successful at eliminating the clamping diodes, which improves the efficiency and reduces the cost, and provides a way to distribute thermal losses across devices eliminating the need of power derating [20]. Additionally, hybrid FC and ANPC topologies have been presented in the literature to combine the benefits of FC and the ANPC topologies [4], [20], [21]. Although, they suffer from the high number of power switches and capacitors. In addition, they possess higher conduction losses due to the increased number of conducting switches. In [22], series connection of NPC modules has been proposed for reaching medium-voltage operation. However, this topology inherits the drawbacks of the traditional NPC, including the clamping diodes.

It has become clear that the existing medium-voltage topologies can suffer from one or more drawbacks, including in-

TABLE I: Output voltage levels and switching states for the proposed topology ($E = V_{dcX}/4$)

Amplitude	Output Voltage	T-type Module 1				T-type Module 2			
		S_{X11}	S_{X12}	S_{X13}	S_{X14}	S_{X21}	S_{X22}	S_{X23}	S_{X24}
$4V_{dc}$	$V_{CX1}+V_{CX2}+V_{CX3}+V_{CX4}$	1	1	0	0	0	0	1	1
$3V_{dc}$	$V_{CX1}+V_{CX2}+V_{CX3}$	1	1	0	0	0	1	1	0
	$V_{CX2}+V_{CX3}+V_{CX4}$	0	1	1	0	0	0	1	1
$2V_{dc}$	$V_{CX1}+V_{CX2}$	1	1	0	0	1	1	0	0
	$V_{CX2}+V_{CX3}$	0	1	1	0	0	1	1	0
	$V_{CX3}+V_{CX4}$	0	0	1	1	0	0	1	1
V_{dc}	V_{CX2}	0	1	1	0	1	1	0	0
	V_{CX3}	0	0	1	1	0	1	1	0
0	0	0	0	1	1	1	1	0	0

creased switch count, increased number of isolated dc sources, low efficiency, lack of modularity, complex modulation or control and/or increased number of sensors. In this paper a new series-connected T-type topology for medium-voltage drive applications is presented. The proposed topology benefits the advantages of three-level T-type modules of lower conduction losses, and lower number of components. In addition, the series connection of low voltage T-type modules are employed for fulfilling the medium-voltage drive operation. In addition, a simple method for voltage balance over the dc-link capacitors is proposed in this paper. The proposed controller is based on the level-shifted pulse width modulation (LS-PWM) and the redundancy property of T-type inverters. Thence, dc-link voltage control and balance can be achieved through employing simple control without adding more components nor complexity to the drive control system.

The remaining of the paper is organized as follows: Section II presents the power circuit topology and the operation of the new proposed topology. The proposed LS-PWM method for capacitor voltage balance control is presented in Section III. The simulation results of the proposed topology and controller are provided in Section IV. The proposed topology is compared with the existing topologies in the literature in Section V. Finally, conclusions are addressed in Section VI.

II. CIRCUIT TOPOLOGY AND OPERATION

The three level T-type inverter has proven superior performance for different applications, including renewable energy applications, UPS systems and motor drive applications [23], [24]. The T-type inverter is advantageous from the number of component and reduced conduction losses point of views. Each inverter leg is composed of four power switches, wherein two of them are similar to the conventional H-bridge leg and the other two are connected in bidirectional cell to the neutral point of the inverter. However, the traditional three-level T-type modules are not suitable for several medium-voltage applications due to the limitations of the blocking voltages of existing commercial switches.

Fig. 1 shows the circuit configuration of the proposed five-level topology. Each phase leg is constructed through the series connection of two three-level T-type modules. An isolated dc-source is required for each phase leg, which in normally

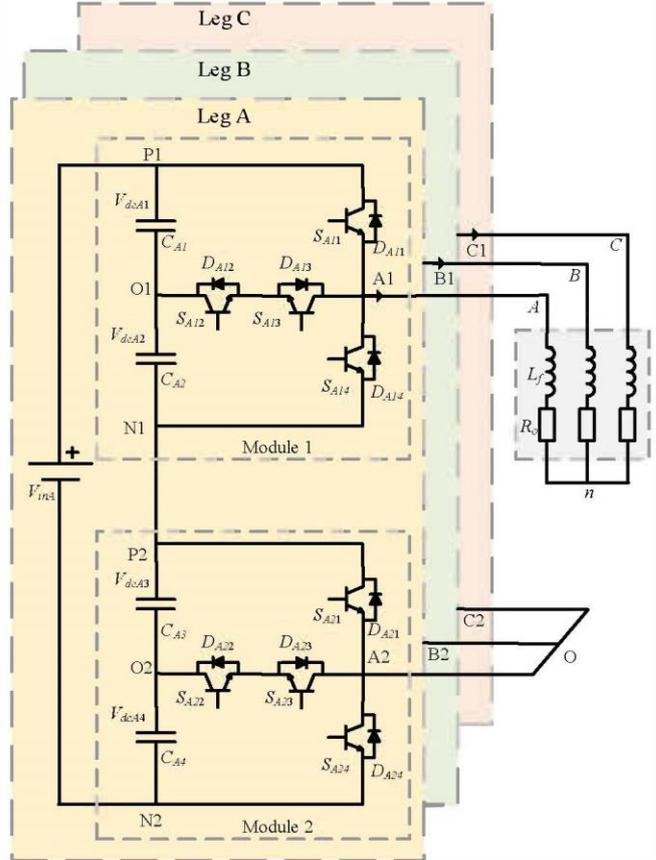


Fig. 1: Power Circuit of the proposed series connected T-type topology.

generated by phase shifted transformers followed by diode bridge rectifiers. The dc voltage is divided equally among the four dc-link capacitors ($C_{X1}, C_{X2}, C_{X3}, C_{X4}$), (where $X \in A, B, \text{ or } C$). Hence, each capacitor voltage ($V_{dcX1}, V_{dcX2}, V_{dcX3}, V_{dcX4}$) is controlled to hold one fourth of the dc-link voltage ($V_{dcX}/4$). The three phase output of the inverter are connected to the load (L_X inductance in series with R_X resistance). The inverter has the neutral point of the load output n , and the connection of the lower module forms a floating neutral point N . Table I summarizes the output voltage levels and switch combination of the proposed topology.

Each T-type module can generate three level output voltage, whereas the connection of two series T-type modules can generate five level output voltage. It can be seen from Table I that each phase leg has nine different switching states, and some of the states are redundant. Redundant switching states can generate the same output voltage level, while they employ different dc-link capacitors and different power switches. Moreover, the charging and/or discharging of dc-link capacitors is highly dependent on the employed switching state.

III. VOLTAGE BALANCE METHOD

Several methods have been proposed in the literature for controlling the dc link capacitor voltage unbalance, such as space vector PWM (SVPWM) [23], [25], phase shift PWM (PS-PWM), level-shifted PWM (LS-PWM) [26], model predictive control (MPC) [27], to name a few. In [28], the PS-PWM has been proposed for controlling capacitor voltages of the series NPC converters. However, complexity arises for the phase output instead of the module output. Whereas, the LS-PWM can determine the output level directly and then the redundant switching states can be employed for controlling the capacitor voltages. Therefore, the LS-PWM method is selected for implementing the proposed voltage balance algorithm in this paper.

Fig. 2 shows the flowchart of the proposed voltage balance algorithm. The proposed controller is based on the LS-PWM through employing the redundancy property of the proposed topology. Firstly, the proposed algorithm generates the modulating signal and the four carrier waveforms for each phase leg. Secondly, through the comparison of the modulating signal and the carrier, the algorithm defines the operating region of the required output voltage levels. Thirdly, the algorithm checks the redundancy in the required voltage levels as shown in Table I. For instance, each of the voltage levels $3V_{dc}$, and V_{dc} possesses two redundant switching states, and the voltage level $2V_{dc}$ has three redundant switching states. Whereas, the voltage levels $4V_{dc}$, and zero do not have redundant switching states. Lastly, suitable redundant vector is selected according to its effects on the voltages of dc-link capacitors and then the gating signals are generated to drive the inverter. For example, the two redundant vectors of the voltage level $3V_{dc}$ at positive current direction have the possibility of charging the capacitor C_{X1} or C_{X4} according to their relative charge. Thence, the suitable redundant vector is selected for this level to achieve the voltage balance over the capacitors.

IV. SIMULATION RESULTS

The proposed topology and voltage balance algorithm are simulated using the PLECS software. The main parameters of the selected case study are: input dc voltage 10.7 kV, output line-line voltage 6.9 kV, dc-link capacitors 2.2 mF, output full load resistance 25 Ω , and output inductance 3 mH. The proposed inverter and voltage balance algorithm are tested at different load changes and modulation index (mi) changes).

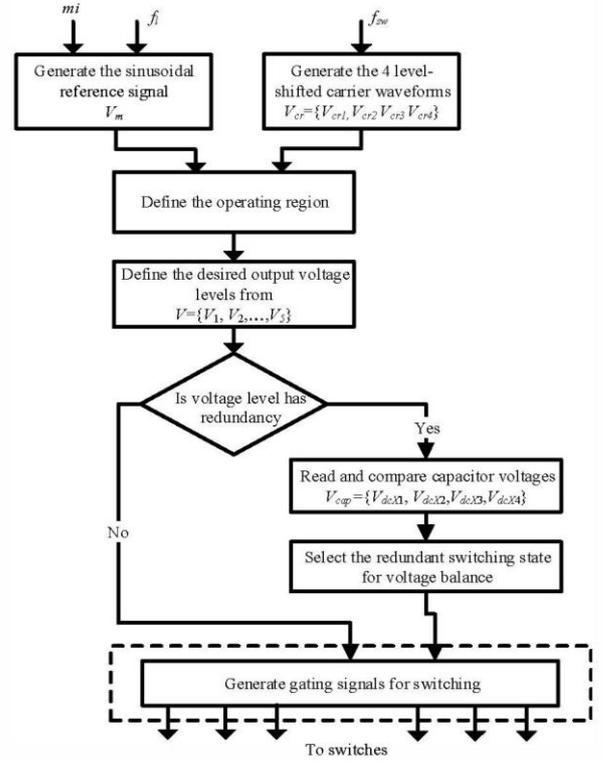


Fig. 2: Flowchart of the proposed voltage balance algorithm.

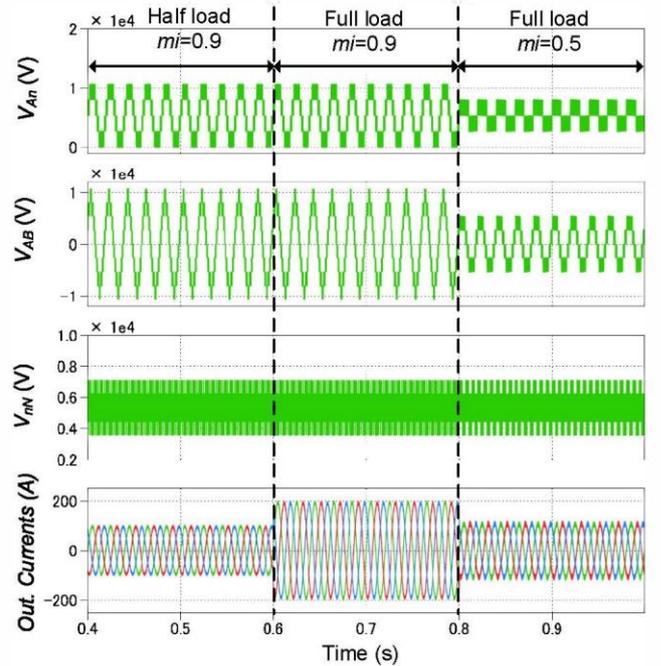


Fig. 3: Simulation results of the proposed topology.

Fig. 3 shows the output phase voltage V_{An} , line-line voltage V_{AB} , the voltage between the neutral points V_{nN} , and the output currents of the inverter. It can be seen that at mi of 0.9 generates five output levels, and nine levels in the line-

TABLE II: Component comparison of the new proposed topology ($E = V_{in}$).

Criterion		CHB	Series NPC	H-T-type	MMC	Proposed topology
Sources	Isolated dc sources	6	3	1	1	3
	dc-link capacitors	0	12	2	0	12
	Flying capacitors	0	0	0	24	0
Count		24	24	24	48	24
Switches	Blocking voltages	$24 \times (V_{in}/2)$	$24 \times (V_{in}/4)$	$12 \times (V_{in}) + 12 \times (V_{in}/2)$	$48 \times (V_{in}/4)$	$12 \times (V_{in}/2) + 12 \times (V_{in}/4)$
	Normalized total blocking voltage	$12E$	$6E$	$18E$	$24E$	$9E$
	Count	0	12	0	0	0
Diodes	Blocking voltages	—	$12 \times (V_{in}/4)$	—	—	—
	Normalized total blocking voltage	—	$3E$	—	—	—
	Count	24	36	24	48	24
Total components	Blocking voltages	$24 \times (V_{in}/2)$	$36 \times (V_{in}/4)$	$12 \times (V_{in}) + 12 \times (V_{in}/2)$	$48 \times (V_{in}/4)$	$12 \times (V_{in}/2) + 12 \times (V_{in}/4)$
	Normalized total blocking voltage	$12E$	$9E$	$18E$	$24E$	$9E$

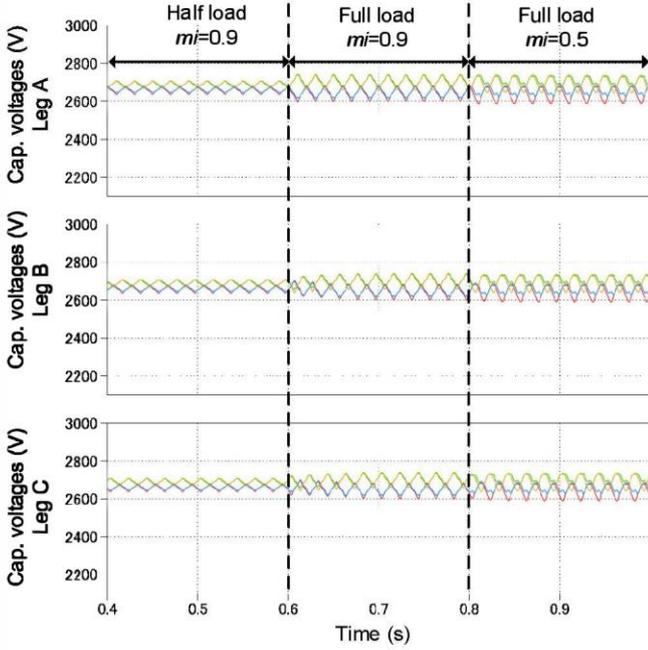


Fig. 4: Simulation results for the dc-link capacitors voltages of the three legs.

line voltage. Whereas at $mi = 0.5$, the phase voltages have a three-level output, and the line-line voltages a five-level output. Moreover, the proposed method can generate a fixed switching frequency output voltage.

Fig. 4 shows the voltages over the dc-link capacitors of the three-phase legs. It can be seen that the proposed algorithm can preserve balanced voltages over the dc-link capacitors at various load changes and mi changes. Firstly, the controller is tested at step change of the load impedance, which has proved fast balance of the voltages without fluctuations. Secondly, the system is tested at step change of the modulation index mi . It can be seen that the voltages are still balanced without

drifting. However, as expected the ripples in the dc-link capacitor voltages are dependent on the loading and mi operating condition. The proposed LS-PWM is advantageous at achieving voltage control of capacitor voltages at each phase independently.

V. TOPOLOGY COMPARISON

Table II compares the proposed topology with the most prevalent medium-voltage topologies in the literature. The performance criteria includes the sources count and capacitors, main switches, diodes, and their voltage stresses. It can be seen that the proposed topology requires lower number of isolated dc sources than the CHB topology. In addition, the proposed topology possesses lower number of switches than MMC topology. The proposed topology and the series connected NPC topology require lower total blocking voltages than alternative topologies. Moreover, the proposed topology does not need clamping diodes as in the series connected NPC topology. The proposed topology can be implemented using the commercially available T-type modules. Thence, the proposed topology eliminates the need for flying capacitors and clamping diodes. This in turn verifies the reduction of the required number of components compared to the other existing topologies in the literature.

VI. CONCLUSIONS

A new series connected T-type topology and simple voltage balance algorithm are presented in this paper for medium-voltage applications. The new proposed topology benefits lower component count, voltage stresses, and without using flying capacitors. In addition, the proposed voltage balance algorithm is based on using the LS-PWM and the redundancy property between switching state, and so it represents simple solution without need for complex calculations. The results of the proposed topology and controller have been shown in the paper at different operating points. The operation,

performance comparison of the proposed topology, and the proposed controller have been presented in the paper. The superior performance of the proposed topology and de-link capacitor voltage controller has become clear.

ACKNOWLEDGMENT

This work was supported by SERC Chile (ANID/FONDAP15110019) and by AC3E (ANID/Basal/FB0008).

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