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Multilevel Converter for 4.16- and 6.6-kV Variable Speed Drives

Jaime W. Zapata , *Member, IEEE*, Gianluca Postiglione, Daniele Falchi , Giovanni Borghetti, Thierry A. Meynard , *Fellow, IEEE*, and Guillaume Gateau, *Member, IEEE*

Abstract—This article presents a new transformerless multilevel converter topology. This power converter is owned by Nidec ASI and is implemented in the medium-voltage drive SILCOVERT-FH. The topology is composed by the series association of two Macro cells, which can be extended in order to increase the number of output levels, and one external selector cell. Among the advantages, the number of devices directly connected in series does not depend on the dc bus voltage. The same devices can be used in 5L and 7L configurations to address the 4.16- and 6.6-kV applications, which is a significant advantage from the industrialization point of view. Moreover, due to its inherent feature, the zero-crossing is performed naturally at zero-voltage switching on the selector cell. Experimental and simulation results are shown in order to validate the performance of the converter, highlighting the main benefits and features of the proposed topology.

Index Terms—DC–AC power conversion, multilevel converters, transformerless, zero-voltage switching.

I. INTRODUCTION

MULTILEVEL topologies have been extensively studied in academia, and widely used in industrial applications due to its maturity and reliability [1]. Initially, the multilevel voltage-source inverters (VSI) emerged in medium-voltage (MV) applications, to overcome the voltage-blocking limitations present in the two-level VSI (2L-VSI) [2]. However, by increasing the number of voltage levels, some additional benefits arise: the reduction of dv/dt , the reduction of output filter size due to the increased output apparent switching frequency, and the improved power quality [3]. In industrial applications, the most common topologies implemented for MV applications are based on two- and three-level configurations. However, due to the limited voltage capability of the semiconductors, the 2L- and 3L-VSI are usually limited to applications up to 4.16 kVac@6.6 kV devices.

Jaime W. Zapata, Gianluca Postiglione, Daniele Falchi, and Giovanni Borghetti are with the Research & Development Department, NIDEC Industrial Solutions, Milan 20092, Italy (e-mail: jaime.w.z@ieee.org; postiglione@Nidec-asi.com; falchi@Nidec-asi.com; borghetti@Nidec-asi.com).

Thierry A. Meynard and Guillaume Gateau are with the Institut National Polytechnique de Toulouse, 31030 Toulouse, France (e-mail: meynard@laplace.univ-tlse.fr; gateau@laplace.univ-tlse.fr).

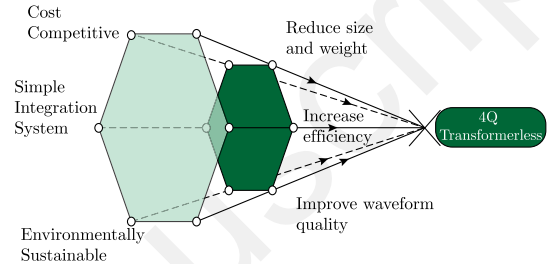


Fig. 1. Benefits of the 4Q transformerless converters using multilevel topologies.

The multilevel converters are widely used as transformerless solutions for MV applications, leading into a lighter, cheaper, and more efficient solution [2]. With the benefits of generating a higher number of levels, the five-level topologies have become more interesting than the traditional three-level topologies. Fig. 1 presents the main motivations of this study with a special focus on four quadrant transformerless applications. From an industrial point of view, the removal of the transformer allows a simple system integration, reducing the converter cost (less copper used, which makes it a more sustainable solution). The other well-known benefits of multilevel converters include improved waveform quality, higher efficiency, and filter size reduction.

This article presents a new multilevel converter topology recently introduced by Nidec ASI. Due to its inherent features, this topology allows a simple integration of commutation cells when the application requires a higher number of levels and a zero-voltage switching operation of the terminal switches. The topology is used for 4.16- and 6.6-kV variable speed drives, working with 5L and 7L structures, respectively.

The rest of this article is organized as follows. The operating principle is explained in Section II. A comprehensive comparison with actual solutions is presented in Section III; experimental results are presented in Section IV, providing an accurate validation of the proposed topology. Finally, the conclusion is given in Section V.

II. PROPOSED TOPOLOGY

The proposed topology, depicted in Fig. 2, can be considered as a series association of two Macro cells, and one external zero-voltage switching (ZVS) selector cell. As can be noted, by connecting in series, these Macro cells nC , the number of levels

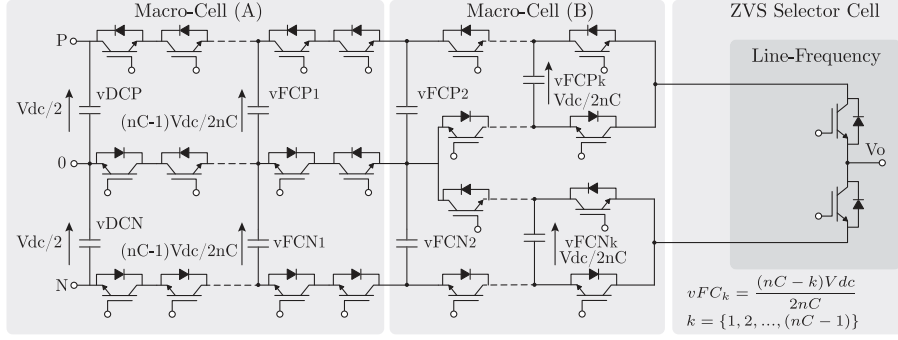


Fig. 2. $(2nC+1)$ -levels proposed topology, where nC is the number of connected cells and k is the number of flying capacitor; $k = \{1, 2, \dots, (nC - 1)\}$.

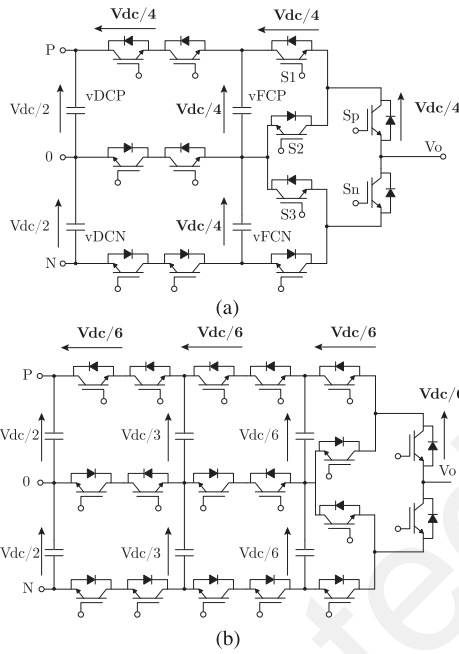


Fig. 3. Proposed topology. (a) 5L configurations to address the 4.16-kV applications. (b) 7L configurations to address the 6.6-kV applications.

Lv increases ($Lv = 2nC + 1$). In addition, also the apparent switching frequency fSw_{app} becomes ($fSw_{app} = nC \cdot fSw$).

Among the advantages of this topology, it is possible to highlight the following.

- 1) Same voltage rating for all the switches, even if the number of level increases.
- 2) The insulated-gate bipolar transistors (IGBTs) in the ZVS cell commute at line-frequency, while the rest of the semiconductors commute at higher frequency only during half of the fundamental period.
- 3) Switches in direct series do not increase by increasing the levels.

For the applications ($U_{rms} = 4.16 \text{ kV} @ V_{dc} = 6.8 \text{ kV}$), the 5L structure shown in Fig. 3(a) is implemented, where the maximum device voltage to block is $V_{dc}/4 = 1.7 \text{ kV}$. On the other hand, for the applications $U_{rms} = 6.6 \text{ kV} @ V_{dc} = 10 \text{ kV}$, the 7L structure shown in Fig. 3(b) is implemented. In this case, the maximum

TABLE I
ALLOWED SWITCHING STATES

Conf	Vo	Sp1	Sn2	S1	S3	Sp
1	Vdc/2	1	1	1	1	1
2	Vdc/4	1	1	0	1	1
3	Vdc/4	0	1	1	1	1
4	0	0	1	0	1	1
5	0	0	1	0	1	0
6	-Vdc/4	0	1	0	0	0
7	-Vdc/4	0	0	0	1	0
8	-Vdc/2	0	0	0	0	0

voltage to block is $V_{dc}/6 = 1.67 \text{ kV}$. It means that using 3.3-kV IGBTs, it is possible to build both configurations, which makes the industrialization process easier. A detailed analysis is presented in the following sections; however, due to article length limitations, only the 5L topology will be discussed in this article.

A. Switching States

Considering the particular case working with a 5L converter, shown in Fig. 3(a), the possible commutation loops are depicted in Fig. 4, and the allowed switching states are listed in Table I. This operation is based on a synchronous commutation in Macro cell A ($Sp1 = Sp1s$ and $Sn1 = Sn1s$), and the complementary signals (e.g., $S2 = \bar{S1}$) are assumed to be well understood. It is possible to see that during a half-period [i.e., Conf. (a)–(d)], IGBTs $Sp1$ – $S1$ commute at a high frequency but IGBTs $Sn2$ – $S3$ remain closed. Additionally, in order to guarantee the ZVS operation, the IGBT Sp commutates naturally once per period and only when $S1 = 0$ and $S3 = 1$, reducing the commutation losses. It can be seen in Fig. 4 during configurations (d) and (e).

B. Modulation

The inherent feature of voltage natural balance in a flying capacitor (FC)-based topology can be achieved with a traditional carrier-based phase-shifted pulsewidth modulation (PS-PWM) technique. The carrier signals between Macro cells A and B cells are shifted by $\pi/2$ degrees, ensuring the natural balance operation. Moreover, during half-period of the fundamental frequency, one of the converter sides (upper/lower) is frozen, while

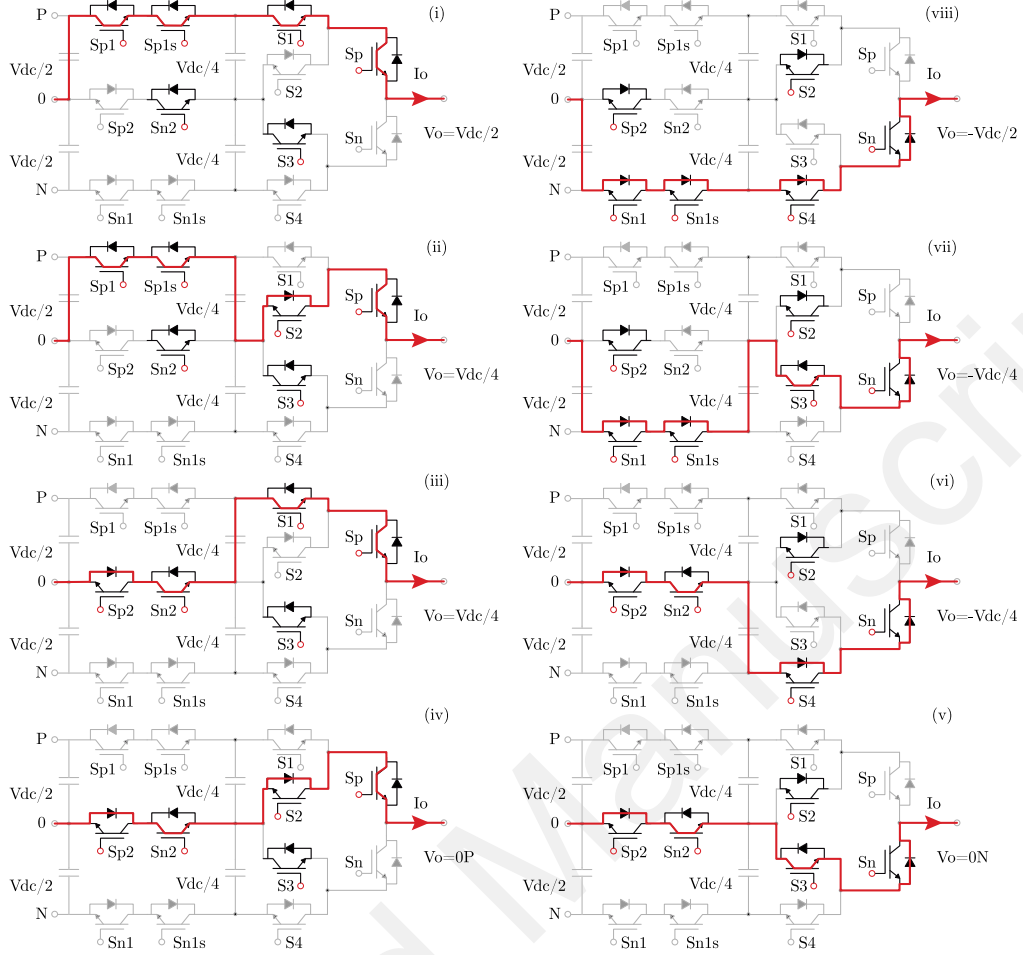


Fig. 4. Positive current commutation during switching transition (P→N); the eight configurations are labeled as (a)–(h).

the another one is commutating. In addition, the IGBTs (SP/SN) commute only once per fundamental period depending on the sign of the modulating signal.

C. Voltage Balance

As was mentioned before, the inherent feature of the multicell FCs-based topologies allows a natural balance using the PS-PWM techniques [4], [5]. However, under certain operation conditions, the voltages could vary among the commutation cells, which could be a risk for the IGBTs if the voltage blocking rate is not high enough ($v_{IGBT} = V_{dc} - v_{FC}$). Therefore, the active voltage balance control shown in Fig. 5(a) is implemented in this proposed topology [6].

The algorithm modifies the modulating signal reference m , depending on the voltage difference (e.g., for positive m -index: $V_{dcP} - v_{FCP}$). The error is corrected with a proportional gain k_{FC} [7]. This parameter increases the speed of the correction and can be defined as

$$k_{FC} = \frac{f_{Sw} \cdot C_{FC} \cdot BW}{2 \cdot f_o \cdot i_{o_{rms}}} \quad (1)$$

where f_{Sw} is the switching frequency, C_{FC} is the capacitance of the FC, BW is the bandwidth expressed in (Hz), and f_o is the output frequency, and i_o is the output current.

The capacitor voltage depends on the current direction; therefore, the sign of the output current is also considered in the algorithm. In order to keep a balanced voltage, the balancing term is added to the modulating signal of one cell (Macro cell A), and subtracted from the another one (Macro cell B). Finally, the modulating reference is modified to work on either positive or negative side of waveform, and send to the PWM scheme. In addition, in order to guarantee a proper dc-link balance, algorithm depicted in Fig. 5(b) is implemented. The algorithm is based on the correction of the modulation index m_{DC} , depending on the sign of the current i_o , and the modulation index m sign. A closed-loop proportional control is required in order to guarantee that the difference between V_{dcP} and V_{dcN} is zero.

III. COMPARISON OF EXISTING TOPOLOGIES

Among the topologies with common dc-link, it is possible to find the solutions listed in Table II.

The most common 3L-VSIs are based on the neutral point clamped (NPC), the active neutral point clamped (ANPC) [8],

TABLE II
TOPOLOGY COMPARISON

Topology	Advantages	Disadvantages
NPC	<ul style="list-style-type: none"> * Low number of switches. * No Flying Capacitors. 	<ul style="list-style-type: none"> * High number of diodes. * Uneven loss distribution among semiconductors. * Not attractive solutions for higher than 3L-VSI. * Excessive number of Flying Capacitors.
FC	<ul style="list-style-type: none"> * Low number of switches * Balanced FC's voltages. * Uniform losses distribution. 	<ul style="list-style-type: none"> * Series association of devices. * High number of switches. * Add a complex switch state sub-sequences to pass (positive \leftrightarrow negative) modulation index. * Large commutation loops at switching frequency. * 4 switches composed by $\frac{(Lv-1)}{2}$ elements in series.
SMC	<ul style="list-style-type: none"> * Low number of Flying Capacitors. 	<ul style="list-style-type: none"> * Series association of devices. * High number of switches. * Add a complex switch state sub-sequences to pass (positive \leftrightarrow negative) modulation index. * Large commutation loops at switching frequency. * 4 switches composed by $\frac{(Lv-1)}{2}$ elements in series.
NL-ANPC	<ul style="list-style-type: none"> * Low number of Flying Capacitors. 	<ul style="list-style-type: none"> * Series association of devices. * High number of switches. * Add a complex switch state sub-sequences to pass (positive \leftrightarrow negative) modulation index. * Large commutation loops at switching frequency. * 4 switches composed by $\frac{(Lv-1)}{2}$ elements in series.
DFC-ANPC	<ul style="list-style-type: none"> * No extra sub-sequences to pass (P \leftrightarrow N). * Natural ZVS for IGBT's in Selector Cell. * Short commutation loops at switching frequency. 	<ul style="list-style-type: none"> * Higher number of Flying Capacitors. * 2 switches composed by $\frac{(Lv-1)}{2}$ elements in series.
Proposed Topology	<ul style="list-style-type: none"> * No extra sub-sequences to pass (P \leftrightarrow N). * Natural ZVS for IGBT's in Selector Cell. * Reduced blocking voltage during commutation in Macro-Cell (A). * Short commutation loops at switching frequency. * Switches in series do not increase by increasing the levels. 	<ul style="list-style-type: none"> * Higher number of Flying Capacitors. * Macro-Cell (A) composed by 2 element in series.

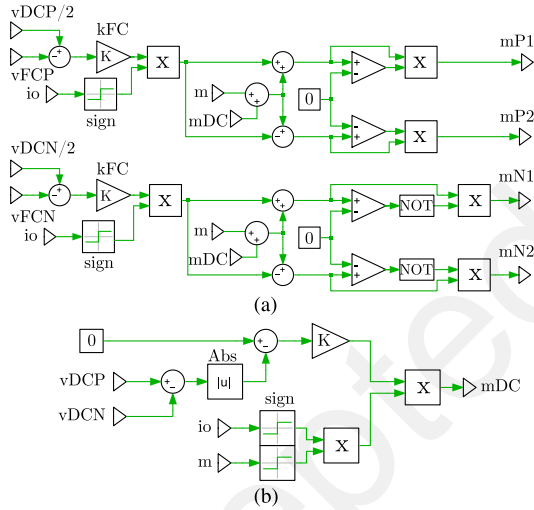


Fig. 5. Voltage balance algorithms. (a) FC voltage balance algorithm for the proposed 5L converter; positive side (upper) and negative side (lower). (b) DC-link voltage balance algorithm.

and the flying capacitor [9] topology. These topologies work with a common dc-bus, which allows a simple integration of the converter in case of a four-quadrant type; the same converter can be connected back-to-back fulfilling the functionalities like power factor correction, voltage support, and improved quality waveforms. However, the high number of switches and high number of common points at the dc-link make multilevel-ANPC topology an unattractive solution for MV converter [10]. On the other hand, the FC has an excessive number of capacitors, which is its main disadvantage, because they are expensive, less reliable, and require maintenance and replacement [1], [11], [12].

In order to reduce the stored energy of the converter, the SMC topology was proposed. It is mainly a hybrid association of FC-based commutation cells, which allows an improved performance in terms of number of levels and switching frequency [13]. However, this topology needs a series association of devices, which is not attractive for higher levels. In order to overcome the issues coming from the large amount of storage elements, some solutions reducing the number of active switches [14], or using hybrid series association with non FCs-based cells [15] are found in the state of the art.

In [16], a new topology has been proposed (NL-ANPC), which has been industrialized as a 5L structure for MV drives (5L-ANPC) [17]. It can be seen as a ANPC cell in series with a two-level cell. This structure allows increasing the number of levels by connecting in cascade the two-level cells. However, in order to maintain the same voltage rating for all switches, it is mandatory to add more devices in series in the ANPC cell. It can be seen as a drawback in case of increasing the number of levels as the case of the 7L-ANPC. In addition, a special subsequence is needed at the zero-voltage crossing, which increases the complexity of the control system. Based on the same general structure, another topology named as DFC-ANPC has been studied in [18]. This solution presents advantages in contrast with the 5L-ANPC, because the series-connected devices are commuted at ZVS. However, this solution requires higher number of capacitors compared with the industrialized solution.

The proposed topology requires the same number of switches per phase leg, compared with SMC, NL-ANPC, and DFC-ANPC (12 for 5L and 18 for 7L structures). The selector cell works at line frequency and ZVS, which is naturally achieved when the modulation index passes from positive to negative. Due to the inherent feature, no additional devices in series are required when the number of level increases. The maximum number of

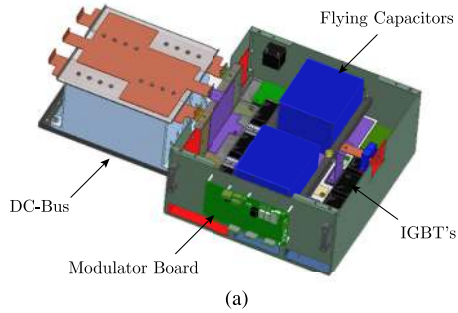


Fig. 6. Experimental test-bench. (a) Three-dimensional CAD image of the power module. (b) Silvert-FH (Nidec ASI).

TABLE III
PARAMETERS OF THE EXPERIMENTAL TEST-BENCH

Parameter	Value
Rated power	1.5 MW
DC-link voltage	5800 V
DC capacitance	300 μ F
FC capacitance	900 μ F
Switching frequency	976 Hz
IGBT (FF450R33T3E3)	3.3 kV @ 450 A

devices in series are 2, in contrast with the NL-ANPC and DFC-ANPC where the devices in series are $\frac{(Lv-1)}{2}$, depending on the number of voltage levels Lv . The number of capacitors is higher than the NL-ANPC, but they are used only 50% of the time, which reduces their RMS current and self-heating. This rms current is in particular much smaller than that of the single capacitor of the NL-ANPC topology.

IV. EXPERIMENTAL VALIDATION

The experimental power module built in the Nidec ASI is depicted in Fig. 6. The 3D CAD image is shown in the upper figure, where the components' position is clearly identified. Moreover, the complete back-to-back prototype is shown in the lower figure, where it is possible to see the six power modules. The rated values of the experimental test-bench are listed in Table III. It is important to clarify that during the experimental

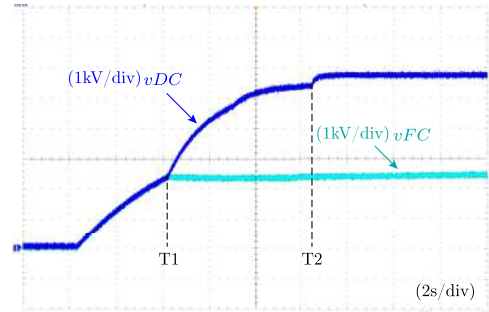


Fig. 7. Voltages of the active precharge.

validation, several tests were carried out at different operating points, so that they were performed during different phases of the prototyping validation previous the industrialization.

The capacitors are sized in order to allow a voltage ripple lower than $\Delta V_{\max} \leq 10\%v_{FC}$, and a maximum output current I_{rms}

$$C_{FC} = \frac{\sqrt{2}I_{\text{rms}}}{nC fSw \Delta V_{\max}}. \quad (2)$$

A. Capacitor Voltage Precharge

The precharge procedure brings the capacitor voltages to their rated values. In practice, the converter needs an auxiliary circuit (precharging unit) connected in parallel to the dc bus, feeding the capacitors banks during the start-up procedure [19]. While the rated dc voltage is different from rated FC's voltages, an appropriate start-up procedure is necessary for charging all the capacitors installed in the converter. It consists mainly in two phases and two configurations of IGBTs, as depicted in Fig. 7.

1) ($0 < t < T1$): In this phase, the external IGBTs of the Macro cell A are saturated ($Sp1/Sp1s = 1$), in order to put in parallel dc bus ($Vdc = VdcP + VdcN$) and FC bus ($vFC = vFCP + vFCN$) with the precharging unit. In this phase, the time constant depends on the parallel of two capacitors (C_{DC} and C_{FC}). It ends when the voltage reaches the FC's rated value ($vFC = Vdc/2$).

2) ($T1 < t < T2$): In this phase, the external IGBTs of Macro cell A are open ($Sp1/Sp1s = 0$), in order to maintain in parallel only the dc bus with the precharging unit. In this phase, the time constant depends on the dc capacitance. It ends when the voltage reaches the dc bus rated value. After $T2$, the start-up procedure is finished, and it is possible to initialize the converter with all the capacitor voltages at the desired values.

B. ZVS Selector Cell

Fig. 8 depicts the the zero voltage switching on the selector cell. It shows the switching commands for the IGBTs (S2, S3, and Sp). The commutation of the IGBT Sp/Sn always happens when the voltage across IGBT is zero. It means that, the IGBT's S2 and S3 are in ON state during SP commutation. The picture shows the historical commands registered for each passage from negative to positive of the modulation index.

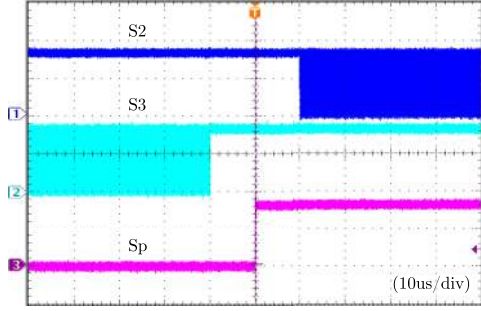


Fig. 8. Switching commands for the IGBTs S2–S3–SP.

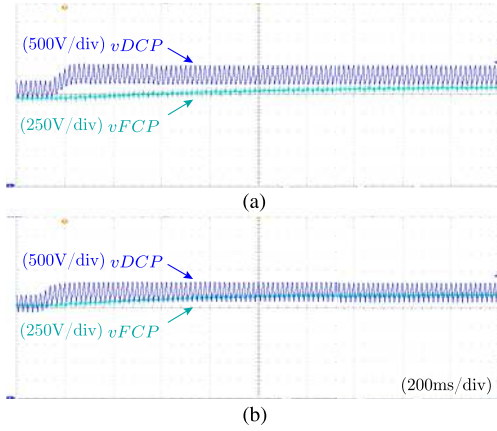


Fig. 9. Experimental results of the voltage balance algorithm. (a) Without balancing algorithm. (b) With balancing algorithm $k_{FC} = 60e-6$.

C. Voltage Balance

The objective of this experimental test is to see the behavior of the flying capacitor algorithm depicted in Fig. 5. In this case, a three-phase diode bridge rectifier is connected to grid for generating a fixed dc bus voltage. As was explained before, the proposed converter has an inherent voltage balance feature. However, its dynamic could be slow that it causes considerable voltage unbalances on the FCs. This effect is shown in Fig. 9(a), where a unbalance is imposed on the dc bus capacitor V_{dCP} . It is possible to see that the voltage tends to follow the dc bus voltage with a slow dynamic. On the other hand, Fig. 9(a) shows the same experiment with the balancing algorithm enable and a bandwidth $BW = 1.5$ Hz ($k_{FC} = 60e-6$). It is possible to see that the balance speed increases, and the time to reach the reference is lower than 700 ms. The voltage ripple on the dc capacitances is due to the diode rectifier, and depends on the load working conditions.

D. Output Voltage

The test bench circuit developed for this test is depicted in Fig. 10(a). The rectifier unit imposes the total dc bus voltage, and the load is an RL circuit. Based on the the parameters used for the test-bench, the power factor is $PF \approx 0.95$. Initially, in order to validate the proposed concept in a reduced power prototype, the values were modified from the rated power. The total dc voltage

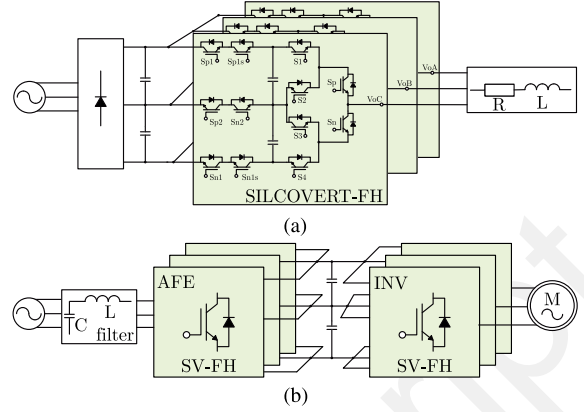


Fig. 10. Circuit diagram of the experimental test bench. (a) Inverter with RL load used for the experimental validation of voltage-balancing algorithm and output levels. (b) Back-to-back configuration used for experimental validation of the motor operation.

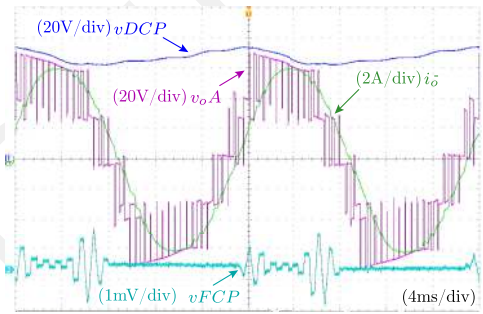


Fig. 11. Experimental voltage and current measurements of the 5L-proposed topology using a RL load. v_o : phase voltages. i_o : output current.

is equal to 120 V, and the FCs voltage is 30 V. Moreover, the modulation index is imposed equal to $m = 0.9$ at 50 Hz. The converter works with a switching frequency of $f_{sw} = 976$ Hz. The output load is a RL circuit with the values ($R = 10\ \Omega$ and $L = 10$ mH), and the results are depicted in Fig. 11.

The figure shows the output phase voltage, where the 5L are clearly depicted, and the output current which corresponds to the connected load. Moreover, one of the flying capacitor voltages v_{FCP} is also depicted in this figure. During half of the period, the voltage is constant because the cell is not commuting, and during the other half, the voltage oscillates around the desired value. This operation could lead to a voltage unbalance of the FC voltages; therefore, the active voltage balance was implemented.

E. Motor Operation

The experimental setup implemented on this test is depicted in Fig. 10(b). The converter is evaluated in four-quadrant operation using an induction motor. The dc voltage is imposed by the active front end (AFE), and the voltage and speed control of the motor is regulated by the inverter. The induction motor has a rated voltage of $U_m = 3.3$ kV at $f = 50$ Hz with four poles, and the test has been conducted with no mechanical load. Therefore, the

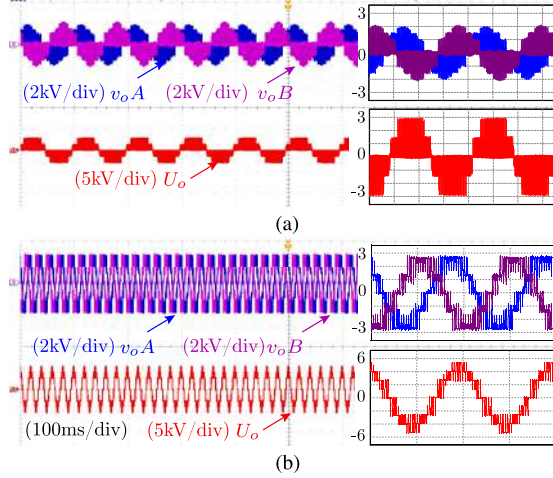


Fig. 12. Motor operation with V/f control. (a) Output frequency at 10 Hz. (b) Output frequency at 50 Hz. v_o : phase voltages. U_o : phase-phase voltages.

current obtained during this test is negligible compared with the nominal current of the converter.

In order to carry out the test, the control of the inverter side works following the standard volts/hertz control scheme [20]. Therefore, the voltage imposed on the motor depends linearly with the frequency or the speed. In this evaluated case, at $f = 50$ Hz (1489 r/min), and the rated voltage considered of the motor is $U_m = 3.3$ kV. In order to validate the motor operation, two different frequencies are depicted in Fig. 12. The operation at 10 Hz is clearly shown in Fig. 12(a); the modulation index is low following the V/f characteristic; thus, the number of levels is lower than the rated operation. In addition, the operation at nominal frequency 50 Hz is depicted in Fig. 12(b); the result shows the 5L on the phase voltage v_o and the 9L on the phase-phase voltages U_o .

F. Harmonic Evaluation

For a brief evaluation of the converter performance during the motor operation, an analysis of the voltage total harmonic distortion (THDV) has been evaluated. As already mentioned, the constant V/Hz profile imposed on the motor permits to perform the THD calculation at different output voltages by varying linearly the output frequency. The results of the voltage spectrum at 10 and 50 Hz are depicted in Fig. 13.

It is well known that the third harmonic injection allows a better utilization of the dc-bus voltage, and extensively used in grid-connected inverters. However, in motor operation, the dc-bus voltage is highly enough to operate the motor. Therefore, for the motor operation, the zero sequence injection is not introduced, leading to a lower THDV at the fundamental output voltage U_o , as depicted in Fig. 14.

G. Conversion Efficiency

In order to estimate the converter efficiency, and due to experimental facilities, only simulation tests are performed for the rated operating values ($S = 1.5$ MVA, $I_o = 208$ Arms,

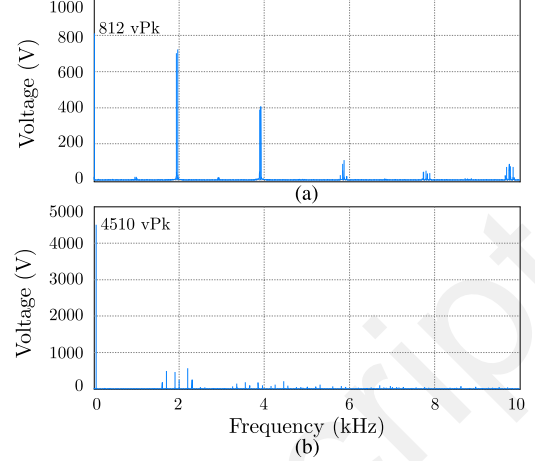


Fig. 13. Voltage harmonic spectrum. (a) Output frequency at 10 Hz. (b) Output frequency at 50 Hz.

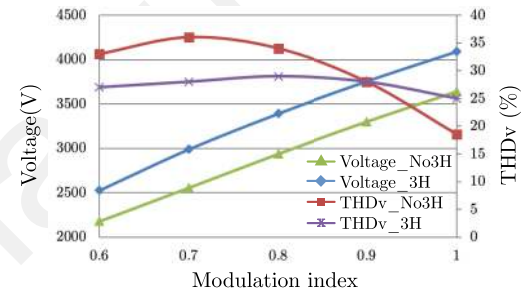


Fig. 14. Output voltage U_o , and THDV related to the modulation index with (blue, violet) and without (green, red) third harmonic injection.

$E = 7$ kV, $m_{\max} = 1.14$). In these tests, the selected devices are the IGBTs Infineon (FF450R33T3T3 3.3kV@450 A). The losses are calculated based on the thermal model using the information from the datasheets. In addition, a constant loss $P_{aux_{\text{loss}}} = 0.015\%$ of the rated power is considered, which represents the inductance iron and auxiliary losses.

The efficiency results working as inverter (motor operation) are depicted in Fig. 15(a). We consider two power factors for the test [PF = (0.8 and 1)], and due to the V/f control, a variation of the modulation depth is made between 5% and 100%. It is possible to see that the highest efficiency is obtained for a PF = 1 and the highest modulation depth. The efficiency results working as AFE operation are depicted in Fig. 15(b). We consider two modulation depths (80% and 100%), so that in this case, a constant V control is used. For this evaluation, a power variation is made between 5% and 100% of the rated power. It is possible to see that the highest efficiency is obtained at maximum power and the highest modulation depth. Moreover, due to the constant losses $P_{aux_{\text{loss}}}$, the efficiency at low power $< 15\%$ tends to decrease. Finally, in order to estimate the global efficiency at four-quadrant operation, we multiply the efficiencies of both operation modes. As can be seen in Fig. 15(c), when the AFE operates at modulation depth = 1 and the inverter working at PF = 1, the highest efficiency $\approx 98.8\%$ is obtained.

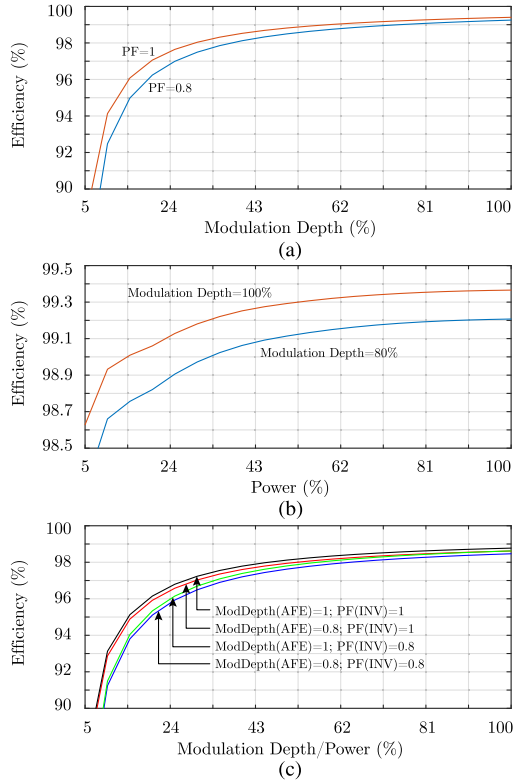


Fig. 15. Efficiency results. (a) Motor operation. (b) AFE operation. (c) Global efficiency.

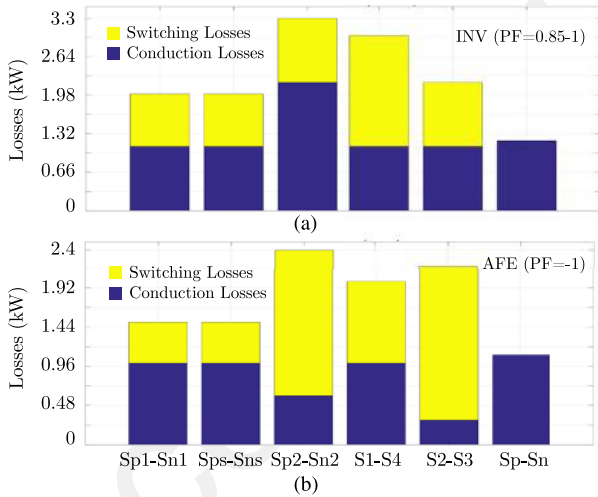


Fig. 16. Maximum conversion losses. (a) Inverter/motor operation at (PF = 0.85→1). (b) AFE operation (PF = -1).

In order to understand the losses distribution, we obtain the maximum losses when the converter operates as AFE and motor [PF = (0.8→1)], respectively. The results are depicted in Fig. 16, where the conversion losses are calculated for the pair of IGBTs operating in the same way. It is worth noticing some important aspects: first, the higher losses are found in the pair of semiconductors (Sp2 and Sn2), so that they conduct the current in the positive and negative sides of the waveform. Then, due to the

ZVS operation of the selector cell, it only presents conduction losses. Finally, the series IGBTs in Macro cell A (Sp1 and Sps1) and (Sn1 and Sns1) switch in a synchronous way. Therefore, it is possible to see that the losses are evenly distributed.

V. CONCLUSION

This article presents a novel transformerless multilevel converter topology for MV applications. The topology is composed by the series association of two macro cells, which can be extended in order to increase the number of output levels, and maintain the same voltage rating on all the switches. In addition, one external selector cell allows zero voltage switching of the terminal selector when transitioning from positive to negative voltage. Among the advantages, the voltage rating and the number of devices connected in series may remain the same for 4.16- and 6.6-kV applications, by using, respectively, the 5L and 7L configurations, and this is a key feature from the industrialization point of view. The converter operation is based on blocking half of the converter during the semi-period of the fundamental waveform, while the other part of the converter is switching. This operation could lead to a voltage unbalance of the FC voltages; therefore, an active voltage balance is implemented. The experimental test validates the correct operation of the converter testing it in different scenarios including active front end and inverter operations. Finally, simulations provide an estimation of losses and efficiency.

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