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Novel Multirate Modulator for High Bandwidth Multicell Converters

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Abstract- Series and parallel multicell converters have been introduced because they provide benefits in term of efficiency and power density. However, they also allow reducing the amount of energy stored in the filters, which potentially allows for faster dynamic responses. Interleaving the control patterns of different cells is another distinctive feature of these converters and is also the root of another potential improvement of the dynamic response: with one PWM update at each subcycle of the switching period, a n-cell converter may change its average output voltage over each of these intervals, while standard converters can only control the voltage over half the switching period. In this paper, a general multirate modulation strategy taking advantage of this property, while avoiding overswitching, and compatible with any n-cell converter is proposed and validated by simulation and experimental results.

I. INTRODUCTION

In recent years, several topologies of converters have been reported in the literature to improve their performances, especially efficiency and power density. Among them, there are multilevel converters with some characteristic features [1], [2]:

- 1) they include several commutation cells, which are the building blocks of the converters;
- 2) the two-level chopped voltage and/or current waveforms of the different cells are added in the circuit to form voltage and/or current waveforms with more levels;
- 3) the control pattern can be interleaved to optimize the output total waveform;
- 4) the filters take advantage of these improved waveforms; storing less energy, they can be smaller than those of classical two-level converters.

Such multilevel converters are employed in a myriad of applications such as HVDC transmission and distribution, energy storage systems and electric vehicles as well as in the naval and aerospace industries [1], [3]–[7]. This wide range of end-uses imply in different requirements for each deployment of the technology. Thus, numerous converter configurations exist [8]–[13], as the well-known neutral point clamped (NPC) [14], the flying capacitor (FC) [15] and the cascaded H-bridge [16] topologies and others as the clamp-double [17] and double-zero [18] converters, each with its particularities.

Furthermore, many applications of multilevel converters may demand or benefit from a faster transient response and a broader stability margin [19]. There are many techniques to achieve fast transient response depending on the application and converter topology. A fast control can be obtained, for example, with analog control without microcontrollers if the electronic circuits are designed to include all structures (converter and control system) [20], [21]. This is better suited for simpler topologies such as buck converters or low power applications [22].

In [23] it is shown that, for the same perceived switched frequency, a multilevel converter can be faster and more stable than its two-level counterpart due to a reduced output filter. Another way to reach better transient response in the control of power converters is to use non-linear techniques instead of the classical linear approach, such as: predictive control [24]–[26], geometric control [27], adaptive control [28], [29], etc. These techniques however come at the expense of increased computational burden, which is still a limitation especially for high frequency applications. Therefore, classical controls are still widely used since they are simple and easy to implement.

Other important aspect of control systems in multilevel converters is the use of distributed control. In applications with high number of switches, the distributed structure is usually adopted due to the impossibility to control all converters cells using a single processor. Thus, a multirate sampling approach is beneficial to implement all control strategies [30]–[32].

Another important subject related to dynamics in multilevel converters is the modulation technique, since decreasing the modulator delay is one way to enhance the control performance [32], [33]. Two classical carrier-based modulation techniques are the Symmetrically Sampled PWM (SS-PWM) and the Asymmetrically Sampled PWM (AS-PWM). These are based in sampling the control quantities and updating the duty cycle of each individual cell in specific moments of the carrier wave. This is done once per cycle for the SS-PWM and twice per cycle for the AS-PWM. However, this sampling and updating limitation deteriorates modulator performance [32]–[34].

To prevent this, the Naturally Sampled PWM (NS-PWM) can be used [35]. This modulator updates the duty cycles of all cells at the same time whenever sampling occurs. Moreover, it is shown in [32] that this modulator is suitable for decentralized control structures, since using it allows the separation of switching, sampling and control frequencies, minimizing control and sampling time and allowing for an overall better control performance in low frequency multilevel converters.

Nevertheless, overswitching (multiple switching pulses per carrier cycle) may incur while using the NS-PWM since each cell can change its duty cycle at any moment. These extra pulses must be avoided since they generate extra losses and EMI problems. Although there are ways to eliminate this via hardware, the Multirate Symmetrically Sampled and Multirate Asymmetrically Sampled modulators (which will be referred to as MSS-PWM and MAS-PWM, respectively) proposed in this paper present a software implemented solution that select which cell can change its state without provoking overswitching. This novel multirate modulator is not dependent of the control strategy nor the multicell converter configuration, i.e., it is generalized for any number of cells in series and/or in parallel.

- 1) they can be used to build DC/DC or DC/AC (as depicted in Fig. 1(a) and Fig. 1(b) and, respectively) converters with any number of cells;
- 2) they can be combined to form series-parallel converters (in Fig. 1(a), S_{Hi} and S_{Li} form cell i , with $i = 1, \dots, 6$; cells 1 to 3 form a series three-cell inverter leg and cells 1 to 6 form a 3x2 series-parallel multicell inverter leg);
- 3) they are convenient to illustrate how some principles are common to series and parallel types and also to point out some differences.

The aim of this paper is to better understand the dynamic performance of series and parallel multicell converters by identifying their physical limits, showing how they can be maximized and comparing results obtained with different numbers of cells. In order to ensure fair comparison between the converters, three rules discussed along the text are followed:

- 1) no overswitching is allowed (a switching cell must never undergo more than one ON-OFF in a switching period);
- 2) the output filters of converters with different numbers of cells are designed according to the same criteria, since the filter values obviously affect dynamic performances;
- 3) the control is adjusted in such way that the fastest response is reached without control saturation.

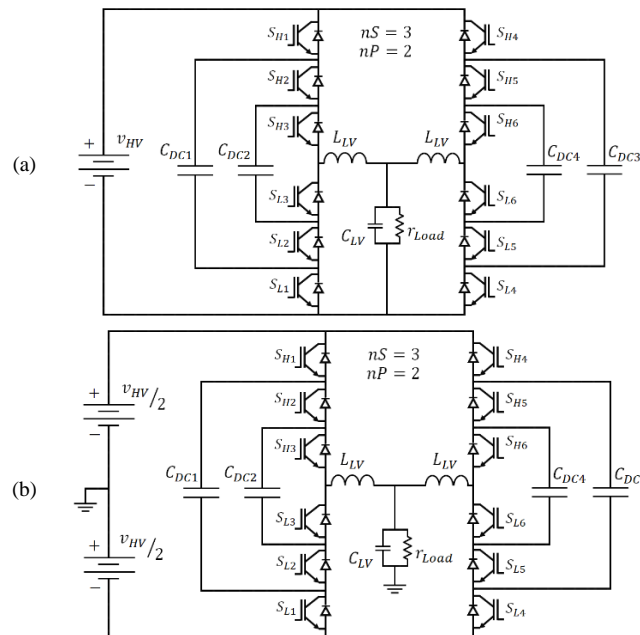


Fig. 1 a) DC/DC series-parallel multicell converter (2 parallel, 3 series) and (b) DC/AC series-parallel multicell converter (2 parallel, 3 series).

The two main contributions of this paper are:

- 1) firstly and mainly, the introduction of a multirate modulation strategy that allows fast duty cycles changes while avoiding overswitching via software and that is more resilient to filter parameter deviation;
- 2) secondly, a better understanding of the influence of the number and configuration of cells in the filter design and control dynamic behavior.

The superior performance of the proposed multirate method is demonstrated in simulations using the PLECS platform, and the impact of the number of cells on the system response is evaluated for parallel converters. The results are validated using an experimental prototype of a DC/DC three-cell converter.

The paper is organized as follows: Section II describes the filter design principles for series and parallel converters, Section III draws the physical performance limit of such converters, Section IV presents the control strategy employed, Section V describe the classical modulation and the proposed method, Section VI shows the simulation and experimental results, and finally in Section VII the conclusions are presented.

II. FILTER DESIGN FOR MULTICELL CONVERTERS

Filter design is not an easy task and it is not the main aim of this paper, so the development carried out here will be kept as simple as possible. Still, it is necessary to identify simple design rules and always apply them in such way that direct comparison can be done to identify the inherent differences of using different numbers of cells in series and/or in parallel.

Firstly, equations that govern the inductor current ripple and the capacitor voltage ripple in DC-DC converter structures as the one in Fig. 1(a) are derived, then it is discussed how these ripples influences the design of the filter. Finally, it is shown how the filter obeying chosen rules evolves with the number of cells in series and in parallel.

A. Inductor Current Ripple

The voltage delivered at the output of a series (s) multicell converter with n_s cells in series and interleaved control (control patterns of the different cells identical but phase-shifted by $2\pi/n_s$) is a square voltage waveform with an amplitude V_{HV}/n_s and an apparent frequency $n_s \cdot f_{sw}$ (where f_{sw} is the switching frequency). In consequence, the inductor current ripple is given by [36]

$$\Delta I_{pkpk} = V_{HV} / (4 \cdot L_f \cdot f_{sw} \cdot n_s^2), \quad (1)$$

where ΔI_{pkpk} is the current ripple peak-to-peak value, V_{HV} is the voltage in the high voltage side of the converter (input) and L_f is the equivalent filter inductor (low voltage side).

In a parallel (p) multicell converter with n_p cells in parallel, each inductor sees only a fraction of the current, but the voltage applied is the same as for a two-level converter. To maintain the normalized ripple in each L_{LV} inductor ($\Delta I_{pkpk}^{cell,N}$), it is needed

$$\Delta I_{pkpk}^{cell,N} (I_{LV}/n_p) = V_{HV} / (4 \cdot L_{LV} \cdot f_{sw}), \quad (2)$$

where L_{LV} is the cell filter inductor. Using an interleaved modulation, the current ripple will be partially compensated [37], resulting in a ripple of the total current divided by n_p

$$\begin{aligned} \Delta I_{pkpk}^{total} &= \Delta I_{pkpk}^{cell,N} (I_{LV}/n_p) / n_p \\ &= V_{HV} / (4 \cdot L_{LV} \cdot f_{sw}) / n_p, \end{aligned} \quad (3)$$

which can be rewritten as

$$\Delta I_{pkpk}^{total} = V_{HV} / [4 \cdot (L_{LV}/n_p) \cdot f_{sw} \cdot n_p^2], \quad (4)$$

where L_{LV}/n_p is the inductance equivalent to the cell inductances in parallel. Comparing Eq. 1 and Eq. 4, it is seen that the total current ripple of the series and parallel multicell converters can be described with a unified equation involving the equivalent output inductance and the total number of cells, no matter if they are in series, parallel or even in series-parallel

$$\Delta I_{pkpk}^{total} = V_{HV} / (4 \cdot L_f \cdot f_{sw} \cdot n_{cell}^2), \quad (5)$$

$$L_f = L_{LV}/n_p, \quad (6)$$

$$n_{cell} = n_s \cdot n_p. \quad (7)$$

B. Capacitor Voltage Ripple

The inductor ripple current is assumed to flow into the capacitor and it provokes the voltage ripple. Keeping in mind that the frequency of the current ripple in the series, the parallel and the series-parallel multicell converter is always $n_{cell} \cdot f_{sw}$ when the control signals are appropriately interleaved, for all three cases the voltage ripple is [36]

$$\Delta V_{pkpk} = \Delta I_{pkpk}^{total} / (8 \cdot C_{LV} \cdot n_{cell} \cdot f_{sw}), \quad (8)$$

where C_{LV} is the filter capacitor.

C. Filter Design

The inductor of a 2nd order low voltage side filter is generally bigger and more expensive than the capacitor and it also generates more losses. All these reasons push the designer to try to minimize the inductor size and this process may result of various complicated tradeoffs. However, as a first approach, it can be considered that $L \cdot I_{pk} \cdot I_{rms}$ is an acceptable indication of the size of the inductor [38], [39]. Very high inductance values result in almost no ripple, but also very big inductors (high energy, $L \cdot I_{dc}^2$). However, very low inductance values would also result in very big inductors, because of high peak and RMS currents. This means that, in practice, the filter inductors are neither chosen based on filtering criteria nor on dynamic performances; their value is chosen to try to minimize their weight, cost and/or losses. A first rule of thumb is to choose the maximum normalized current ripple ΔI_{pkpk}^N and, for the case of a series-parallel converter, through Eq. 5 yields

$$L_{LV} = V_{HV} / (4 \cdot \Delta I_{pkpk}^N \cdot I_{LV}/n_p \cdot f_{sw}) / n_s^2, \quad (9)$$

which combined to Eq. 6, 7 and 8 gives

$$C_{LV} = \left(\frac{I_{LV}}{V_{HV}} \right) \cdot (\Delta I_{pkpk}^N / \Delta V_{pkpk}^N) / (8 \cdot f_{sw} \cdot n_s \cdot n_p^3), \quad (10)$$

where ΔV_{pkpk}^N is the normalized voltage ripple. In this work, these equations are used to design the filters and impose current and voltage ripples of $\Delta I_{pkpk}^N = 30\%$ and $\Delta V_{pkpk}^N = 0.5\%$.

Notably, the constraint in the parallel converter is the current ripple in each leg (cell). Designing the maximum ripple in the cell, the output current ripple will be smaller, and the capacitor will be designed for this ripple. For the series converter, the constraint is directly the output current ripple thus the capacitor will be bigger to keep the maximum voltage ripple.

D. Filter Calculation with the Number of Cells

By these rules, filters for multicell converters are easily designed, and the similarities/differences of series/parallel converters can be better understood. Table I gives the 2nd order filter characteristic values for both topologies using the value of ripple previously mentioned, and considering a converter input voltage $V_{HV} = 100V$, maximum output current $I_{LV} = 20A$ and switching frequency $f_{sw} = 20kHz$. These parameters are used throughout this work for simulation and experimental results.

III. DYNAMIC PERFORMANCES AND PHYSICAL LIMITS FOR MULTICELL CONVERTERS

The general trend is that increasing the number of cells allows increasing the cutoff frequency of the filter, so it must be possible to increase the dynamic performances. Before getting into more details about the control strategy that respects all the requirements of a feasible power converter with as fast as possible time response, a study of the physical limits of large-scale response time resulting of the fixed DC voltage is first developed. This limit is in fact relative and it will be used later to compare with the result of the proposed modulation strategy.

State plane analysis is a convenient tool to study the evolution of second order filters, and it will be first analyzed the simplest case, i.e., a step of the reference from 0% to 100% without any load. It is easy to understand that the voltage to be applied for fastest response is 100% for a first time interval T_1 , to deliver as much energy as possible to the filter, then 0% for second time interval T_2 , to avoid voltage overshoot and allow current to reach zero at the time that the voltage reaches 100%; at this time the applied voltage must become 100% again to maintain the output voltage at the targeted value.

This process requires perfect timing, but in this specific undamped case, the trajectories are perfect circles and, since the angles in the state plane translate to fractions of the natural frequency, it can be seen from Fig. 2 that the minimal time response is 1/3 of the natural frequency. This principle can be generalized to a more realistic case, i.e., a loaded converter. The centers of the circles are now along a line with a slope imposed by the value of the load, and the trajectories are now logarithmic spirals that makes analytic calculation much more difficult (see Fig. 3).

It is however possible to find numerically the values of T_1 and T_2 corresponding to this case, using the following process:

TABLE I
FILTER PARAMETERS: $V_{HV} = 100V$, $I_{LV} = 20A$, $f_{sw} = 20kHz$
(SERIES “s” AND PARALLEL “p” CONVERTER CONFIGURATIONS)

	n_{cell}	1	2	3	4	5	6	7
C_{LV} (μF)	p	75	9.3	2.8	1.17	0.6	0.35	0.2
	s	75	37.5	25	18.75	15	12.5	10.7
L_{LV} (μH)	p	208	416	625	833	1041	1250	1458
	s	208	52	23.1	13	8.3	5.8	4.2

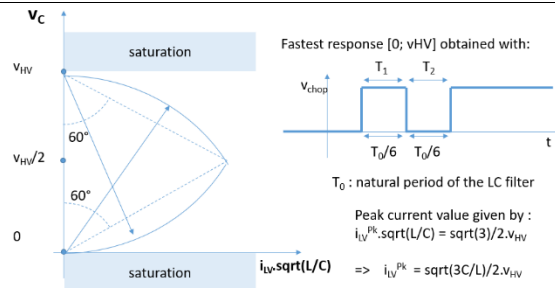


Fig. 2 Optimal response at no-load.

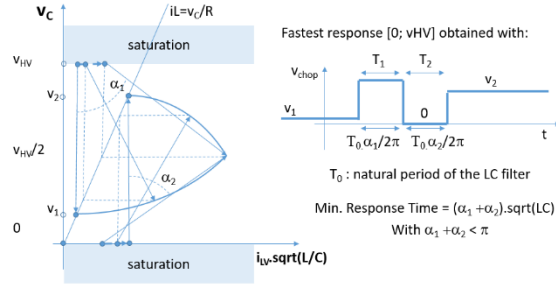


Fig. 3 Optimal response of loaded converter.

- 1) write the model equations as functions of applied voltage, filter parameters and load;
- 2) impose initial conditions of point *A* and find first trajectory with full applied voltage;
- 3) impose final conditions of point *B* and find second trajectory by reverse simulation with zero applied voltage (reverse means a negative step at each iteration);
- 4) find intersection of the two trajectories, times T_1 and T_2 .

Using this method and considering the previously calculated filter parameters, Table II presents the optimal time responses as a function of the switching period (t_{sw}) of the loaded series and parallel converters for $r_{Load} = 5 \Omega$ (rated load resistance). It is seen that the response varies with the number of cells and with the series and parallel structures.

The simulation results for a parallel converter as the one from Fig. 4 with $n_{cell} = 3$ and $r_{Load} = 5 \Omega$ are shown in Fig. 5.

TABLE II
OPTIMAL TIME RESPONSE (MULTIPLES OF t_{sw}): $V_{HV} = 100V$,
 $I_{LV} = 20A$, $f_{sw} = 20kHz$ AND RATED $r_{Load} = 5\Omega$
(SERIES “s” AND PARALLEL “p” CONVERTER CONFIGURATIONS)

n_{cell}	1	2	3	4	5	6	7
p	5.0	1.98	1.55	1.6	1.76	1.79	1.80
s	5.0	1.75	0.95	0.61	0.44	0.33	0.26

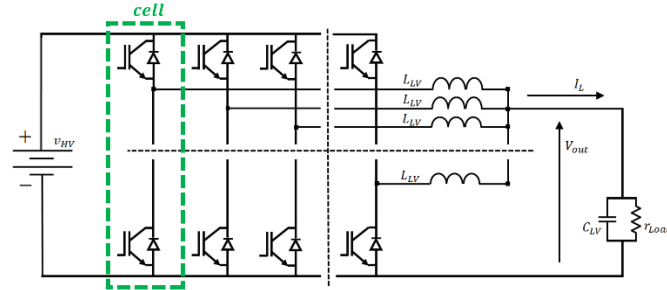


Fig. 4 Generic n_{cell} parallel converter.

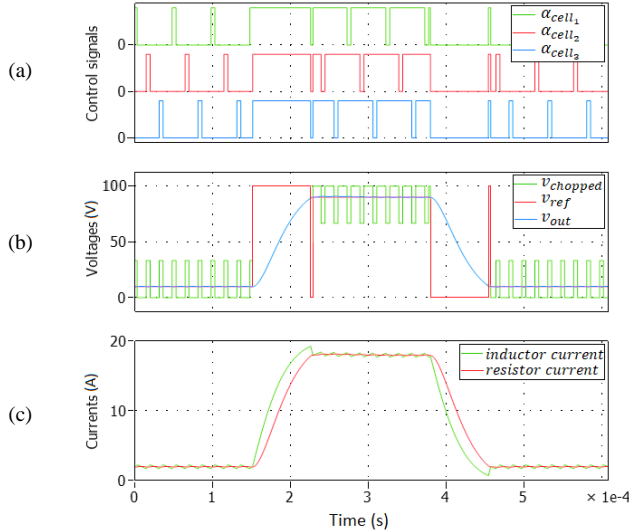


Fig. 5 Optimal response of the output filter designed for a three-cell parallel converter with $r_{Load} = 5 \Omega$: (a) command signals, (b) reference voltage, cell voltage,

output voltage and (c) cell current (inductor), output current (load).

From Fig. 5, the response time is $1.55 \cdot t_{sw} = 77.54\mu s$ for a voltage output step on the loaded converter, value that is in close agreement with the one shown in Table II. Despite giving the “optimal response”, calculating T_1 and T_2 is not trivial and, thus, it is hard to implement in a microprocessor for the control of multicell converters.

These trajectories and minimum response times are ideal optima that do not respect most limitations of practical setups (i. e. they represent theoretical physical limits). These will be used as comparison references, since they cannot be achieved by practical converters with sampling, delays, etc.

IV. CLOSED LOOP CONTROL OF OUTPUT VOLTAGE IN MULTICELL CONVERTERS

A. Inductor Current Ripple

As demonstrated previously, an appropriate filter design allows taking advantage of the multicell topologies to reduce the output filter size. In the same way, increasing the number of cells favor higher filter cutoff frequencies, implying that faster dynamics could be expected. In contrast, seeking high bandwidth for the output voltage requires a system modeling with focus on specific points related to the control performances, including the modulator.

The equivalent filter model on Fig. 6 can be used for modeling the filter in series or parallel multicell converters. The output voltage V_{OUT} depends on the filter parameters and on the common mode voltage V_{CM} provided by the converter. The filter includes the equivalent inductor L_f (and its equivalent winding resistance r_{Lf}), the capacitor C_{LV} and the load r_{Load} .

Whatever the converter topology, $V_{CM}(t)$ could be expressed as a composition of the single cell voltage contributions

$$V_{CM}(t) = \frac{V_{HV}}{n_{cell}} \sum_i^{n_{cell}} \alpha_{cell_i}(t), \quad (11)$$

with $\alpha_{cell_i}(t)$ the instantaneous cell duty cycle of the i^{th} cell.

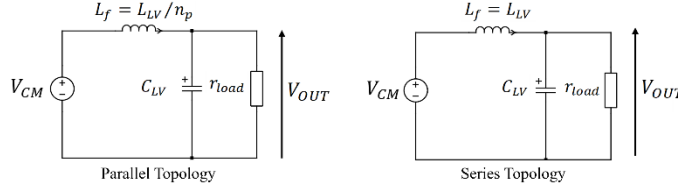


Fig. 6 Filter equivalent circuit for parallel and series topologies.

To be suitable for the control design, Eq. 11 must be transformed into its mean value formulation. The mean value V_{CM} of the converter voltage is written with Eq. 12 by introducing an equivalent mean common mode duty cycle α_{CM} .

$$V_{CM} = \frac{V_{HV}}{n_{cell}} \sum_i^{n_{cell}} \alpha_{cell_i}(t) = V_{HV} \cdot \alpha_{CM} \quad (12)$$

Using the previous formulation, a generalized state space system of the converter-filter can be established:

$$\begin{bmatrix} \dot{I}_L \\ \dot{V}_{OUT} \end{bmatrix} = \begin{bmatrix} -\frac{r_{Lf}}{L_f} & -\frac{1}{L_f} \\ \frac{1}{C_{LV}} & \frac{1}{r_{load}C_{LV}} \end{bmatrix} \begin{bmatrix} I_L \\ V_{OUT} \end{bmatrix} + \begin{bmatrix} \frac{V_{HV}}{L_f} \\ 0 \end{bmatrix} \alpha_{CM}. \quad (13)$$

B. Closed loop control of the output voltage

To be suitable for a closed loop control, the state space model in Eq. 13 must be discretized at the sampling time t_{sample} [40]. In a classical approach, the closed loop operation can be performed using discrete state space feedback with an integral action as in Fig. 7. A pole placement design allows calculating the feedback gains by choosing the desired closed loop performances required to generate the duty cycle α_{CMk} [41]

$$\alpha_{CMk} = -[K_L \ K_f] \begin{bmatrix} I_{Lk} \\ V_{OUTk} \end{bmatrix} - K_i \int (V_{refk} - V_{OUTk}), \quad (14)$$

where α_{CMk} is the mean duty cycle in the discretized k instant and K_L , K_f , K_i are the gains of the state space feedback control. The poles' frequencies are chosen according to the desired time of first peak during the system's step response. This time value is chosen as the minimum peak time in a 10% to 90% voltage step without duty cycle saturation. The peak time is selected using an iterative simulation which changes this set of gains to achieve the best time response with these restrictions. For the same control restrictions, improving the modulator yields better gains and better overall performance. Thus, Section V details the proposed multirate

modulator and Section VI shows its superior performance when compared to the classical ones.

V. MODULATION IN HIGH BANDWIDTH CONTROL OF MULTICELL CONVERTERS

A. Classical Modulator

The final objective of the control strategy is to generate the appropriated cell duty cycles $\alpha_{cell_i}(t)$ from α_{CM_k} . To generate these duty cycles, a PWM strategy is commonly implemented.

In the classical SS-PWM and AS-PWM, the discrete duty cycle α_{CM_k} is compared to n_{cell} triangular carrier signals with a phase shift of $2\pi/n_{cell}$ [42]. To get the mean value of the common current and to avoid overswitching, α_{CM_k} is updated on specific events related to the minimum or/and maximum values of the carrier signals. The duty cycle is then sampled with a period of $t_{sample} = t_{sw}/n_{cell}/s_{rate}$, with the sampling rate $s_{rate} = 1$ for symmetrical and $s_{rate} = 2$ for asymmetrical samplings. An example is shown on Fig. 8 for $n_{cell} = 3$ and an update related to the minimum value of each carrier (SS-PWM).

When a change occurs on the duty cycle command α_{CM_k} , each cell duty cycle α_{cell_i} is transformed through a sampling process with a cascaded delay, as depicted in Fig. 8. The real resulting duty cycle $\alpha_{CM_EQ_k}$ is then different from the required α_{CM_k} in the middle of the period, and the real mean output voltage V_{CM} is not rigorously equal to $V_{HV} \cdot \alpha_{CM}$. This implies that the state space model of Eq. 13 using α_{CM} is not strictly representative of the real behavior of the whole controlled system. The same observations can be done if the duty cycle α_{CM_k} is updated both on minimum and on maximum of the carrier signal (AS-PWM).

This sampling process strongly penalizes the control performances. Often omitted for slow bandwidth control by assuming that the duty cycle sampling process is perfect ($\alpha_{CM_EQ_k} = \alpha_{CM_k}$), it will be shown in the following that this behavior matters when high bandwidth control is requested.

B. Proposed Multirate Modulator

To reduce the influence of the sampling process on the output voltage control, a novel strategy is proposed to improve the generation of the cell duty cycles. The goal of such approach is to allow changes in all cell's duty cycles for each event on the carrier signals, not only for the event related to a specific cell. For this purpose, the mean voltage provided by the converter is studied over a subcycle period defined by t_{sample} .

Table III defines the notations used in this paper.

Depending on the number of cells and the sampling rate, a time window with duration t_{sample} starting from the sampling event is used to extract the shape of the carrier signals. As an example, Fig. 9(a) depicts the shape of the carrier signals in a subcycle for a three-cell converter in which the duty cycle update occurs only when the carrier passes through a minimum. At each instant t_k , regardless of which one is the active cell, the contribution of each cell to the global mean output voltage is defined for a three-cell converter as

$$V_{OUT}^{t_k} = (V_{cell_k}^{t_k} + V_{cell_{k-1}}^{t_k} + V_{cell_{k-2}}^{t_k})/3. \quad (15)$$

The comparison of the carrier signal with each duty cycle cell allows computing the mean voltage value of each of these cells over t_{sample} . Hence, from Fig. 9(b), the mean voltage of each cell during one sample period is not a linear function of the cell duty cycle as to a classical two-level converter.

This observation is a main point of the proposed approach. Usually neglected, this non-linearity constitutes a key point to improve the ability of the converter to provide a required voltage. With this, the objective is to find, at each t_k , the duty cycles $[\alpha_k^{t_k}, \alpha_{k-1}^{t_k}, \alpha_{k-2}^{t_k}]$ to apply during the next period t_{sample} to guarantee, if possible, the required output voltage $V_{OUT}^{t_k}$.

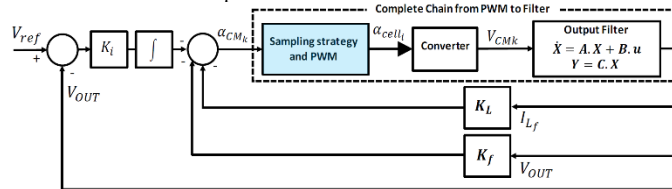


Fig. 7 State space feedback control.

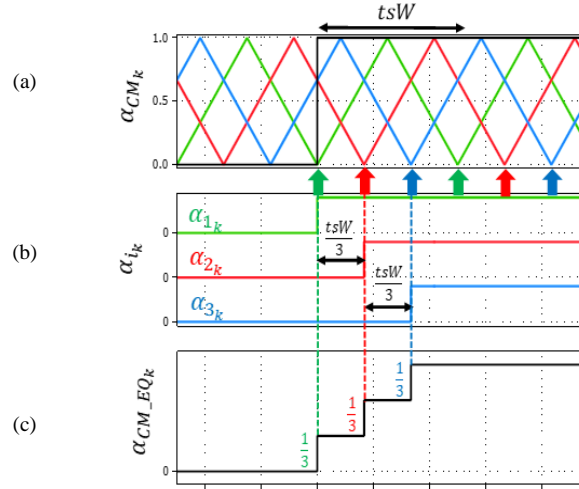


Fig. 8 Classical SS-PWM strategy for a three-cell converter: (a) shifted carriers signals and command, (b) cell duty cycle and (c) resultant duty cycle.

TABLE III
DEFINITION OF USED VARIABLES

$cell_k$: cell of which associated carrier signal equals 0 at t_k
$cell_{k-1}$: cell of which associated carrier signal was equal to 0 at t_{k-1}
$cell_{k-2}$: cell of which associated carrier signal was equal to 0 at t_{k-2}
$V_{cell_k}^{t_k}$: average normalized voltage on $[t_k, t_{k+1}]$ generated by $cell_k$
$V_{cell_{k-1}}^{t_k}$: average normalized voltage on $[t_k, t_{k+1}]$ generated by $cell_{k-1}$
$V_{cell_{k-2}}^{t_k}$: average normalized voltage on $[t_k, t_{k+1}]$ generated by $cell_{k-2}$
$\alpha_k^{t_k}$: signal sent to the non-inverting input of comparator k during $[t_k, t_{k+1}]$
$\alpha_{k-1}^{t_k}$: signal sent to the non-inverting input of comparator $k-1$ during $[t_k, t_{k+1}]$
$\alpha_{k-2}^{t_k}$: signal sent to the non-inverting input of comparator $k-2$ during $[t_k, t_{k+1}]$

While knowing that every cell can change its state twice (at any time, once for the positive carrier slope and once for the negative), the first task is to verify which cell has already switched during its own PWM cycle. With this, considering that the converter mean voltage output is given by Eq. 15, it is possible to calculate using Eq. 16 the required voltage (V_o) to be synthesized by the cells that are still able to switch. Since overswitching is not allowed, the state of the cells that already switched cannot be changed and their contributions ($V_k^{switched}$) to the desired converter output voltage $V_{OUT}^{t_k}$ is already defined.

$$V_{OUT}^{t_k} = \frac{1}{n_{cell}} \cdot \left(V_o + \sum V_k^{switched} \right) \quad (16)$$

Thus, an additional “watchdog” must be included to avoid the overswitching. For this purpose, it is defined new variables en_{k-1} and en_{k-2} respecting the rules presented in Table IV. With these rules, four different cases can be distinguished:

- 1) Case 0: if $[en_{k-1}, en_{k-2}] = [0,0]$, $cell_{k-1}$ and $cell_{k-2}$ already switched. Only $\alpha_k^{t_k}$ is free to be chosen as

$$\alpha_k^{t_k} = 2 \cdot V_{OUT}^{t_k} - \frac{2}{3} (V_{cell_{k-1}}^{t_k} + V_{cell_{k-2}}^{t_k}). \quad (17)$$

- 2) Case 1: if $[en_{k-1}, en_{k-2}] = [0,1]$, $cell_{k-1}$ already switched. $\alpha_k^{t_k}$ and $\alpha_{k-2}^{t_k}$ are free to be chosen as

$$\alpha_k^{t_k} = \alpha_{k-2}^{t_k} = V_{OUT}^{t_k} - \frac{1}{3} V_{cell_{k-1}}^{t_k}. \quad (18)$$

- 3) Case 2: if $[en_{k-1}, en_{k-2}] = [1,0]$, $cell_{k-2}$ already switched $\alpha_k^{t_k}$ and $\alpha_{k-1}^{t_k}$ are free to be chosen as

$$\alpha_k^{t_k} = \alpha_{k-1}^{t_k} = 2 \cdot V_{OUT}^{t_k} - \frac{2}{3} V_{cell_{k-2}}^{t_k}, \quad (19)$$

for $V_{cell_k}^{t_k} + V_{cell_{k-1}}^{t_k} < 1$, and

$$\alpha_k^{t_k} = \alpha_{k-1}^{t_k} = V_{OUT}^{t_k} - \frac{1}{3} V_{cell_{k-2}}^{t_k} + \frac{1}{3}, \quad (20)$$

for $V^{t_k}_{cell_k} + V^{t_k}_{cell_{k-1}} > 1$.

- 4) Case 3: if $[en_{k-1}, en_{k-2}] = [1, 1]$, α_k^{tk} , α_{k-1}^{tk} and α_{k-2}^{tk} are free to be chosen. An infinity of solutions is possible under respect of Eq. 16. It can be chosen for example as

$$\alpha_k^{tk} = \alpha_{k-1}^{tk} = \alpha_{k-2}^{tk} = V^{t_k}_{OUT}, \quad (21)$$

where $[\alpha_1^{tk}, \alpha_2^{tk}, \alpha_3^{tk}]$ can finally be defined by arranging the duty cycles $[\alpha_k^{tk}, \alpha_{k-1}^{tk}, \alpha_{k-2}^{tk}]$ by choosing the index k equal to the cell from which the carrier signal event comes from (1, 2 or 3).

This is summarized in

Table V, where “*pos*” corresponds to the cell number related to the considered carrier signal event.

For the sake of simplicity and easier understanding, the proposed approach is detailed for a three-cell parallel converter and symmetrical sampling. It must be underlined that one advantage of the proposed strategy is to be extendable to whatever the number of cells and the sampling rate by building a generic algorithm parametrized by n_{cell} and the sampling rate s_{rate} . Furthermore, since the output voltage expression is the same for parallel and series topologies, such proposed multirate strategy is suitable for any of these converter topologies. From a practical point of view, the proposed strategy is implemented in C-language to be suitable for real-time running.

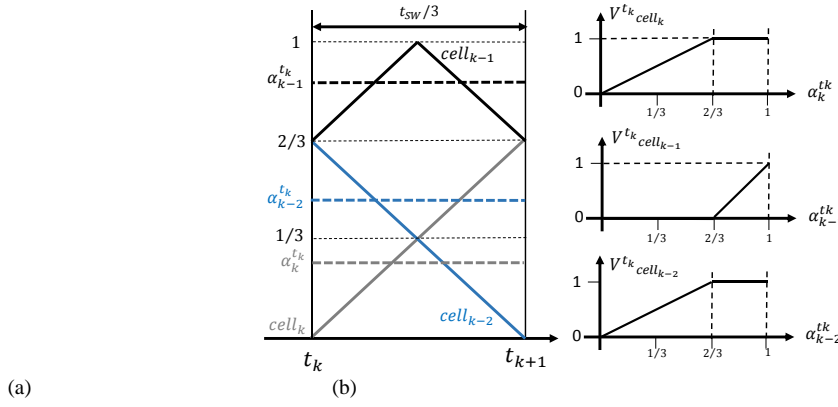


Fig. 9 Hypothetical three-cell converter: (a) PWM carriers during one subcycle sampling period and (b) possible voltage contributions of each cell.

TABLE IV
RULES FOR en_{k-1} AND en_{k-2} TO AVOID OVER-SWITCHING

en_{k-1}	If $\alpha_{k-1}^{t_{k-1}} < 2/3$, the cell $cell_{k-1}$ has already switched during the last increasing phase of the carrier signal: $en_{k-1} = 0$ (no change allowed on the duty cycle).
	If $\alpha_{k-1}^{t_{k-1}} > 2/3$, the cell $cell_{k-1}$ has not switched during the last increasing phase of the carrier signal: $en_{k-1} = 1$ (change allowed on the duty cycle).
en_{k-2}	If $\alpha_{k-2}^{t_{k-1}} < 2/3$, the cell $cell_{k-2}$ has not switched during the last decreasing phase of the carrier signal: $en_{k-2} = 1$ (change allowed on the duty cycle).
	If $\alpha_{k-2}^{t_{k-1}} > 2/3$, the cell $cell_{k-2}$ has already switched during the last decreasing phase of the carrier signal: $en_{k-2} = 0$ (no change allowed on the duty cycle).

TABLE V
MULTIRATE ALGORITHM RULES TO AVOID OVER-SWITCHING

Step 1 - Determination of $[\alpha_{k-1}^{t_{k-1}}, \alpha_{k-2}^{t_{k-1}}] = f(pos, \alpha_1^{t_{k-1}}, \alpha_2^{t_{k-1}})$
Step 2 - Determination of $[en_{k-1}, en_{k-2}] = f(pos, \alpha_{k-1}^{t_{k-1}}, \alpha_{k-2}^{t_{k-1}})$
Step 3 - Determination of $[V_{cell_{k-1}}^{t_{k-1}}, V_{cell_{k-2}}^{t_{k-1}}] = f(\alpha_{k-1}^{t_{k-1}}, \alpha_{k-2}^{t_{k-1}})$
Step 4 - Determination of $[\alpha_k^{t_k}, \alpha_{k-1}^{t_k}, \alpha_{k-2}^{t_k}] = f(V_{cell_{k-1}}^{t_{k-1}}, V_{OUT}^{t_k}, en_{k-1}, en_{k-2})$
Step 5 - Determination of $[\alpha_1^{t_k}, \alpha_2^{t_k}, \alpha_3^{t_k}] = f(\alpha_k^{t_k}, \alpha_{k-1}^{t_k}, \alpha_{k-2}^{t_k}, pos)$

VI. RESULTS

A. Considerations

The goal of this study is to determine the fastest response obtainable in closed loop operations using the classical SS-PWM and AS-PWM and comparing them with the proposed MSS-PWM and MAS-PWM. Only parallel converters will be assigned in the following. As already mentioned, the multirate modulator is directly transposable to series converters.

The definition of the “fastest response” implies taking into account the duty cycle saturation. In contrast to the classical small signal approach, the simulations are focused on a large-scale reference voltage step (from 10% to 90% of the DC bus voltage). In these conditions, the best reachable performance of a topology is defined as the fastest step response while respecting the duty cycles’ physical limits, i.e. $\alpha_{CM} \in [0,1]$.

The state space feedback gains are computed by choosing a specified time instant for the first peak value t_{peak} of the closed loop output voltage with a damping ratio $\xi = 0.7$ to ensure a corresponding voltage overshoot less than 5%. An iterative approach using numerical simulations is performed to find the fastest response according to the duty cycle limitations. Starting from a specified closed loop time response involving the duty cycle saturation (typically $t_{peak} < t_{optimal}$), t_{peak} is increased step by step until it is found the first step response for which the duty cycle α_{CM} is less than one, meaning that the control does not saturate. This response is then considered as the best for the situation under analysis and, thus, these control gains are used.

Moreover, the following premises will be assumed in the simulations and for the experimental results:

- 1) $V_{HV} = 100V$ and $f_{sw} = 20kHz$;
- 2) The filter is designed for each parallel converter, as the procedure described in Section II, i.e. the filter parameters of Table I are employed;
- 3) The controller gains are always calculated for each specific case in order to have the fastest possible response, changing with n_{cell} , the filter parameters, the load and also with the modulation strategy.

B. Simulation Results – Parallel Multicell Converters

To illustrate the use of the previous algorithm, closed loop simulations are performed using parallel converters, as depicted in Fig. 4, for $n_{cell} \in [1,7]$ with filter parameters of Table I and rated load resistance ($r_{Load} = 5\Omega$). This allows comparing the performances of the proposed multirate modulator with regard to the classical strategies of updating the cells duty cycles.

The step response performance changing the reference from 10% to 90% is evaluated using the first peak time t_{peak} expressed as a function of the switching period t_{sw} and the overshoot for the different number of cells and different sampling rate, as depicted in Fig. 10. In the same figure is also plotted the optimal time response of the output filter calculated as demonstrated in Section III and shown in Table II. This reference allows evaluating the distance between the control performances and the best obtainable physical responses.

The sampling process clearly reduces the bandwidth and the use of an asymmetrical sampling enhances the response for two and three cells. From Fig. 10, the time response with the proposed multirate modulation is improved in relation to the classical symmetrically and asymmetrically sampled ones no matter the number of cells, providing a closer-to-optimal response than the latter. As the classical approach does not account for the non-linearity of the system, the overshoot tends to be higher when compared to the proposed multirate.

Through Fig. 10, it is also observed that the fastest response can be achieved with a three-cell converter. This is a particular case for the chosen filter design that keeps the equivalent inductance (L_{LV}/n_p) constant independently of the number of cells (see Table I), while the capacitance drops with n_p^3 . The dynamics is more affected for smaller number of cells and tends to be constant increasing the number of cells. The s_{rate} also has higher influence on converters with a smaller number of cells.

As the three-cell parallel converter has the fastest response in this case, it is the one chosen for study in the following sections.

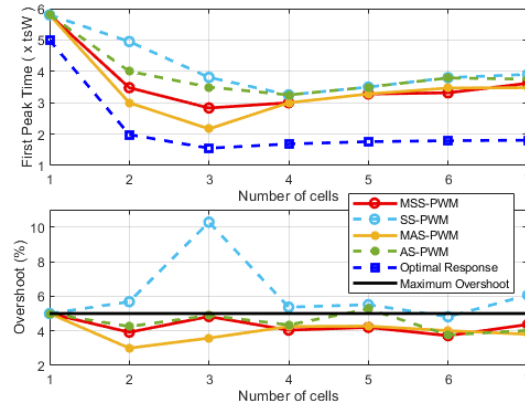


Fig. 10 Closed loop system response of n_{cell} parallel converters using the SS-PWM, AS-PWM, MSS-PWM and MAS-PWM for rated resistance.

C. Simulation Results – Three-Cell Parallel Converter

First, the effect of the variation of filter parameters on the three-cell parallel converter is investigated. The inductance and capacitance values presented in Table I are considered as a base and they are varied from -20% to $+20\%$. Fig. 11(a) and (b) show the time of the first voltage peak as a function of t_{sw} for both classical SS-PWM and proposed MS-PWM, respectively.

It can be seen that, when the classical modulator is employed, the system is more prone to variations in the time response. In this case, the higher the inductance, the slower is the response. However, the most important factor is the capacitance: the higher it is the faster is the response.

When the multirate modulator is employed, the capacitance has almost no effect on the time response when evaluated individually, whereas the inductance has a small influence. One can notice that the multirate modulator reduces the effect of the parameters variation and always leads to a better response compared to the classical one.

Since the results from Fig. 11 consider a fixed load (rated current), Table VI shows the comparison of the time to reach the first voltage peak between both modulators for different load resistances. Furthermore, the optimal time is presented for sake of comparison. The system response is more affected when the classical modulator is employed and the proposed method has superior performance regardless of the load resistance.

D. Experimental Setup – Three-Cell Parallel Converter

The experimental setup is constituted of a three-cell parallel converter. Its structure is the same as the one presented in Fig. 4 with $n_{cell} = 3$.

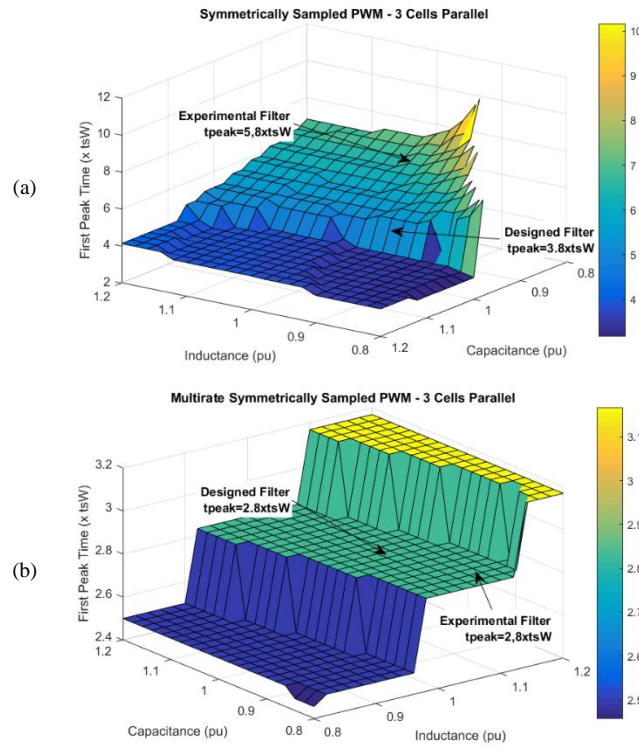


Fig. 11 Time response of three-cell parallel converter with closed loop control for $r_{load} = 5 \Omega$: (a) SS-PWM and (b) proposed MSS-PWM.

Fuji Electric 2MBI300VB060 IGBT are used and the system is controlled by a PLECS RTBox with a deadtime of $1\mu s$. Each individual carrier has a frequency of $f_{sw} = 20\text{kHz}$, thus the sampling period is $t'_{sample} = 16.6\mu s$ for the symmetrically sampled cases and $t''_{sample} = 8.3\mu s$ for the asymmetrically sampled ones. The employed filter has similar parameters to the previous design. In fact, there is a small difference in the prototype values ($L_{LV} = 650\mu H$, $C_{LV} = 2.5\mu F$), that influences the system response mainly in the SS-PWM, as demonstrated in the points signaled in Fig. 11. The workbench used on all tests is depicted in Fig. 12.

E. Experimental Results – Open Loop

First, an open loop study is made. For this, it is important to check the mean value of all individual α_{cell_i} , which is the mean equivalent duty cycle (α_{eq}) perceived by the converter. Fig. 13 shows α_{eq} for the classical SS-PWM, the proposed MSS-PWM and also for the NS-PWM.

TABLE VI

TIME TO FIRST PEAK FOR A THREE-CELL PARALLEL CONVERTER (MULTIPLE OF t_{sw}): $V_{HV} = 100V$, $I_{LV} = 20A$, $f_{sw} = 20\text{kHz}$, $s_{rate} = 1$

$r_{load} (\Omega)$	3.5	5	6.5	8	9.5	11	20
SS-PWM	7.83	3.81	3.80	3.83	3.83	3.83	5.81
MSS-PWM	4.17	2.83	2.50	2.17	1.83	1.83	1.83
Optimal	2.37	1.55	1.25	1.13	1.07	1.03	0.97

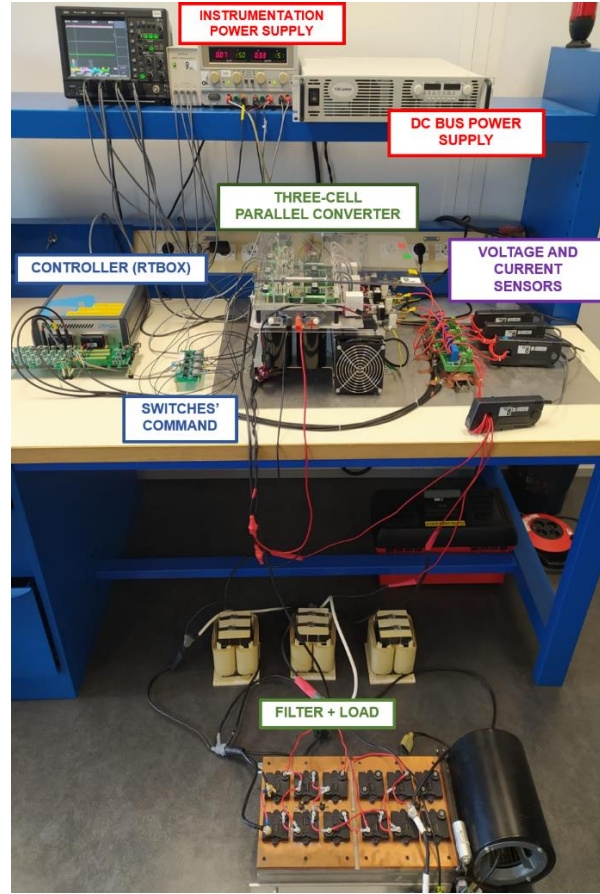


Fig. 12 Experimental setup: DC/DC three-cell parallel converter.

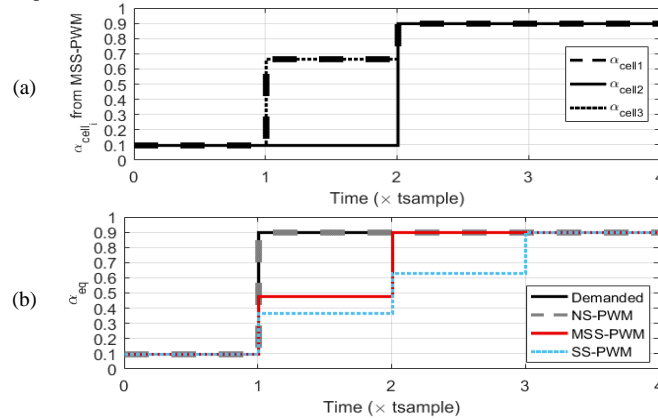


Fig. 13 Experimental results in open loop and symmetrical sampling: (a) α_{cell_i} with the MSS-PWM algorithm and (b) comparison between α_{eq} determined via the NS-PWM, SS-PWM and MSS-PWM during a step in reference.

When updating duty cycles in multicell converters without overswitching, there is a time delay between calculated and synthesized equivalent duty cycles. This is due to the restriction that each cell can switch only in a certain proper time. As shown in Fig. 13, during the given step change, the multirate algorithm reaches the final desired reference level a whole sampling time earlier (twice as fast) than the classical SS-PWM approach, which reduces the aforementioned modulator delay.

Fig. 14 shows the load voltage comparison of the NS-PWM, SS-PWM, AS-PWM, MSS-PWM and MAS-PWM for the rated load resistance ($r_{Load} = 5 \Omega$) in open loop operation. The inherent time delays (t_{delay}) between computing the duty cycle and outputting

the commands are highlighted in the graph for each sampling strategy.

When the system is submitted to a change in the reference output voltage, the NS-PWM allows for a fast response by immediately updating the duty cycle of every single cell in the converter regardless of the occurrence of overswitching. Given that overswitching is a problem because it increases losses and causes EMI problems, it is desired that this behavior is avoided.

The classical SS-PWM and AS-PWM prevent the occurrence of overswitching by allowing the update of each cell duty cycle only once per carrier period. The proposed multirate PWM is a middle ground between the natural and classical PWMs: by determining which cell has already switched during its own PWM cycle and preventing their duty cycle from changing at a software (code) level, it allows the immediate update of all of the other cells' duty cycles while avoiding overswitching. Thus, the proposed multirate is able to present faster responses than the classical SS-PWM and AS-PWM as observed from the curves presented in Fig. 14.

F. Experimental Results – Closed Loop

The load voltages from Fig. 14 present steady state error for all of the tested PWM methods. Therefore, even though the advantages of the proposed modulator can be seen in open loop, an enhancement of the response can be better in closed loop. Table VII shows the closed loop gains calculated for rated load resistance load for the tested modulation methods. Only the strategies without overswitching will be compared.

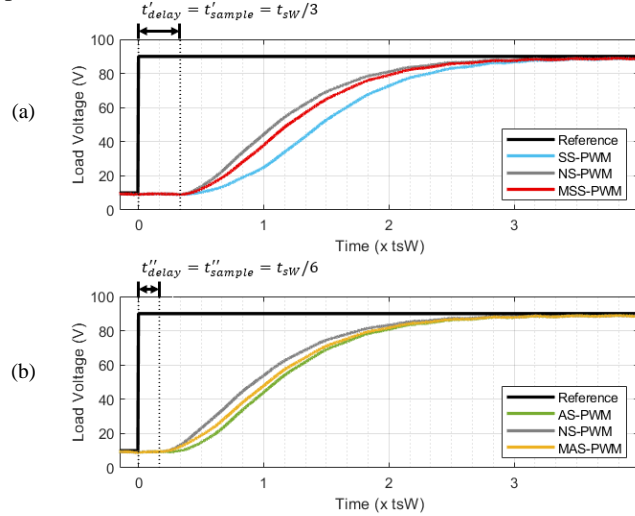


Fig. 14 Experimental results (time response) of the three-cell parallel converter in open loop with rated load: measured load voltages with (a) the SS-PWM, NS-PWM and MSS-PWM and (b) the AS-PWM, NS-PWM and MAS-PWM.

TABLE VII
DESIGNED CLOSED LOOP GAINS FOR EACH TESTED MODULATOR

Modulator	K_L	K_f	K_i
SS-PWM	0.0527	-0.0080	-123.4379
AS-PWM	0.1778	-0.0114	-619.7231
MSS-PWM	0.1049	-0.0039	-469.0183
MAS-PWM	0.2033	-0.0074	-924.3017

Trying to make the control extremely fast is a challenge in the prototype due to the inherent time delays between duty cycle computations and analog to digital conversions (ADC) of measurement samples. Using the measured quantities in the control leads to an unstable behavior since it has not been designed to compensate these delays. This particular point is out of the present paper scope.

To overcome this problem and validate the proposed method, a state space estimator [41] based on Eq. 13 is implemented to estimate the voltage and current used in the control instead of the measurements. In this configuration, it is possible to highlight the performances of the modulator regardless of the constraints related to the measurement delays. Nevertheless, it is important to highlight that the experimental results presented are from direct measurements of the output voltage.

The converter duty cycles are computed by the control, using the estimator and the modulator. The RT Box's processor does this within the available calculation period of $16.6\mu s$ for symmetrical sampling and $8.3\mu s$ for asymmetrical sampling. To complete a computation cycle, it takes a total time of $1.1\mu s$ for the multirate strategy (MSS-PWM and MAS-PWM) and $0.62\mu s$ for the classical one (SS-PWM and AS-PWM). For the worst scenario of asymmetrical sampling, this means 13.3% and 7.5% of processor usage, respectively.

Fig. 15(a) shows the comparison of the SS-PWM, AS-PWM, MSS-PWM and MAS-PWM for rated load resistance ($r_{Load} = 5 \Omega$) in closed loop operation. For the sake of validation, the simulation results are also plotted using the filter parameters of the experimental setup. In fact, the measurements have a delay of one sampling time in comparison with the simulation, because the digital control platform has an inherent calculation time and the command signal is only made available in its output in the next sampling period. For a more direct comparison, the simulation data is delayed by its modulator respective t_{delay} in the presented graph.

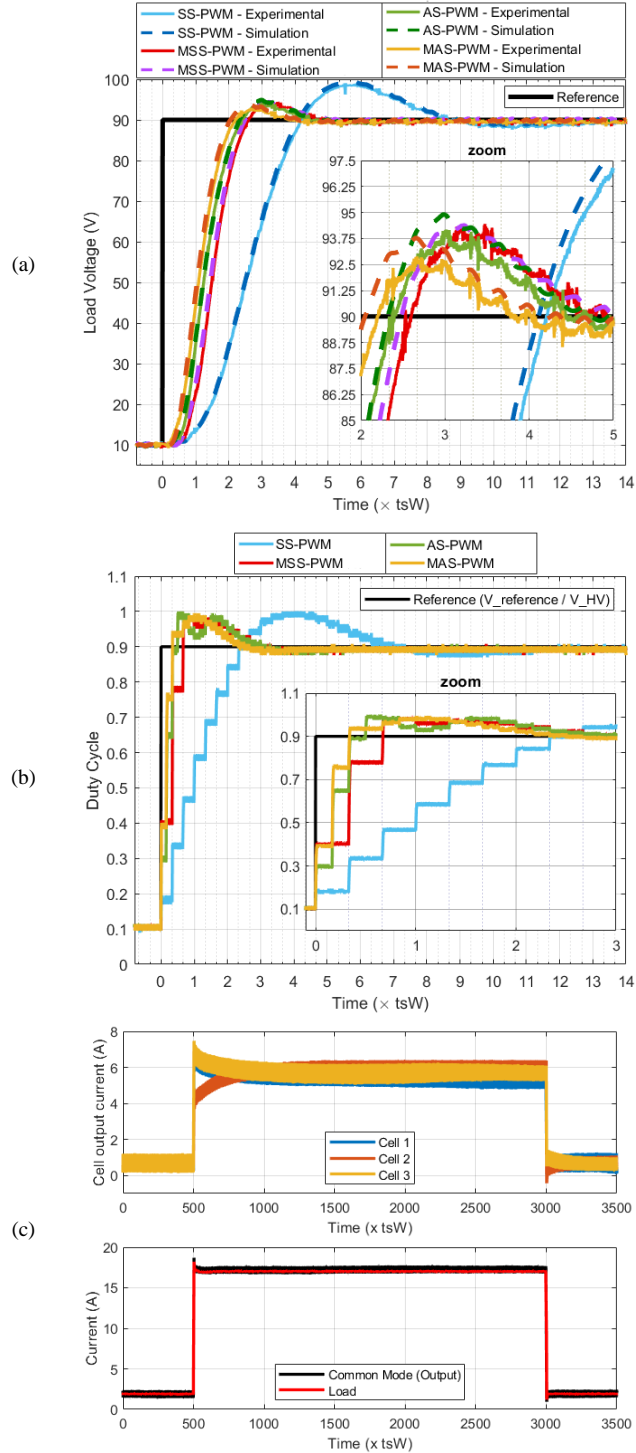


Fig. 15 Experimental results (time response) of the three-cell parallel converter with closed loop control using the classical SS-PWM and AS-PWM and the proposed MSS-PWM and MAS-PWM: (a) load voltage, (b) duty cycle (control command) and (c) cells, common mode and load currents with MSS-PWM.

From Fig. 15, for the symmetrical sampling cases, the proposed method makes the response much faster and it also reduces the

overshoot. This happens because the multirate modulator can effectively control the average value of the chopped voltage over each $t_{sw}/3$ interval (instead of t_{sw} for the standard modulator). For the asymmetrical sampling cases, the response is faster with the multirate modulator, but the improvement is marginal for this specific test. As already mentioned while discussing the simulation results and it will be reinforced by the experimental results, such improvement depends on the load and the filter.

It is also important to highlight that, in both cases, the control output (duty cycle) peaks at (but does not exceed) 100%, as in Fig. 15(b). This proves that both controllers were efficiently designed to maximize speed without distortion in this 10% to 90% voltage reference ($V_{reference}$) step. Thus, the enhancement in the system performance is due to the proposed method, not because of the different control tuning for each load.

As shown in Fig. 15(c), the average current values of each cell converge to values that are very close to each other, with the differences between them being due to deviations inherent to the manufacturing process of the used inductors. This small unbalance in steady state exists for all the modulation strategies and it can be eliminated by using differential control techniques as the one presented in [43]. To disturb the common mode current as little as possible and have a fast response, the single constraint is to design the differential control with a low bandwidth with regard to the common mode dynamic.

Furthermore, it can be seen from Fig. 15(a) that the measured load voltage overshoot and first peak time for all tested modulators (specially for the multirate ones due to their resilience to parametric deviation) is in agreement with the information disclosed in Fig. 10 and Fig. 11 for $n_{cell} = 3$ and the previously discussed filter analysis is validated.

Fig. 16 shows results for the symmetrical and asymmetrical sampling strategies with different r_{Load} . From it, the higher the resistance (smaller current), the faster the response in all cases. The multirate modulator has faster responses than the classical strategy while keeping the overshoot within design constraints.

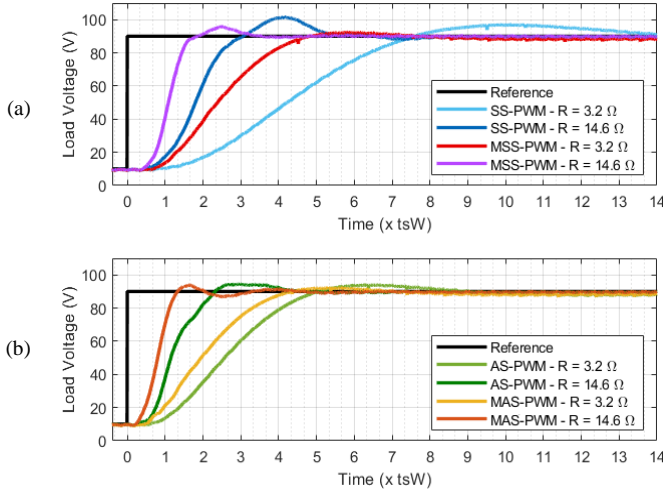


Fig. 16 Experimental results obtained by changing the load resistance (rated values): a) SS-PWM and MSS-PWM and b) AS-PWM and MAS-PWM.

G. Experimental Results – Steady State Analysis

To deepen the study of the proposed multirate modulator, it is fitting to carry out an analysis of its performance in steady state through zoom-ins on Fig. 14 and Fig. 15. Thus, Fig. 17 allow the comparison between the steady state load voltages' waveforms with rated load for both the classical and multirate modulators. From all the curves shown in these figures, it is noted that the multirate modulator not only allows for faster responses with smaller overshoot, but it also does not provoke any degradation of the system's performance in steady state.

VII. CONCLUSIONS

In this paper, a novel multirate modulator is proposed to improve the closed loop performances of the output voltage control of parallel and series converters. This modulator takes into account the non-linearity between the subcycle duty cycle and the subcycle average output voltage of multicell converters. A generic multirate modulator has been developed to be adaptable for any cell number and for the two different sampling strategies (symmetrical and asymmetrical). One of its advantages is that both the MSS-PWM and MAS-PWM are fully software implemented and overswitching is avoided.

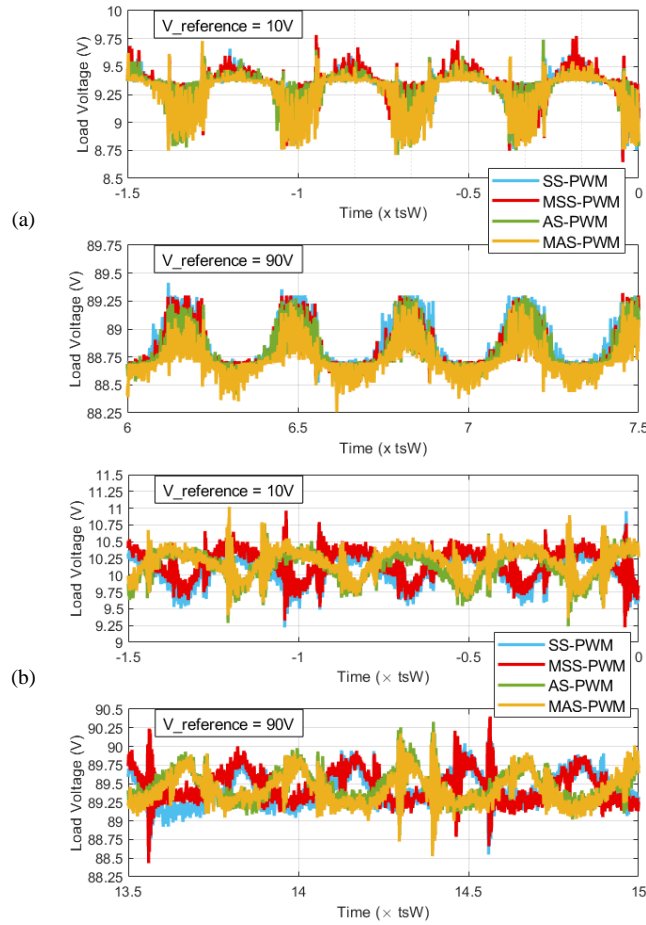


Fig. 17 Experimental results of the three-cell parallel converter with rated load for both a 10V and a 90V voltage reference: steady state load voltages with the classical and multirate modulators in (a) open loop and (b) closed loop.

The reduction of the modulator delay will affect the overall control performance and it is one way to achieve a better global response. The open loop step responses demonstrate that the multirate modulator allow the converter's mean equivalent duty cycle to reach steady state faster than the classical SS-PWM and AS-PWM. This improved performance also lead to better results for the closed loop tests. Thus, by using the multirate modulator, it is possible to obtain faster responses (without degrading the system's steady state performance) and this can be a significant improvement when high bandwidth is required.

It was shown through simulations and experimental results that this proposed multirate strategy (the MSS-PWM and MAS-PWM) always surpasses the classical SS-PWM and AS-PWM regarding the reachable time response no matter the load and even considering a variation in the filter parameters. This concept is also immediately applicable to series converters since there is a duality between them.

Lastly, the effects of decreasing the modulator's time might not be noticeable if the filter design is not proper. If this happens, the effects of the modulator's delay reduction may be overshadowed by the slower dynamics imposed by the filter itself. In light of this, a study of the influence of the number and configuration of cells in the filter design and control dynamic behavior was presented. By optimizing the filter and having a quick multirate modulator, it is possible to design even faster controllers to have fast global responses.

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