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D. Bosch, F. Andrieu, X. Garros, L. Ciampolini, A. Makosiej, et al.. Back-bias impact on variability and BTI for 3D-monolithic 14nm FDSOI SRAMs applications. 2019 Joint International EUROSIOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSIOI-ULIS), Apr 2019, Grenoble, France. pp.1-4, <10.1109/EUROSIOI-ULIS45800.2019.9041890>. <hal-02998370>

HAL Id: hal-02998370

<https://hal.science/hal-02998370v1>

Submitted on 19 Nov 2020

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Back-bias impact on variability and BTI for 3D-monolithic 14nm FDSOI SRAMs applications

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Abstract— We fabricated and characterized 14nm planar Fully-Depleted-Silicon-On-Insulator (FDSOI) 0.078 μm^2 SRAM cells. Temporal and spatial variability as well as sensibility to temperature, supply voltage (V_{DD}) and back bias (V_{well}) are extracted. These data evidence that the 14nm SRAM is read-limited, which could be improved by a smart back-bias management [1]. In this work we demonstrate a 50mV Static Noise Margin (SNM) variability improvement (at $V_{DD}=0.8\text{V}$) by back-bias, without additional BTI stress. Such an assist technique can be eventually leveraged at fine-grain by 3D monolithic integration, owing to local back-planes.

Keywords- 3D-monolithic; FDSOI; BTI stress; Supply Read Retention Voltage; SRAM margins; variability

I. INTRODUCTION

3D-monolithic integration, also named 3D sequential, consists in stacking active device layers on top of each other in a sequential manner on a given wafer substrate. This technology improves digital performance by reducing the wire length [2]. Moreover, it enables the integration of local back-planes (Figs 1-2), which can be dynamically biased in order to improve the performance of standard cells [3] and SRAMs [1] without area overhead. In order to verify if this fine-grain assist can be also used to compensate spatial variability with high reliability, we measure in this work, the impact of back-bias on 14nm planar FDSOI SRAM variability and BTI.

II. CHARACTERIZATION OF 14 FDSOI SRAMs

High-density (HD, 0.078 μm^2) and High-current (HC, 0.098 μm^2) 14nm planar FDSOI SRAMs have been fabricated on silicon channel with a single p-type metal gate and single p-doped well (SPWELL) [4]. SRAM typical figures of merits, SNM and Write Noise Margin (WNM), have been electrically characterized. Considering worst-case measurements at low V_{DD} and 125°C and including global variability considerations, one finds that 14nm FDSOI SRAM stability is read-limited (Fig.3). In fact, to enhance SNM, standard assist technique can be used [5]. More specifically, Fig.4 shows that a Word-line (WL) underdrive by 20% improves the SNM by 37% at $V_{DD}=0.8\text{V}$.

A. SNM spatial compensation with back bias

A 63-50 mV/V threshold voltage sensibility on well bias (V_{well}) was extracted for the HC-HD Pass-Gate (PG),

respectively (Fig.5). This enables either the PG drive current to be boosted by 44% for $V_{well}=2\text{V}$ or its leakage to be reduced below 0.1pA for $V_{well}=-2\text{V}$ on demand (Fig.6). Since the well is shared between all devices in planar FDSOI, $V_{well}<0$ strengthens PMOS Pull-Up (PU) with respect to NMOS (PG, Pull-Down PD), helping the PU to maintain BLTI=1 and BLFI=0 during the read operation. On the contrary, using $V_{well}>0$ improves the PG/PU strength ratio (and so the WNM). Thus, the sensibility of SRAM to the back bias can be used to assist the read ($V_{well}<0$) and write ($V_{well}>0$) operation. This feature can be used as a process compensation technique, to narrow die-to-die variations, as illustrated by the 50mV SNM variability improvement in HD bitcells across wafer (Fig.7).

B. BTI-induced dynamic variability at the bitcell level

In order to check if this bias-bias assist influences the ageing, we measured the so-called Supply Read Retention Voltage SRRV at 125°C and $V_{DD\text{stress}}=2\text{V}$, which is representative of the SNM (Fig.8 and [6]). Our Bit-Line (BL) current fast measurement method is effective to extract the reduction of the read margin induced by stress (Fig. 9 and [6]). ΔSRRV distributions at different stress times for $V_{well} = 0$ and -0.8V are reported in Fig. 10. Same ageing is observed for both positive and negative V_{well} , proving that back biasing does not degrade the BTI reliability. Finally, $V_{well}=-0.8\text{V}$ boosts SRRV by 65.5mV-38.1mV on fresh bitcells and after stress, respectively (Figs 11-12).

III. PERSPECTIVES

We provide guidelines to improve SNM variability in 14nm SRAM cells without ageing drawback. This opens the path towards a fine-grain back-bias assist technique using the unique features of 3D monolithic CoolCubeTM integration.

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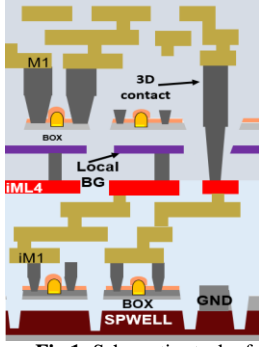


Fig.1: Schematic stack of CoolCube™ 14nm Design Kit with a via between the back gate and the upper intermediate metal line.

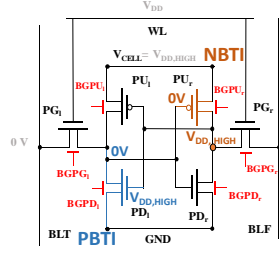


Fig.2: SRAM schematics. The additional terminals provided by CoolCube™ technology are highlighted in red. BTI setup is indicated in gray.

FOM (mV)	High-Density (HD)	High-Current (HC)
SNM (T=25°C, V _{DD} =0.8V)	139	148
WNM (T=25°C, V _{DD} =0.8V)	320	351
SNM (T=125°C, V _{DD} =0.55V)	68	88.5

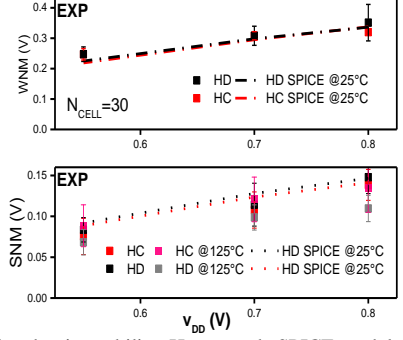


Fig.3: Right: Read and write stability, Home made SPICE model vs. Experimental for different V_{DD} and temperature. Left: SNM-WNM extracted values from graph.

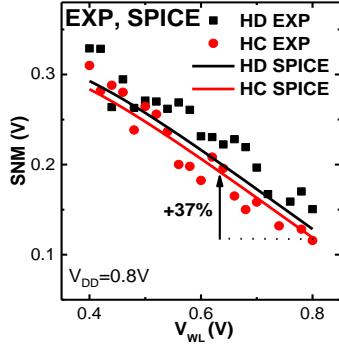


Fig.4: Exp vs. SPICE SNM in function of WL voltage (worldline underdrive read assist).

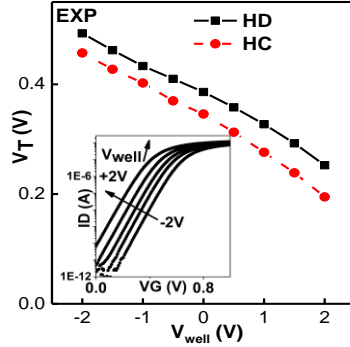


Fig.5: Exp. pass Gate threshold voltage modulation with back biasing. $I_D(V_G)$ (insert).

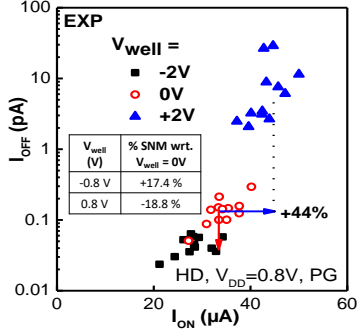


Fig.6: Exp. High density Pass Gate $I_{OFF}(I_{ON})$ for different V_{well} . SNM vs. V_{well} (insert)

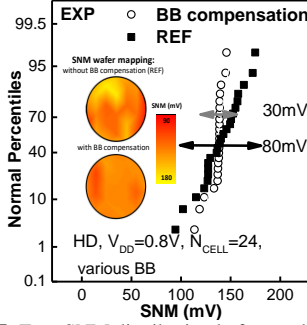


Fig.7: Exp. SNM distribution before and after back bias compensation.

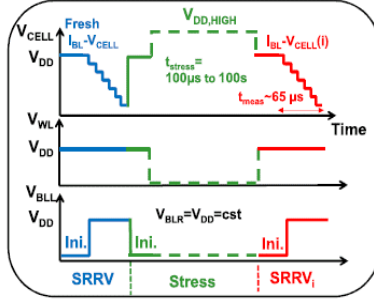


Fig.8: Fast procedure waveform used for SRAM cell reliability characterisation [6].

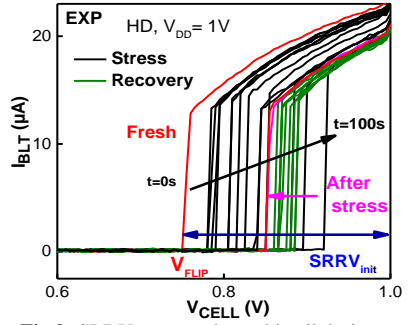


Fig.9: SRRV measured on a bitcell during stress & recovery.

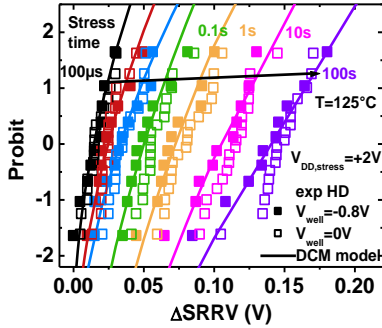


Fig.10: Experimental $\Delta SRRV$ distribution on ~20 bitcells for two V_{well} polarizations and fitted using the model [6].

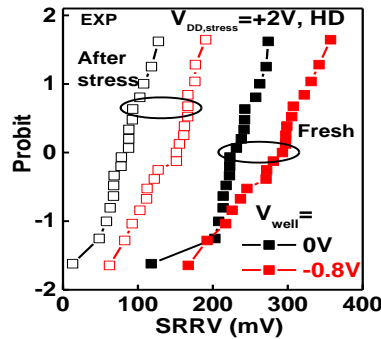


Fig.11: Fresh and after stress SRRV distribution for different p-well biasing.

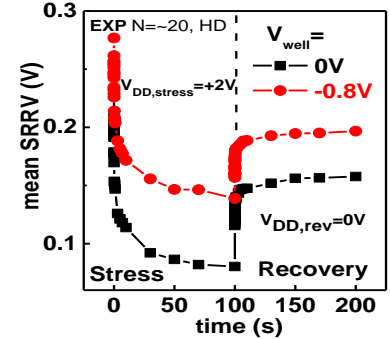


Fig.12: $\mu SRRV$ during stress and recovery. A -0.8 V V_{well} biasing achieves better stability.

ACKNOWLEDGMENTS: This work was supported by French Public Authorities through LabEx Minos ANR-10-LABX-55-01.