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PROJECT AMELIZ: PATTERNING TECHNIQUES FOR COPPER ELECTROPLATED METALLIZATION ON HETEROJUNCTION CELLS

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ABSTRACT: For the current PV production about 2000 tons of silver are consumed per year. This is already 10% of the entire world annual silver supply. The PV production is expected to grow significantly in the next decades in order to enable the energy transition to 100% renewables. Annual production volumes in the terawatt range are predicted already for 2030 and this may lead to higher silver price and put more pressure on the industry to replace silver by copper.

With the currently available processes the cost advantage of copper plating over screen printing is relatively small and the implementation of plating in production is slowed down by the high up-front investment for equipment. The highest cost share of the process sequence has the patterning and research activities focus on new, i.e. more cost competitive patterning techniques.

Within the Ameliz project several approaches are investigated: firstly, patterning by printing a metal seed grid with a dielectric layer as plating mask and secondly masking by a monolayer of self-assembling molecules. These molecules consist of a phosphonic acid group and a hydrocarbon chain. They are bonded to the ITO surface and form a monolayer of well-ordered, densely packed hydrophobic chains, which protects the ITO surface against plating solutions. Furthermore, methods for selective formation of a copper seed layer by electrografting and for improved adhesion by ITO reduction are being investigated.

1 INTRODUCTION

“2019 was one of the best years ever for solar in the European Union. The region installed 16.7 GW – a 104% increase over the 8.2 GW added the year before.” [1] The global PV installations have reached 0.5 TW by the end of 2018 and the Compound Annual Growth Rate of PV installations was 36.8% in the last years. [2] [3]

The predictions for annual PV production in 2030 differ from 300 GW (IEA), through 700 GW (Breyer “Electricity”) to 1400 GW (“Broad electrification”) [3] [4] A panel of renowned experts from research and industry envisages total global PV installations at 10 TW by 2030 [5].

Currently 2000 tons of silver are consumed for solar cell production, assuming 100 mg paste laydown, 5 Wp per cell and 100 GW annual production. In 2019 already 10% of the entire world silver supply were consumed for the PV sector for production slightly above 100 GW [6]

Because of the increasing demand for PV the silver price may rise in the coming years and the replacement of silver as well as of other rare elements becomes necessary for the industry. [7]

With our baseline copper plating sequence high efficiency has been demonstrated on industrial heterojunction cell precursors and excellent module stability has been confirmed in extended aging tests.

The process offers a small cost advantage compared to screen printing, the cost difference being highly dependent on the silver price. The patterning has the highest cost share of the entire process sequence and several alternative patterning approaches are being developed within the Ameliz project.

2 BASELINE PROCESS

Our baseline process comprises a sputtered metal seed layer and patterning by hotmelt inkjet printing. After copper plating the hotmelt mask is removed and the seed layer etched back in between the fingers.

Line dimensions of 25 μm width and 25 μm height are reliably feasible with hotmelt inkjet patterning. The specific resistivity of lines deposited from our electrolytes is slightly higher than the resistivity of bulk copper (1.7 $\mu\Omega\cdot\text{cm}$) and the measured values vary between 1.8 and 2.6 $\mu\Omega\cdot\text{cm}$. The used seed layer stack, consisting of a thin adhesion layer and a copper layer for sufficient lateral conductivity, allows for low contact resistivity in the range 0.05 to 0.5 $\text{m}\Omega\cdot\text{cm}^2$ on different TCOs, and for good adhesion. In a 180° peel test performed on cells with soldered ribbons force values above 4 N/mm have been measured. Good efficiency above 24.7% and 83.3% fill factor have been achieved on an industrial precursor for a monofacial cell with four busbar layout.

Table 1: Cell efficiency certified by ISFH CaTec

HJT cell	Area [cm ²]	Jsc [mA/cm ²]	Voc [mV]	FF [%]	Eff. [%]
4BB, monof.	222.8	40.3	736.1	83.3	24.73

Excellent stability of modules made of heterojunction cells featuring copper plated metallization has been confirmed for interconnection with wires (Smart Wire Connection Technology) as well as for interconnection with soldered ribbons, exceeding in both cases three times the IEC 61215 norm.

Further details of the process are described in [8].

3 PRINTED SEED GRID AND DIELECTRIC LAYER

Another approach is to use a thin layer of dielectric as plating mask instead of an organic resist [9]. The dielectric layer such as silicon nitride, silicon oxide or aluminum oxide is less than 100 nm thick. The process sequence is visualized in **Figure 1**. At first a grid of lines and current collecting busbars is printed on both sides of the cell. Either screen printing or inkjet printing of a metal particle paste are applicable. Contrary to standard screen printing for heterojunction cells with busbar-layout the lines are very fine as the required conductivity will be provided by the subsequently electrodeposited copper. In the next step a dielectric layer is deposited over the entire surface. Since the surface of a printed seed line is rough and the dielectric layer not perfectly tight on top of the lines, electrons can pass through and copper can be deposited on top of the printed seed grid. The dielectric layer remains on the cell and in the module and serves as double antireflective coating. The thickness of the underlying thin conductive oxide can thus be reduced (lower cost) while preserving good optical properties of the whole stack.

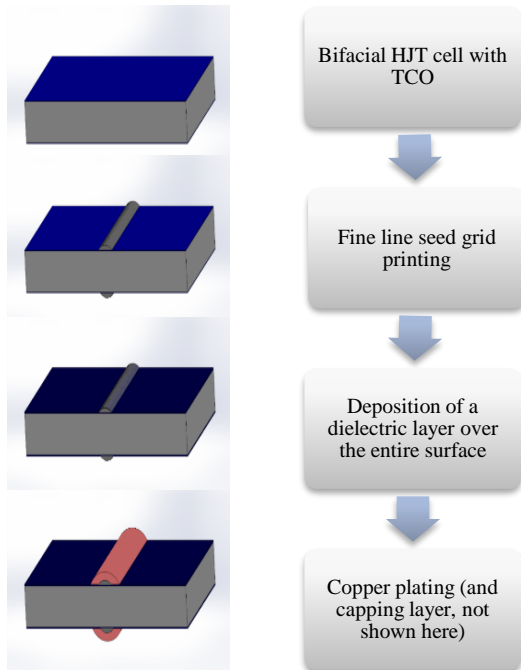


Figure 1: Process sequence with printed seed grid and a dielectric layer as plating mask.

For the first cell tests standard M2 cell precursors with ITO and screen-printed seed-grid with 4-busbar-layout have been used, with standard printing parameters, optimized for cells with busbars and with accordingly high silver paste laydown above 300 mg (bifacial cells). A thin aluminum oxide layer (8 nm) has been deposited by ALD as plating mask and good plating selectivity as well as continuous copper deposition on the printed grid have been obtained from an acidic copper electrolyte at moderate current density of 8 A/dm². (**Figure 2** and **Figure 3**). Because of the wider fingers the J_{sc} and the cell efficiency were slightly lower after plating.

In the next experiment a grid with very fine lines will be used and only the electrodeposited copper will provide the required line conductivity.

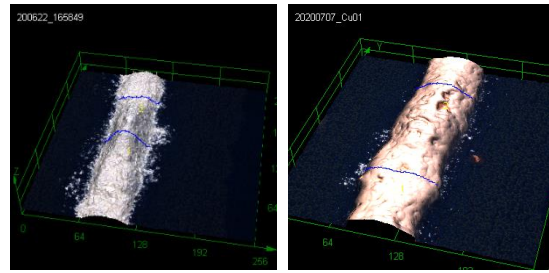


Figure 2: Screen-printed seed-grid (on the left), and printed finger covered with electrodeposited copper.

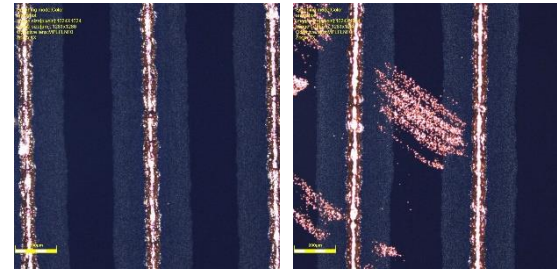


Figure 3: Cell area with selective copper deposition on the seed-grid and heavy ghost plating on scratched area.

To enable further cost reduction a commercially available copper paste has been tested as seed-grid for plating. The resistivity of the paste is significantly higher than of the silver paste (**Table 2**), but by far sufficient to conduct the small current needed for electrodeposition of copper. Paste optimization will be necessary for printing of very fine lines on textured wafers as well as for contact formation on thin conductive oxides. Contact resistivity of 3.0 and 3.4 m Ω ·cm² has been measured on IWO and ITO, respectively.

Table 2: Specific contact resistivity of low temperature silver paste, copper paste and electrodeposited copper

Paste / galvanic Cu	CS-area [μm^2]	Resistance [Ω]	Spec. resistivity [$\mu\Omega \cdot \text{cm}$]
Ag paste (200°C)	2925	0.12	4.0
Cu paste (200°C)	1880	1.24	27.4
Cu plated on paste	5480*	0.04	2.8
Only plated Cu	3600**	0.04	1.8

* Entire cross section of the line with Cu plated over Cu paste

** Cross section of the copper paste underneath subtracted

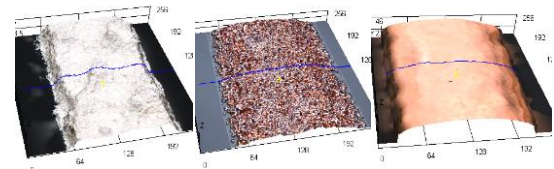


Figure 4: Lines with screen printed silver paste, screen printed copper paste and copper electrodeposited over copper paste; printed on glass.

Thin conductive oxides like IWO and ITO are excellent barriers against copper diffusion [10] [11]. Photoluminescence measurements on heterojunction cell precursors with IWO or ITO with screen-printed copper paste show no impact on cell passivation after annealing at 200°C for 60 minutes. To confirm in extended annealing tests

4 SELF ASSEMBLED MONOLAYER (SAM)

Since SAMs utilize an extremely small amount of material, the monolayer being only ~2nm thick, this approach could achieve plating selectivity with ultra-low costs. Commercially available perfluorinated phosphonic acid as shown in **Figure 5** as well as octadecyl phosphonic acid (C18-PA) were applied at first on polished silicon wafers with low roughness ITO. [12]

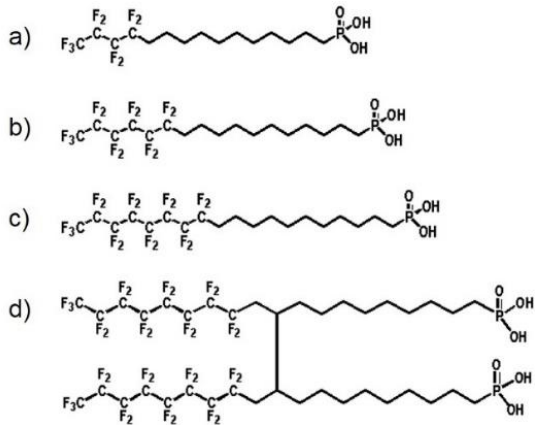


Figure 5: Chemical formulas of used perfluorinated phosphonic acids, a) Nonafluoropentadecylphosphonic acid (fC15-PA), b) Tridecafluoroseptadecylphosphonic acid (fC17-PA), c) Heptadecafluorononadecylphosphonic acid (fC19-PA), and d) Heptadecafluoronylicosanediyldiphosphonic acid (bis-fC19-bisPA).

Dynamic contact angles were measured before and after 10 minutes immersion in a highly acidic copper electrolyte. The results are shown in **Figure 6**. The measurements before and after immersion in the copper electrolyte confirm a lesser attack of the ITO surface when covered by bis-f19-bis-PA and C18-PA molecules. We interpret this as a result of a better packing of the hydrophobic chains in the self-assembled monolayers. While hydrocarbon chains present a linear structure, perfluorinated chains form a helical structure and therefore self-assemble in less compact and more disordered layers. [13]

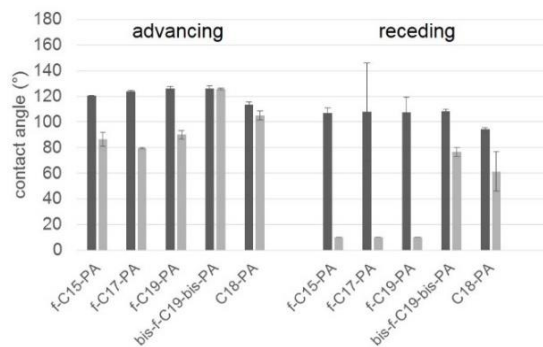


Figure 6: Dynamic water contact angles of various SAMs on low roughness ITO surface. The contact angles were taken before (dark grey) and after immersion (light grey bars) for 10 min in a highly acidic copper electrolyte.

Octadecyl phosphonic acid (C18-PA) was then applied on textured surface, on a standard M2 HJT cell precursors by spraying and patterned with oxygen plasma using a hard mask. Nickel was plated on a cup plater with back side contacting. Lines of 62 μm width have been realized. However, the plating selectivity was not sufficient and some ghost plating was present on the SAM covered area (**Figure 7**). After optimization of spraying parameters and of the patterning, 20 μm wide lines and selective plating have been realized (**Figure 8**)

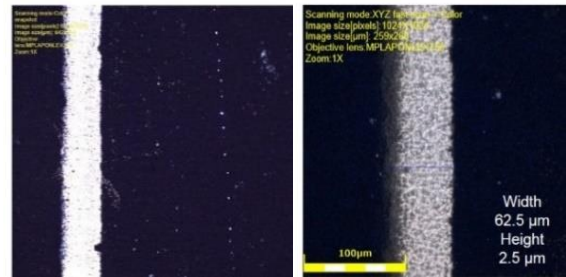


Figure 7: Scanning confocal microscopy images of a HJT cell precursor with SAM mask, after Ni plating.

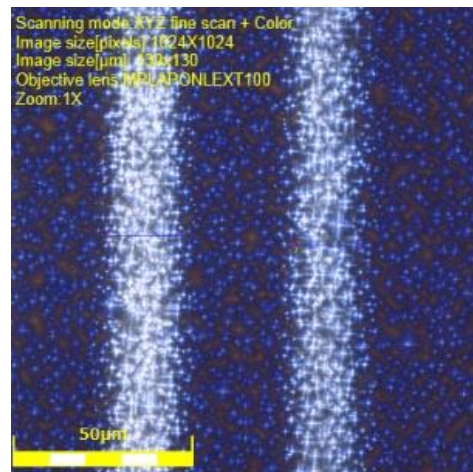


Figure 8: 20 μm wide lines after Ni plating on a heterojunction cell precursor with SAM mask.

5 FORMATION OF A COPPER SEED LAYER BY ELECTROGRAFTING ON ITO

The principle is depicted in **Figure 9**. Benzodiazonium salts react at the cathode and are covalently bonded to the surface. In case a copper salt is present in the electrolyte, the copper ions are trapped within the electrografted layer and also reduced. [14].

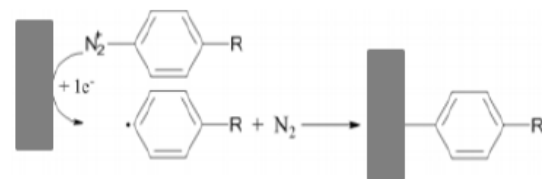


Figure 9: Schematic of electrografting

For this purpose, a diazonium compound having good complexing properties for copper ions was selected. After optimization of the electrolyte composition and of the deposition potential, homogenous copper-rich films up to 300 nm thickness have been obtained on polished silicon with ITO (**Figure 10**). The focus of current experiments is on further improvement of the electrolyte composition and of the patterning.

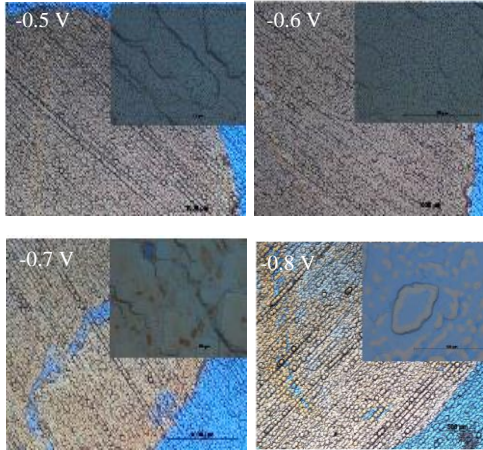


Figure 10: Electrografted copper layers deposited at different potential. Films are more homogenous at -0.5 and -0.6 V than at lower potential.

6 ITO REDUCTION

The adhesion of metal layers electrodeposited directly on thin conductive oxides is not sufficient for metallization of heterojunction cells for standard interconnection with soldered ribbons. Through reduction of the topmost ITO layer to form a thin metallic layer, the adhesion of subsequently electroplated metal is improved.

After several iterations good plasma conditions were found for appropriate ITO reduction. The ITO reduction has been confirmed by lowered sheet resistance and XPS measurements. Optimization of the plasma parameters is ongoing to fully eliminate the remaining minor impact on cell passivation.

Table 3: Sheet resistance after H₂-plasma reduction.

Sample	R _{sheet} [Ω/square]
As deposited	339
500W ICP-H ₂	156
700W ICP-H ₂	81

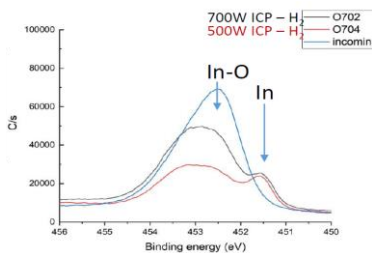


Figure 11: XPS measurement on reduced ITO

7 SUMMARY

The results obtained so far within the Ameliz project are encouraging. Partially in an early stage of development, it has been confirmed that the new patterning approaches are principally feasible. A lot of work is still required to optimize the process parameters and to optimize the processes towards industrialization.

However, the work done and progress achieved on single process steps may form the base for a copper plating sequence applicable for PV production in terawatt range in the future.

The silver price has increased by more than 60% in the last months and the replacement of silver by copper seems to be necessary even before the production will reach terawatt levels [15].

8 ACKNOWLEDGMENT

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