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Demonstration of Back Contacted III-V/Ge Triple Junction Solar Cells

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Abstract. Lattice matched III-V/Ge solar cells are mainstream for Concentrator PhotoVoltaics (CPV). Having both contacts on the back side could increase efficiency thanks to reduced shading and would provide an alternative to wire-bonding, shingling and MIMs as interconnections methods. In this paper, we present the first demonstration of back side contacted lattice matched III-V on Ge solar cell (InGaP/(In)GaAs/Ge). A specific process was developed to fabricate solar cells with a V_{OC} of 2,38 V and a J_{sc} of 9,9 mA/cm². This result is a proof of concept and further developments should increase cell performance.

INTRODUCTION

The heart of a CPV system is the high efficiency solar cell, that is usually made of III-V/Ge (lattice matched, InGaP/(In)GaAs/Ge) with the emitter contact in the shape of busbar and metallic fingers on the front side and the base contact on the back side. The development of back contacted solar cells stems from two major incentives. (1) It should allow for lower front metallization area, lowering metallization shading [1] (2) It also provides an alternative to usual connection methods such as wire-bonding, shingling and MIMs [2], in order to simplify module assembly or achieve higher cell density. Making back side contacted solar cells using lattice matched, InGaP/(In)GaAs/Ge epitaxial structures would therefore be beneficial for CPV systems performance and reliability, while leveraging on the state-of-the-art material quality provided by years of research.

For silicon solar cells, there are 3 main approaches for back-contacted single junction cells fabrication [3]: Metallization Wrap Through (MWT), Emitter Wrap Through (EWT) and Back Junction (BJ). For multi junction cells, EWT is inapplicable as the upper junctions are usually grown by epitaxy, and BJ is inapplicable as well. Therefore, MWT seems to be the most viable option and it has already been presented in the literature [4, 5]. Itou *et al.* [4] present a triple junction cell grown upon a semi-insulant GaAs substrate which is not an active part of the device. Therefore, the through wafer vias used to achieve the contact transfer from front to back do not need any electrical insulation. Salvetat *et al.* [5] present an inverted dual-junction ($Ga_{0.51}In_{0.49}P/Al_{0.03}Ga_{0.97}As$) grown on a GaAs substrate with vias etched from the future back side of the cell and are electrically insulated by a Si_3N_4/SiO_2 bilayer.

In this paper, we present a generic fabrication method to make back side contacted triple junction solar cells and we demonstrate the first triple junctions InGaP/(In)GaAs/Ge solar cell with back side contacts.

EXPERIMENTAL

The main challenge for back side contacted multijunction solar cells fabrication resides in the etching, insulation and metallization of high aspect ratio (ratio between depth and width) vias holes. To achieve this, we propose to start

by conventional front side processing, followed by etching of a through cell via from the back side of the cell. The via is then insulated and metallized. Therefore, only few steps must be added compared to conventional fabrication methods.

As a proof of concept, we only use one single via per cell, located under a bus bar. This via is 420 by 280 μm to maintain its aspect ratio around $\frac{1}{2}$ and facilitate its fabrication (the device is 180 μm thick). As the whole etched area is under the bus bar, the loss of active material should not affect the cell performance as the area would have been shadowed anyway. The via is etched in two steps resulting in an isotropic profile in Ge and a tapered profile in III-V layers.

The process can be divided into 11 macro steps, detailed in Fig. 1. We start with a Ge wafer (170 μm) upon which the III-V layers have already been grown using MOCVD (Fig. 1. (a)). Standard cells with Anti-Reflection Coating (ARC) would require 6 steps while this process requires 12 steps (with ARC). It is too early yet to transfer this process to industry and therefore it is hard to clearly assess the added manufacturing cost of these cells. The process has yet to be optimized for both yield and costs. We hope that a part of the extra manufacturing cost will be recovered by the absence of wire bonding step when assembling the cell into the module.

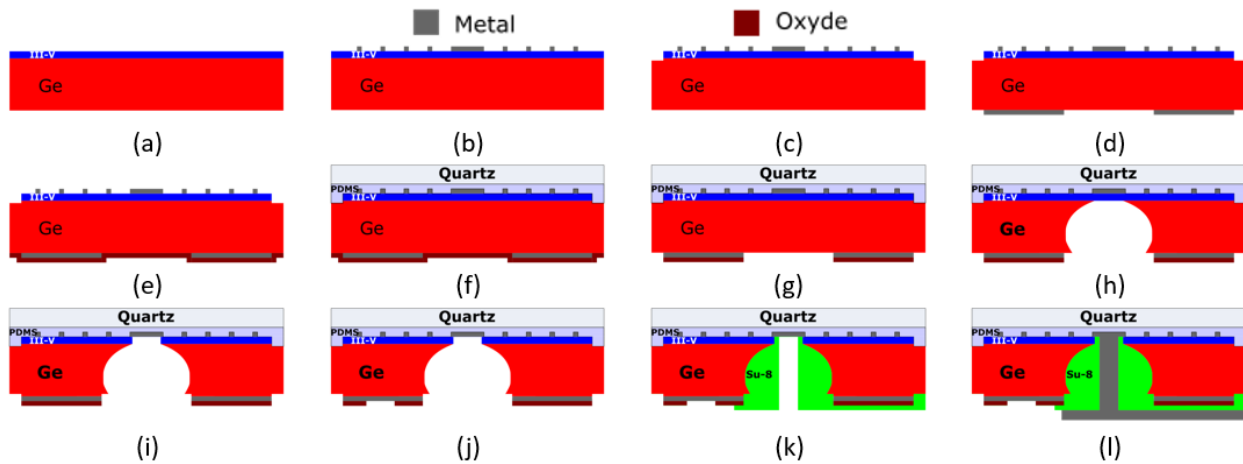


FIGURE 1. Cross section view of the 12 main steps of the process flow. (a) Initial sample state. (b) Front metallization. (c) Mesa etching. (d) Base Metallization. (e) Sacrificial silicon oxide layer deposition. (f) Front face quartz bonding. (g) Sacrificial oxide patterning. (h) Etching of the Ge part of the via. (i) Etching of the III-V part of the via. (j) Base contact opening. (k) Via sidewall insulation. (l) Via metallization and backside emitter electrode formation by serigraphy.

First, the front face (emitter) is fabricated (Fig.1. (b)). To do so, the front metallization is deposited and patterned by lift-off. The combination of metals, Ni/Ge/Ni/Au, was chosen to form an ohmic contact as well as to comply with the future via etching process. The ohmic behavior was confirmed by Transmission Line Method (TLM).

Then, mesas are formed by plasma etching (Fig.1. (c)). The goal is to etch the active layers out of the intended cells area. The etching process is done in an Inductively Coupled Plasma (ICP) machine, using $\text{SiCl}_4/\text{Cl}_2$ and H_2 . This process was developed to minimize plasma-induced damage [6].

Next step is to deposit the base metallization (Fig.1. (d)). Unlike usual solar cells we need to apply a pattern here to keep an area clear for the future via. To achieve the alignment between both sides of the device, a laser is used to drill holes through the sample. These holes are aligned on designated patterns out of the active areas on the front face and will be the alignment marks for the base metallization (Ni). Nickel is deposited by evaporation and patterned by lift-off, but the dimensions and tolerance margins are compatible with deposition through a shadow mask. At this point, the contact layer on the emitter side is wet etched and the device is similar to a standard cell except for the lack of ARC and the patterned base electrode.

A layer of protective silicon oxide is now deposited on the back side by Plasma Enhanced Chemical Vapor Deposition (PECVD (Fig.1. (e)). Following this step, the front face is permanently bonded to a quartz slide using PDMS [7] (Fig.1. (f)). This bonding technic protects the front face from any mechanical or chemical damage during the rest of the process. It also allows the front metallization to maintain integrity when exposed during the future through cell via etching. Such step may not be required though with optimized metal thickness and via dimensions. The front side is now finished. All remaining steps are performed on the back side.

The protective oxide is then locally removed by lithography and dry etching (Fig.1. (g)) to reveal the Ge surface where the via will be etched. Using lithography, a resist mask is patterned to allow for via etching. Each via is aligned directly underneath the central bus bar of the cell. The Ge is etched by SF₆ plasma in the ICP machine (Fig.1. (h)). The etch profile is isotropic, which is desired to simplify the insulation and metallization steps. This first etch step into Ge is 170 μm deep, and the lower layer of III-V material acts as an etch stop layer.

The resist mask used for the etching of the Ge part of the via is now stripped and, Ge itself acts as a hard mask for self-aligned III-V materials etching. The same plasma recipe as for the mesa etching is used here (SiCl₄/Cl₂/H₂). The etching endpoint is controlled via optical emission spectroscopy and the etching is stopped when the front metallization is revealed. The resulting via profile is first isotropic (Ge ~160 μm) and then tapered (III-V ~9 μm) (Fig.1. (i)). Its bottom consists in a thin metallic membrane which is part of a bus bar from the front metallization. The previous Quartz/PDMS bonding keeps this membrane mechanically sound.

The protective oxide layer is opened by dry etching to reveal the base contact (Fig.1. (j)) and SU-8 resist is spin-coated and patterned by lithography (Fig.1. (k)) to electrically insulate the via sidewalls. SU-8 is a permanent epoxy based negative resist.

Finally, Ag paste is screen printed to simultaneously form the back emitter contact and fill the via (Fig.1. (l)). Note that the via could be filled by electroplating or even light induced plating [8].

Figure 2. shows a SEM view of the cross section of the via after the full process. The cut missed the center of the via, which is why the SU-8 seems to separate the Ag paste and the front metallization. A void in the serigraphy paste is also observed but did not deter the cell performances. The very large thickness of the Ag paste (~100μm) and the void in the via result from manual deposition of the paste and could be solved by using a screen-printing tool.

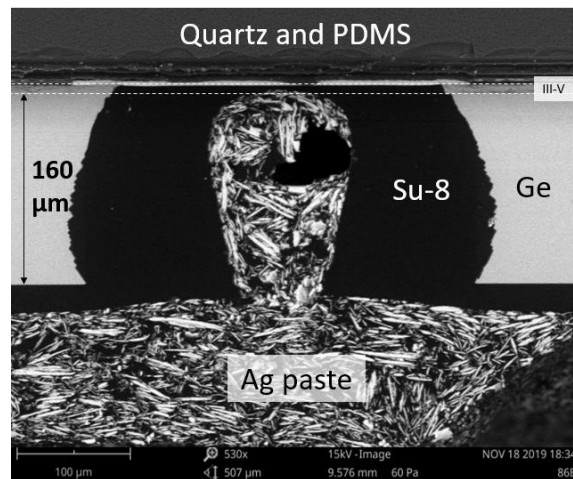


FIGURE 2. SEM view of the cross section of the finished via. Only 160 μm of Ge is left as it is also etched by the III-V etching step. The sample cut is at the edge of the via.

ELECTRICAL RESULTS

Figure 3. shows the I-V curve of one back side contacted cell measured under 1-sun illumination (red curve). The electrical characteristics of one cell of the same wafer but with conventional electrodes is also presented in this figure as a reference (grey curve). The V_{OC} of the back-side contacted cell is 2,38 V which is good, but slightly lower than the 2,48 V of the conventional cell. We attribute this V_{OC} decrease to manipulation of the sample as well as the Ge etch step that may create recombination centers at the sidewalls of the via in the germanium. Further developments such as cleaning and passivation steps should allow to increase this value. An unexpected behavior around V=0 V with a strong increase of the current density can be observed figure 3 for the back side contacted cell. Other back-side contacted cells showed similar behavior. We attribute this behavior to a reduction of the shunt resistance of the top and/or middle cell that appears during the via etch step. It is attributed either to non-volatile In etching by-products redeposition at the sidewalls, or to redeposited sputtered Ni from the front metallization. We expect dedicated cleaning processes could correct this problem.

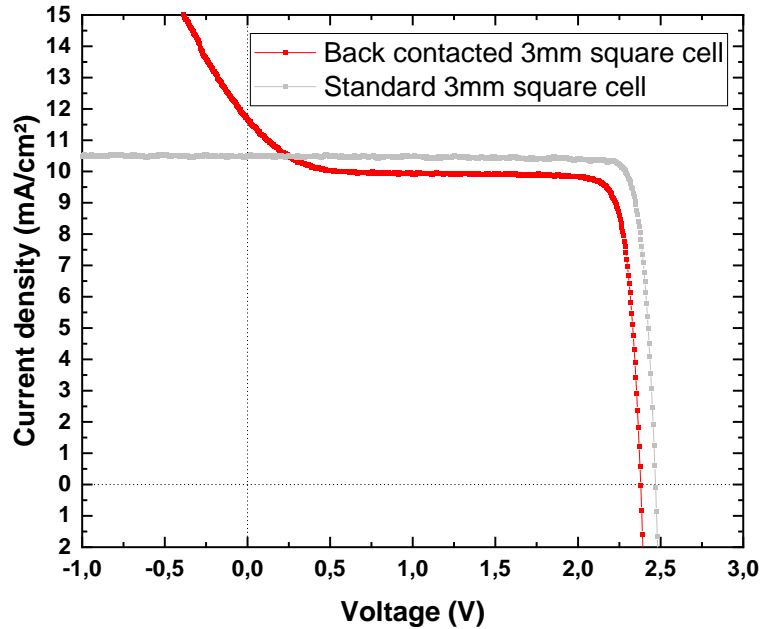


FIGURE 3. 1-sun J-V curve of a functional back contacted solar cell (3 by 3 mm square cell). A deviation caused by a shunt can be observed around $V=0$ V

Considering the J_{SC} value to be at the plateau, we get $J_{SC}=9,9$ mA/cm² which is a bit low (10,5 mA/cm² for the reference standard cell). This could be expected given the abnormal behavior around $V=0$ V. Fixing this abnormal behavior should result in higher J_{SC} values.

CONCLUSION AND PERSPECTIVES

We presented a fabrication method to make backside contacted solar cells with MWT structure, by appending 9 process steps to a conventional process for solar cell fabrication.

Functional triple junction back contacted solar cells were fabricated with one single large via centered below the bus-bar. Except for a small deviation around $V=0$ V, the cells operate as intended. The origin of this deviation has been identified and should be corrected in further developments.

To the best of our knowledge, these are the first lattice matched, InGaP/(In)GaAs/Ge back contacted solar cell to be fabricated; This opens the path to lower the metallization shading and increased efficiency as well as increased packing density in receivers.

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