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Abstract :

In this study, we describe an original method to build up a superficial and nanostructured porous polysilicon (POpSi) thin film on a Silicon substrate for thermoelectric (TE) applications. The POpSi layer is electrically isolated from the conductive Silicon substrate by an SiO_2 interlayer. In thermoelectricity, nanostructuration is commonly used to engineer the thermal conductivity of the material. Here, we show that the nanostructuration brought by porosification breaks the thermal conductivity of polysilicon layers (polySi) and has no detrimental impact on their Seebeck coefficient: a POpSi with up to 62% porosity has a Seebeck value maintained at about 255µV/°C when the standard polysilicon, it is built from, is n type with a carrier density of $3.4\times10^{19}/cm^3$. On the other hand, the benefit of the thermal conductivity reduction (by a factor of about 30) clearly over-compensates the degradation of the electrical conductivity measured in the POpSi layers, in terms of impact on the factor of merit ZT. Compared to the standard polySi layer, the ZT value is increased 25-fold in POpSi with 44% porosity (it increases from 0.004 to 0.1). Such a novel material is a good candidate for planar thermoelectric devices using Silicon technologies. As a demonstration, a modeling shows that if the optimum POpSi thin film is integrated into a planar TE microgenerator (µTEG) with suspended membranes, it would permit an improvement of conversion efficiency of up to 28% compared to a µTEG integrating the standard polySi layer counterpart.

Keywords : polysilicon, porous, thermoelectricity, thermal conductivity, nanostructuration, power factor, factor of merit.

1. Introduction

Over the last decade, the market of Internet of Thing (IoT) has expanded at a rate never seen before. The energy consumed by an IoT node can appear low, however if one takes into consideration the prospected count of IoT nodes that will be needed over the next half-century, the total energy consumption could reach several TW.h/year. Thereby, the spread of lots of new applications in the field of microdevices will be significantly hampered by a possible lack of energetically efficient and eco-friendly methods to feed them [1]. In this context, all innovative solutions to harvest energy from environment sources play a strategic role even to collect "small energy". This is the reason why Energy Harvesting (EH) activity gathers remarkable attention from the scientific community to master the conversion of waste energy into useful electrical one. In particular this can be done via thermoelectricity which convert waste thermal energy directly into electricity (thermoelectric or Seebeck effect [2-4]). Heat is one of the most abundant energy sources that can be harvested. For several decades, the thermoelectric (TE) effect has been predominantly exploited in thermal sensors [5,6] or in infrared detectors, where it displayed high sensitivities despite the low conversion efficiency [7-9]. However, over the past few years, it has shown a great interest in numerous EH research activities [10-13]. The biggest interest of electrical power generation from the heat lies with the inherent reliability of

TE devices due to its solid-state character and to the fact it does not require any fuel or moving part; this make μTEGs very suitable for a large variety of applications.

To quantify the maximum achievable power conversion efficiency of a thermoelectric material when used into a classical TEG (series of bulk p and n type legs), one generally calculate the dimensionless figure of merit ZT [2,3]. This factor is defined as a function of the electrical conductivity σ, the Seebeck coefficient α and the thermal conductivity κ of this material : $ZT = (\sigma \times \alpha^2/\kappa) \times T$. The product $\sigma \times \alpha^2$ is named power factor (PF) and is also used as a criteria of quality. Henceforth good TE materials must combine a high α, a high σ and a low κ. All these factors dependent on carrier density and on temperature in antagonist ways which complicates the succes in the optimisation of materials with a high ZT value [10,14]. In this context, many studies on thermoelectricity feature the benefit of nanostructuration to improve the fundamental properties of TE materials, particularly nanostructuring permits to tune the thermal conductivity to very small values [15-18]. This can be done by reducing the thermal lattice phonon contributions to κ. The use of nanostructures, of low dimensional systems or of nano-composite structuration, confines the phonon heat transport in quasi-2D or 1D or so. Thermal conductivities in such media are significantly reduced with values ten to much more times smaller compared to conventional bulk materials. As far as TE materials compatible with CMOS technology are concerned, nanostructuration is tentatively employed to improve micro-device performance [20-22]. The nanowire shape is so far considered as the best method for increasing ZT in Silicon [21-24]. Starting from values around 0.01 in bulk Si single crystal, ZT was reported to reach 0.6 (at room temperature) for nanowire 50 nm diameter [25], and even 1 at 680 K [26]. However, one has to keep in mind that, opposite to expectations raised a quarter of century ago, with the inaugurating work of Hicks and Dresselhaus [27,28], most of the nanostructuring methods used in many TE material systems, to improve their ZT, have scarcely proved to have any effective impact on Seebeck effect improvement (or PF) itself.

In this work, we report for the first time on the original fabrication and characterization of a novel nanostructured TE material composed of n-type porous polysilicon (hereafter named POpSi) as a new candidate for integration into EH devices. In a first part is presented the original method to anodize thin polysilicon (polySi) layers into POpSi and the technic to disconnect electrically this one from the silicon substrate on which it is grown. The manufacture of singular bar test thermopiles is then described. In a second part, the characterizations of the thermoelectric and electric properties are presented. Finally, in the last section is discussed the improvement of the factor of merit, due to the drastic reduction of its thermal conductivity.

2. POpSi, porous polysilicon layers

2.1 Fabrication of PS and of POpSi

Numerous studies have shown great interest of porous Silicon (PS) use as thermal insulator in Silicon technologies [29-32]. PS presents a thermal conductivity up to a hundred times lower than the one of single-crystalline Silicon, thanks to the nanostructuration brought by the numerous pores distributed in a tight mesh into the Silicon perfect crystallographic lattice. In this section, we show how anodization used for a poly-crystalline Silicon layer (polysilicon or polySi) lead to the fabrication of a new kind of nanostructured layer (the POpSi; porous polySi). The original fabrication method of POpSi is based on the same manufacturing process as the one of standard PS, added with a few extra technological steps in order to finally obtain a layer electrically isolated from its template.

Classical PS is often made starting from the polished surface of a single crystalline Si wafer, highly p-doped with Boron so its electrical resistivity is very low (about 0.01 Ω.cm). In our usual experience, the chemical etching that leads to PS is performed onto 3-inch 380µm thick Si(100) wafers, at room temperature, in a double tank-anodizing cell from AMMT®, with an electrolyte mixture of 27% fluorhydric acid (HF), 38% of deionized water and of 35% ethanol (CH3OH) (shown in Fig. 1-a,b) [33-35].

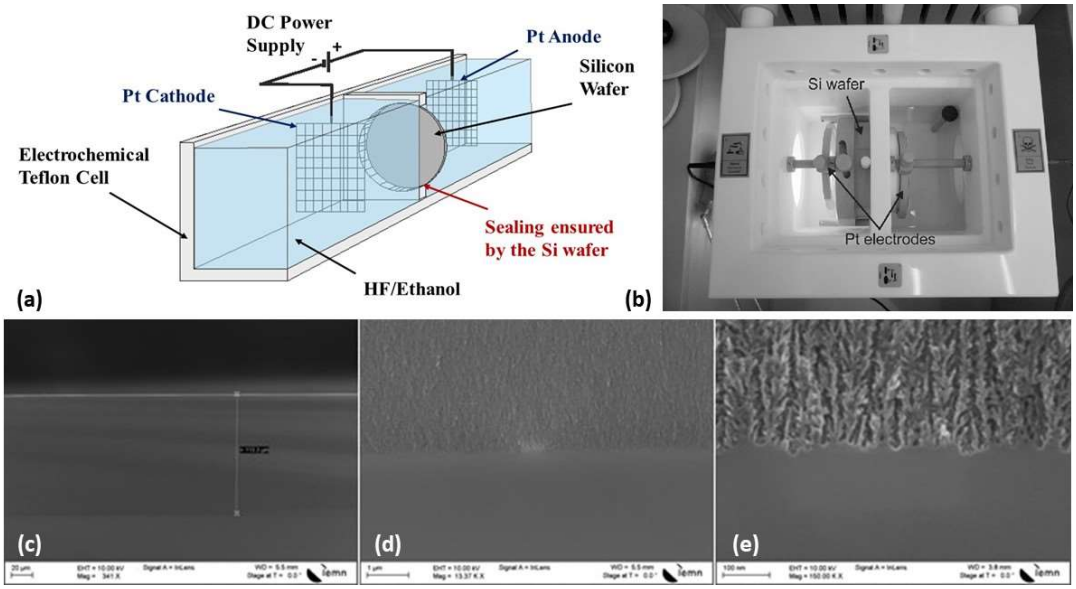

Fig. 1. (a) Schematic view of a double-tank anodizing cell, (b) Photograph of double tank anodizing cell (AMMT®), and (c,d,e) SEM cross section views of porous Silicon at different scales

The surface morphology, the volume microstructure and the thickness of PS are characterized by scanning electron microscopy (SEM). Fig. 1-c,d,e show typical pictures of a PS sample cross-section. The evolutions of PS thickness and its porosity as a function of anodizing conditions, ie. time and current density, is given in Fig. 2. The porosity of the material is defined by the percentage of air relative to Silicon, which is generally determined by gravimetric method [32,35]. The porosity value is given by the ratio $\frac{m_1-m_2}{m_1-m_3}$, where m_1 and m_2 are the masses of the Si sample before and after the anodization respectively and m_3 is the mass after removing of the porous layer in a sodium hydroxide solution. The masses of samples are weighed using a Mettler Toledo® microbalance with accuracy (~0.1µg). We can control porous Si with a porosity from a few % to some 85%. Those porosification trends obtained for bulk Si (ie in PS) are our benchmark to carry out the porosification of polySi films.

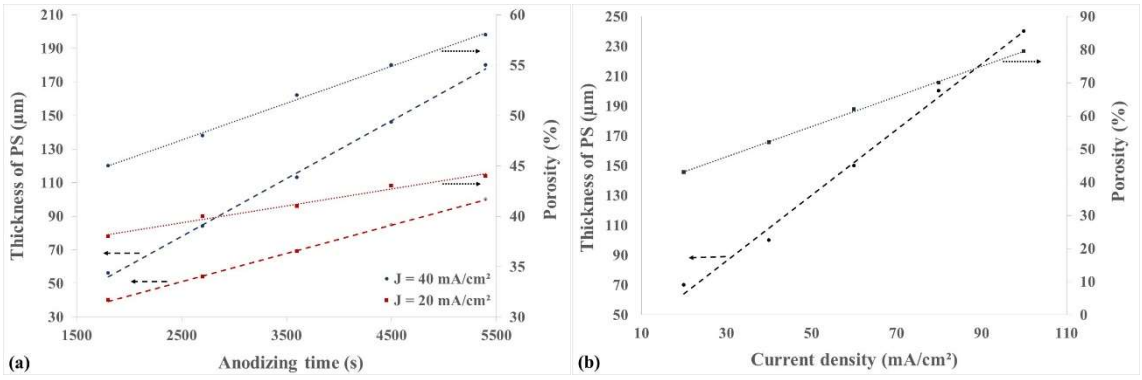

Fig. 2. Evolution of thickness and porosity of porous Silicon (PS) as a function of (a) anodizing time (for two current density 20 mA/cm^2 and 40 mA/cm^2) and, of (b) current density for a constant anodizing time of 60 min.

If electrochemical etching for the technological fabrication of PS has been widely described in the litterature [28-35], and is also regularly used by us for developing thermal discontinuities into templates of micro heat-flux sensors [36], the built up of a superficial thin porous layer, electrically disconnected from the bulk Silicon on which it is deposited, remains a challenge. Usually, in our above described etching process, the Si substrate ensures the sealing between the two tanks contenting the electrolyte (Fig. 1) and in which is dipped two platinum electrodes used to inject an electrical current. This latter is essential to allow the reaction between fluorine, hydrogen and silicon atoms. The injected current flows through the highly-doped conductive Si wafer perpendicularly to its surface.

Thereby, taking into account these experimental conditions, it seems easy to extrapolate to the fabrication of POpSi by anodizing a highly-doped polySi layer grown by LPCVD (Low Pressure Chemical Vapor Deposition) directly on a highly-doped Si substrate and of course preferably one would use the same type (p) of polySi layer as the type of the substrate (p++). However, if one wants to functionalize the superficial POpSi layer into an active media for a planar thermoelectric microdevice application, an insulating sublayer must be embedded between the initial polySi layer and the Si substrate. This is what we have done, *in a particular way* using silicon dioxide (SiO_2), in order to adjust periodic conductive vertical channels through the insulating sublayer so the anodization current can flow anyway through the wafer, for the porosification. Another singular new element is that we choose for this first work to have standard n-type polySi layer deposit.

In Fig. 3 is given the flow chart of the POpSi fabrication process into ribbons that we used. Ribbon shape is appropriate for two reasons: i/ uniform anodization of a full 3-inch wafer and ii/ tailoring of POpSi surfaces, insulated from the substrate, enough large to design characterization specimens for the determination of TE properties. In particular, stripes are perfectly shaped to be used as part of plated thermocouple strip. In other regions of the wafer small squares or bars are designed for the electrical characterisation using Van der Pauw-Hall method. The technological steps are as follows:

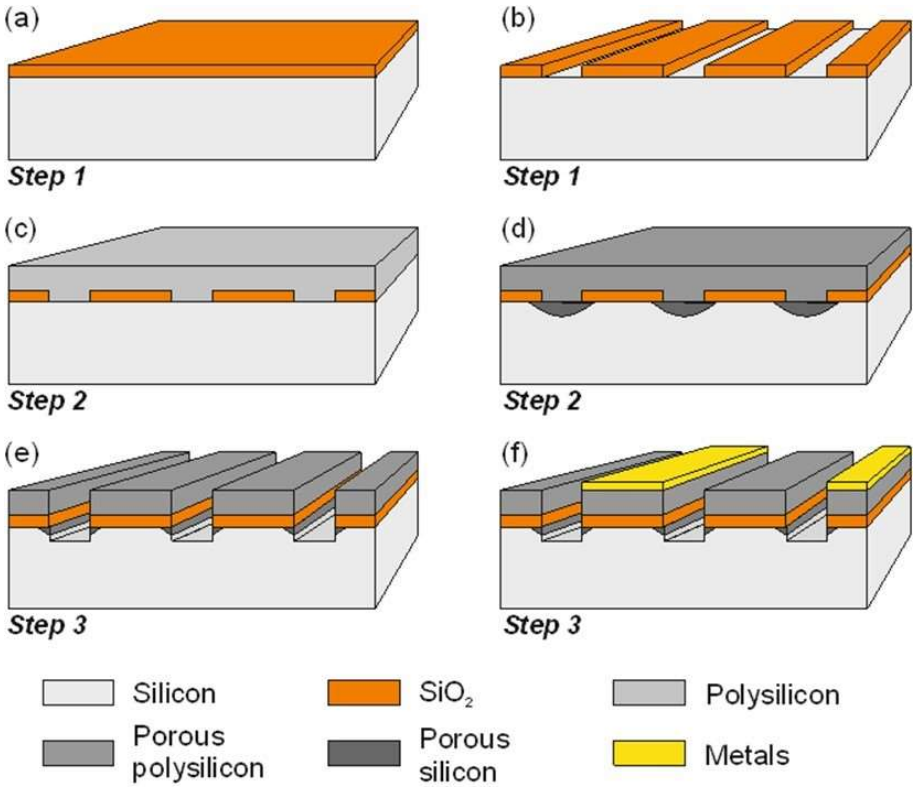

Fig. 3. Flow chart of the porous polysilicon layer (a to d) and plated thermocouple strip (f).

- Step 1: First, the Si wafer is completely cleaned by a typical piranha etch of highly concentrated sulphuric acid (99%) and HF (purity 50%) mixture in ultrasonic cleaner until the end of the bubbling phenomenon on the wafer surface. The organic pollutants that contaminate the Si surface are removed into a 10% HF acid/DI water solution, and thoroughly rinsed by DI water. A low-temperature SiO_2 layer, 260 nm thick, is then deposited on the wafer (Fig. 3.a) by LPCVD in a Tempress furnace. It is etched to be shaped into long strips, 200 µm wide (Fig. 3.b). The interstrip is 50µm wide. Almost all the thickness is etched by Reactive Ion-Etching (RIE), using fluorinated gases then chemical etching in 5% HF acid is used for the last tens nanometers to avoid deterioration of the Si surface.

- Step 2: A 1 µm thick polySi layer is deposited on the SiO_2/Si(100) wafer by LPCVD. It is in-situ doped with Phosphorous (n type). The microstructure of such a polySi layer is columnar. The electrical properties of the polySi layer are $n \sim 3.7 \times 10^{19}/cm^3$ and $\rho \sim 0.012$ Ω.cm (doping level is selected to obtain polySi which has almost the same conductivity as the substrate). This layer is electrically connected to the Silicon substrate through the strip shaped holes into the SiO_2 sublayer (Fig. 3.c). The anodizing is performed in the same conditions as described earlier for classical PS. The current is supplied by a direct current (DC) electrical source and the current density is controlled to be maintained in a range between 10 mA/cm² and 200 mA/cm². The electrolyte in front of the substrate is electrically connected to the cathode and its potential can be considered as negative, whereas the substrate can be considered being the anode due to its rear face connected with the positive electrolyte (in which is immersed the anode). In Fig. 4.a. is shown a SEM zoom on the cross-section of one of the stripe. During anodization the electrical current flows through both the polySi layer and the Si substrate. In the areas where polySi and Si are electrically connected, the current lines were either not deflected or slightly deflected. On the opposite, the SiO_2 mask areas lead to a strong deflection of the current lines in the polySi: as seen in Fig. 4.b. SEM image, the line features, which are alignment of mesopores, in the POpSi sample cross-section, symbolize the current pathway during anodization. The electrochemical etching of polySi and Si follow the current line directions, with engraving speeds of a few tens of nm per second. The porous polySi (POpSi) obtained presents a singular columnar structure (different from the polySi one) with ramifications perpendicular to the surface sample and has pore size from 5 to 15 nm (Fig. 4.c). To make sure that all the polySi thickness will be entirely anodized, the etching time was maintained longer than necessary. Hence, the Si substrate is also anodized, as seen in Fig. 4.a. In most trials, there was only a few nanometers of polySi residual layer left upon the SiO_2 interlayer (Fig. 4.d), everywhere else it has become POpSi. However, this method was not systematically efficient and will need further tuning.

- Step 3 : The last part of fabrication, shown in the Fig. 3 chart, consists to design the superficial thermopile shaped into a zig-zag strip from the porous polysilicon. To isolate electrically the POpSi and the substrate, both are periodically etched by RIE until excavation of the deep trench (see Fig 3.e). A layer of metals Ti:10 nm/Au:200nm (the second thermoelement) is periodically evaporated on POpSi stripes to form series of long thermocouples as shown in the next section (2.2). On each 3-inch wafer it is possible to fabricate 16 thermopiles.

- Step 3–bis: In parallel to the etching of thermopile zones in each 3-inch wafer, using the same set of lithography masks, other areas are etched into several clover-leaf shaped samples and Hall-bars to be used for Van der Pauw–Hall electrical characterisation (see picture in section 3). In these cases, the metal plating is carried out only on area dedicated for four-probe test

contacts. Their fabrication is less complicated than the thermopile; this is the reason why a focus is made hereafter only on these later.

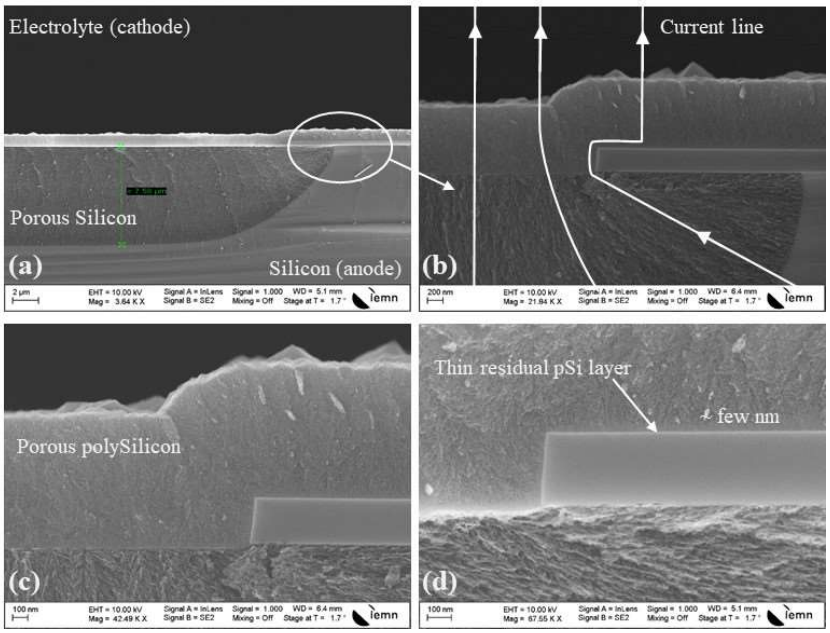

Fig. 4. SEM images of : (a) anodization of Si and polySi into PS and POpSi, (b) electrical current lines through the sample, (c) nanostructuration, and (d) residual polySi layer after anodization .

2.2 Fabrication of POpSi/gold thermopiles

Long plated thermocouple (TC) bars can be used for thermoelectric characterizations. Typically, we made in this work 25 mm long thermopiles. However, the realization of POpSi with the previously described anodization method requires, for uniformity reasons, to define stripes with a width of the order of 200µm. Therefore, in order to avoid high electrical resistance thermopiles, we made artificially wider TCs by using four legs of POpSi connected electrically in parallel as the first thermoelement. The second thermoelement is the gold plated ribbon (deposited upon a single stripe POpSi). Fig. 5.a is an illustration of the electrical connection in a thermopile made of one single TC. Each of the real experimental thermopiles have 3 TCs in series and a picture of one of them in given in Fig. 5 b,c,d.

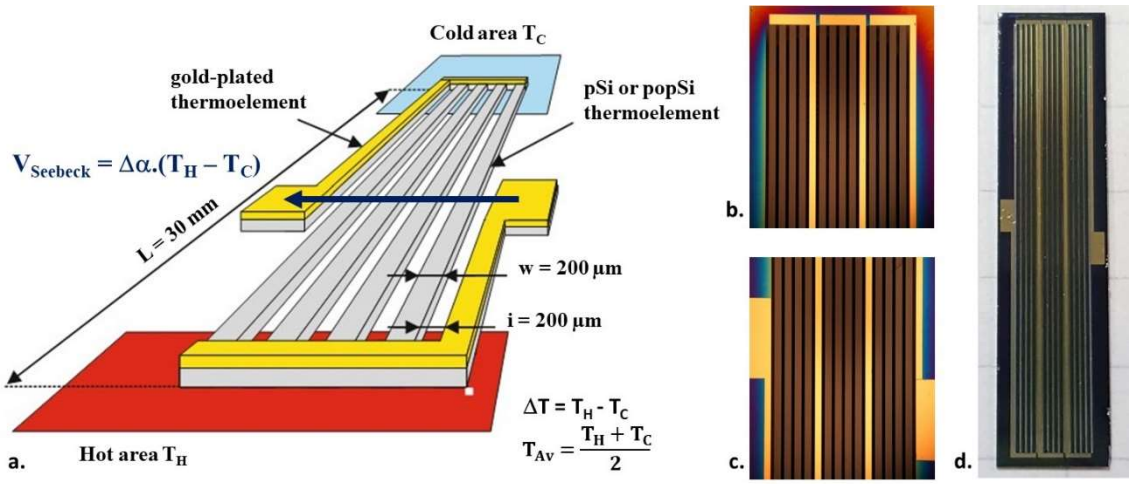

Fig. 5. (a) Illustration of the electrical connection in a thermopile with one TC made from POpSi**,** and photographs of a thermopile with 3 TCs in series: (b) extremity of the TCs, (c) Contact pad disposition and (d) whole Seebeck test barrete

The two metal contact pads of the thermopile have been arranged along both sides of the thermocouples (Fig. 5.c). For the measurement of the Seebeck coefficient, the heat flow is imposed between both extremities of the strips (TC junctions, cold and hot areas Fig. 5 a,b).

3. Characterization of POpSi layers

3.1 Porosity

In this part, we determine the electrical and thermoelectrical properties of numerous porous polysilicon POpSi wafers as a function of the level of the porosity. To this aim, we have realized different anodizing test structures from polySi wafers with five different current densities. The polySi layers were simultaneously grown by LPCVD on 3-inch Si substrates periodically masked with SiO_2. Table 1 gives the estimated porosities of the POpSi test structures extrapolated from measurement made with PS calibration samples (same conditions). Indeed, the thicknesses of POpSi layers are too thin and therefore too light, to allow their porosity measurements by the gravimetric method. The pSi_{ref} specimen is the non-anodized polysilicon used as the reference layer; $POpSi_1$ to $POpSi_4$ are the four POpSi layers made with four different current densities and time.

Based on Fig. 1.b, the etching speeds have been estimated to be about 1 to 4 µm/min (for respectively 20 to 100 mA/cm² current densities). To make sure that the whole polySi layer has been anodized, as underlined before, anodization/etching times have been chosen larger than those required, even though substrate is also engraved. The corresponding porous Silicon regions will be removed anyway by RIE etching. The whole porous thicknesses (cumulating POpSi and PS) were measured by SEM, and increases with the anodization current (also reported in table 1).

pSi and porous POpSi Samples	Current Density (mA/cm²)	Anodizing Time (s)	Estimated Porosity (%)	Total Porous Thicknesses (pSi and Si) (µm)
Polysilicon pSi_{ref}	-	-	-	-
Porous $POpSi_1$	20	180	44	~ 3.2
Porous $POpSi_2$	40	180	52	~ 4.5
Porous $POpSi_3$	60	150	62	~ 6.3
Porous $POpSi_4$	100	120	80	~ 8.1

Table 1. Manufacturing parameters of porous polysilicon layers.

3.2 Electrical properties

The Van der Pauw–Hall method is used to measure the electrical properties of the five polySi and POpSi thin films. An Accent© probing station using four-probe heads is used to determine properties such as resistivity and doping level (sheet carrier density). Such measurements were carried out at room temperature on clover-leaf-shaped or bridge-type samples (Fig. 6 a,b) located in between thermopile samples. The relatively large Au contact pads permit to reduce contact resistances.

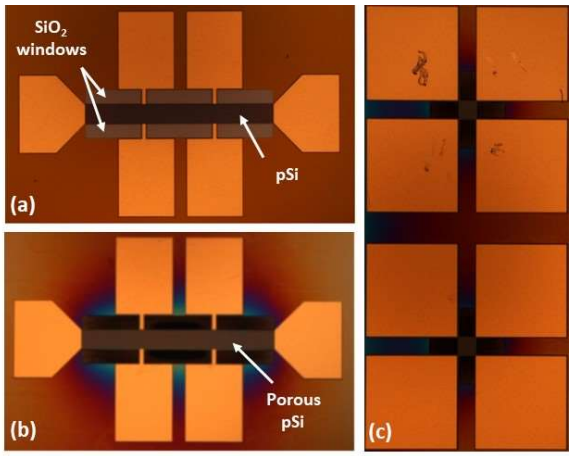

Fig. 6. Optical photographs of : Typical Hall bar or Van der Pauw geometry used for transport measurements (a) of polySi, (b) of porous polySi and (c) clover-leaf shaped pattern.

Table 2 presents the averaged values of the measured electrical properties of those polySi and POpSi layers (we remind that all of them are 1 µm thick). Each type of POpSi layer was characterized several times (at least ten test samples were used, the uniformity within each wafer was pretty good).

pSi and porous POpSi Samples (1 µm)	Porosity (%)	Sheet carrier density n (/cm²)	Sheet resistance (Ω/□)	Mobility µ (cm²/V.s)	Electrical resistivity (Ω.cm)
Polysilicon pSi_{ref}	0	$3.4\ 10^{15}$	136	13.5	0.014
Porous $POpSi_1$	44	$2.7\ 10^{15}$	180	12.7	0.018
Porous $POpSi_2$	52	$2\ 10^{15}$	420	6.8 (*)	0.042
Porous $POpSi_3$	62	$5.3\ 10^{14}$	1390	8.5	0.139
Porous $POpSi_4$	80	$4.6\ 10^{12}$ (? *)	> 135000	< 7	> 13

Table 2. Electrical properties of polySi and porous POpSi layers using the Van de Pauw method. (* see text)

The measurements show that the electrical resistivity increases with the porosity. Obviously, the POpSi layers remained n type. The reduction of the electrical conductivity is related to both, the reduction of carrier density (n) and of carrier mobility (µ). This is consistent with the evolution of the material microstructure: the higher the porosification, the narrower is the polySi un-etched skeleton and also the larger is the surface of the interface between Si and meso-voids (and likely interface is oxidized at the nanoscale). Those two changes disturb the free carriers (electrons here) by trapping them and scattering them in a more and more severe way as porosity is increased (lowering of n and µ). The measured mobility of $POpSi_2$ (52% porosity) seems to be smaller than expected compared to $POpSi_3$ (62% porosity). The electrical properties of $POpSi_4$ (80% porosity) are so much degraded that they could not be measured in a reliable and reproducible way with the Van der Pauw method nor with Hall bar. It required a very small current (~ 1µA) to at least get an approximate value of the carrier density. Also, for this very porous POpSi, the resistivity varies from one thermopile to the other and is pretty high in all cases (see table). To sum up, one can state that up to some 52 % porosity, the electrical properties are not too much degraded (factor of 3.4 on the resistivity).

3.2 Thermopower

The homemade set-up used to determine the thermoelectric power (Seebeck coefficient) is compatible with thin planar materials and for temperature in the range 25 - 105°C. The Seebeck characterisation was carried out on the long thermopiles that were described in the previous

section. The characterization bench is made of two copper blocks that can be independently heated in order to impose a temperature difference ($\Delta T = T_{Hot} - T_{Cold}$) between the extremities of the thermopile (each end being clamped into one of the Cu blocks). Dedicated hardware and software ressources have been developed to monitor and regulate the temperatures of both Cu pieces with an accuracy of about 0.2 K (with Class A Pt_{1000} sensors). The temperature of each TC junction is the same as the one of the copper block in which it is embedded. This one is supposed uniform due to the high thermal conductivity of copper.

The measurement protocol consists in i/ applying a temperature difference ΔT between the junctions of the thermopile that is kept at a given average temperature corresponding to $T_{Av} = \frac{T_{Hot}+T_{Cold}}{2}$), and then ii/ increasing the temperature gradient ΔT from 0°C to 10 or 12°C in 2 or 3°C steps (Fig. 7.a). The Seebeck coefficient at T_{Av} can then be deduced from the slope of the linear curve $V_{Seebeck} = f(\Delta T)$: $\alpha = \frac{1}{n}\frac{\partial V}{\partial \Delta T}$ (where n is the number of thermocouples). Fig. 7.b shows the Seebeck coefficient measurements $\alpha(T_{AV})$ of eight thermopiles in pSi_{ref} wafer for T_{AV} in the range of 25°C to 75 °C (α deviation is lower than 5%); each value $\alpha(T_{AV})$, in each curve, being calculated from the slope as described.

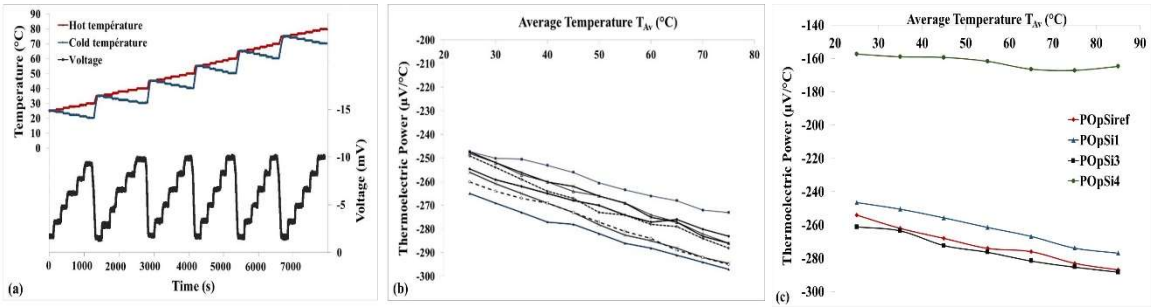

Fig. 7. (a) Measurement protocol, (b) Thermoelectric coefficient of eight samples of pSi_{ref} versus temperature, and (c) Thermoelectric coefficient of different POpSi layers.

Using this characterization method, Seebeck coefficients $\alpha(T_{AV})$ for the five studied POpSi layers is carried out. In all cases $\alpha(T_{AV})$ increases slowly with the temperature T_{AV} as exemplified in Fig. 7 .c, where are reported one $\alpha(T_{AV})$ plot for each category of POpSi. This behavior of POpSi is consistent with the classical one of bulk Si or of polySi films. The room temperature (25°C) value (averaged over several thermopiles) is given in table 3. On the other hand, the electrical resistance of each thermopile is measured and is checked for consistency with the calculated value obtained from electrical resistivity Van der Pauw specimens.

	Polysilicon pSi_{ref}	**Porous $POpSi_1$**	**Porous $POpSi_2$**	**Porous $POpSi_3$**	**Porous $POpSi_4$**
Seebeck coefficient α (µV.K^{-1})	-255	-248	-10 to -30	-260	-160
Electrical Resistance (kΩ)	13	19	8	140	> 2 to 6 MΩ

Table 3. Average values of Thermoelectric coefficient of polySi and POpSi layers and electrical resistance of the test thermopiles (at 25°C).

As shown in Table 3, the electrical resistance of the thermopile made from polySi and POpSi layers increases with the layer porosity, as expected. The experimental values are consistent with the calculated ones, except for the electrical resistance of the $POpSi_2$ thermopiles: the average found, 8 kΩ, is almost ten times lower than the calculated value. This issue could be clarified afterward : it is certainly due to a short circuit between the thermopiles and the highly

doped Si substrate (technology process problem on strips). Independently of this, excluding $POpSi_2$ case (with its short-cut issue) one can see that a porosity up to 62 % seems not to impact the value of the Seebeck coefficient: the thermopower is kept in the range of the polySi layer value: 248 or 260 µV/K versus 255µV/K. Incidentally, we see that porosification of n-type polySi layers lead to nanostructured POpSi layers without any improvement of Seebeck coefficient. This points out our introduction statement: the seemingly scarcity of thermopower enhancement by any nanostructuration, as unfortunately commonly seen in TE community for several kind of nanostructured materials. As far as the case of $POpSi_4$ (80% porosity) is concerned, opposite to the difficulty we met for measuring Hall effect, we are able to measure α for several samples and it ranges between -160 and the -300µV/K ; the negative sign is a proof that the layer remains n type, however the carrier transport is likely no more classical.

4. Thermal conductivity and impact on the figure of merit

As viewed in the introduction, to assess the performance of a new thermoelectric material, the most used parameters are the power factor $PF=\sigma.\alpha^2$ and the dimensionless figure of merit $ZT = (\sigma.\alpha^2/\kappa)\times T$. Actually, for a planar TEG using a thermopile instead of bulky vertical legs, the maximum achievable output electrical power (P_{MAX}, seen hereafter) is proportional to the PF and to the square of the temperature difference ΔT. Whereas ZT value is not related to the planar device performance: indeed κ impact is damped by the thermal contribution of the embedding layers in planar topologies. We already underlined this for the case of IR planar microsensors (µSIR) in [22]. Thermal conductivity κ indirectly contributes into ΔT. Anyway, the figure of merit ZT can be calculated as an indicator of material "quality" in case this material was used for bulky device.

The main benefit expected for the POpSi layers is clearly the lower values of their thermal conductivity compared to polySi layer counterpart. In this work we did not carry a direct study of this parameter on the thin layers : the strip shape of our current POpSi layers does not allow a simple measurement with a method as 3ωor so (alternative are looked for). Actually we extrapolate thermal conductivy value in POpSi from the experience we got from the measurement of κ into bulk PS material. Many studies have shown that the thermal conductivity of anodized Silicon, with a porosity superior to 40% and pore sizes about 10 to 20 nm, is significantly reduced due to the collapse of the thermal lattice contributions [32,37,38]: in this kind of PS with a high porosity, the thermal conductivity is a hundred times lower than in single crystalline Si. In our case, we have measured for instance κ_{PS} = 1.9 W/m.K for 54% porosity whereas κ_{Si} = 140 W/m.K [39]. For severe porosity (higher than 70%), we even measured κ_{PS} ~ 0.6W/m/K.

Henceforth, if we assume that porosification of a polycrystalline Si layer (polySi), which κ_{pSi} is ~31 W/m/K [40-42], into a POpSi layer with 44% to 80% porosity, behaves thermally (in terms of the scattering of phonons) with an impact of the same order of magnitude as for the porosification of single crystalline Si (and assuming a possible extra effect due to the evolution of polySi grain boundaries during porosification), one can expect that κ_{POpSi} will be lower than 1 W/m/K thanks to what we can name the ***double nanostructuration*** : if κ is divided by 70 as for our PS, one would find κ_{POpSi} varies from 0.5 down to 0.2 when porosity varies from 44% to 80%. So c**onservatively**, without making too much simplification, one can say that κ_{POpSi} is at maximum 1 W/m/K. Considering such a value of POpSi thermal conductivity, leads to the PF and ZT calculated values given in Table 4 for the 5-studied POpSi layers:

	Polysilicon pSi_{ref}	Porous $POpSi_1$	Porous $POpSi_2$	Porous $POpSi_3$	Porous $POpSi_4$
Power Factor $PF = \sigma.\alpha^2$ ($\mu W/cm.K^2$)	**4.64**	3.41	1.4*	0.49	0.002
Thermal conductivity κ (W/m.K)	**31**	~ 1	~ 1	~ 1	~0,6
Figure of merit $ZT = (\sigma.\alpha^2/\kappa)xT$ (at 300K)	**0.004**	0.1	0.04 *	0.014	$6\ 10^{-5}$

Table 4. Power factor $PF = \sigma.\alpha^2$ and estimated dimensionless figure-of-merit $(\sigma.\alpha^2/\kappa).T$ (at 300K) of polySi and POpSi layers (estimated κ for porous layer, see text).
(* PF value calculated assuming a Seebeck coefficient in between $POpSi_1$ and $POpSi_3$)

Though the power factor in POpSi is significantly reduced due to the anodization (a little for 44% porosity, much severe for 62%), the improvement of thermal properties can somewhat compensate this diminution if one compare the values of the figure of merit. The best ZT, ~0,1, is obtained for $POpSi_1$ layer (44% porosity), which is a pretty good values compared to standard polySi (25-fold increase).

To go further in porous polysilicon optimization, we can potentially target an even higher ZT in POpSi, if we consider starting the anodization from a polySi layer with a higher PF: for instance with a very highly B-doped and annealed polySi layer in which the best PF is about 21 $\mu W/cm.K^2$ (ie. 4.5 higher PF than in pSi_{REF}) [43]. In such a situation if the anodization of a stack $polySi(p)/SiO_2/Si(p^{++})$ behaves as efficiently as in our current experiment, $polySi(n)/SiO_2/Si(p^{++})$, we would succeed to fabricate POpSi with $ZT \sim 4.5xZT(POpSi_1)$, ie $ZT \sim 0.45$, which is a value that is getting closer to the published values experimentally found in another type of nanostructured Silicon: the Si nanowires [24-26]. The interest of thin layers compared to forest of nanowires being the "a priori" ability to tailor large-scale devices.

As far as thermoelectric devices applications are concerned, for the devices where is needed the thermal heat to flow into the whole bulk substrate (as in micro-heat flux sensors), the thermal conductivity reduction of the planar TE layer induces no relevant increase of the performance. The sensitivity will not be much affected. However, using porous active layers could provide an real advantage in other planar TE devices in which heat transfer are superficial as in µTEGs or µSIRs based on membranes [9,13,22].

For instance, if we model several µTEGs realized onto suspended membranes (4 or 5 membranes, optimum geometry we have described in [44], integrating either an active TE layer built of POpSi (as $POpSi_1$) or integrating a simple polySi (as pSi_{ref}), we can deduce the performance modification by calculating $P_{max}=N^2.\alpha^2\Delta T^2/4/R_{INT} = PF.\Delta T^2x(\text{geometrical-factor})$, the maximum achievable output power on an adapted load (N and R_{INT} being respectively the number of TC and the internal electrical resistance of the thermopile, R_{INT} is directly proportional to ρ, assuming no parasitic contact resistance). For a fixed amount of heat flux to harvest, the difference of temperature ΔT experienced at each TC of the thermopile is directly related to κ_{POpSi} and can be calculated using COMSOL® multiphysic thermal tool simulation. For 1W to harvest arriving on the surface of a 5-membrane based TEG (~ 34mm², 560 thermocouples), we find that ΔT increases when κ reduces from 31 to 1W/K/m following the monotonous trend shown in Fig. 8. The difference odf temperature ΔT is increased by some

32 %, for 5 membranes based µTEGs (it goes from 68K to 90K); whereas the experimental PF varies from 4.65 µW/cm.K^2 (pSi) to 3.4 µW/cm.K^2 (POpSi$_1$ layer). This leads to P_{max} increasing by a factor of ×1.28: P_{MAX} varies from 123 µW/cm² to 158 µW/cm², which is a significant improvement.

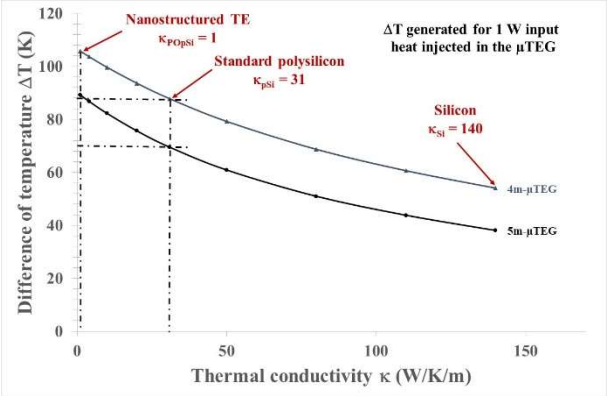

Fig. 8. ΔT between the junctions of the thermopile in planar µTEG (for 1W input heat injected) calculated using Comsol®. Evolution as a function of the thermal conductivity of the embedded TE thin layer (here Silicon based).

Such an illustration shows that though the electrical properties are slightly reduced, this can be clearly compensated by the benefit due to the hermal properties modification: globally it leads to an improvement of the device performance efficiency of up to 28% just by porosification, all other parameters being the same.

Finally, further work is to be continued also to better clarify what is the optimum porosity (% and "orientation" of meso-pores ramifications) and optimum doping level and nature (n or p type initial polySi). In the case of bulk free-standing PS [45,46] it was found that the optimum porosity to get the maximum value for Seebeck coefficient is around 51% [45]. Optimum POpSi porosity and carrier density leading to higher PF and /or ZT values once found will then be effectively integrated into membrane based µTEGs.

Conclusion

This article presents an original porosification method of a superficial n-type polysilicon layer, electrically disconnected from its conductive p-type Silicon substrate on which it has been grown. The study focus on the possible improvement of the thermoelectric properties induced by the anodization process in the resulting porous POpSi layers. Although the electrical properties have been degraded, yet the benefit on the thermal conductivity clearly compensates it, which results into a 25-fold increase of the factor of merit between polySi and POpSi layers, when porosity is set at 44%. The described new method of extra nanostructuration in polysilicon layers should eventually permit to fabricate membrane-based planar thermogenerators with improved conversion efficiency by a factor up to ×1.3. Forthcoming work is being oriented towards further improvement of the thermoelectric properties of POpSi porous layers. Among the new routes considered, the p-type doping of initial polySi by B implantation seems to be a promising solution to dispose of a clearly higher power factor. A better tuning of porosity between 40 and 60% is also looked for. Finally, the manufacture of POpSi where mesoscopic ramifications are made in the plane of the thermopile should certainly improve even more the results.

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Conflicts of Interest

The authors declare no conflict of interest.

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