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Keywords

«EMC/EMI», «Converter circuit», «dc/dc converters», «Silicon Carbide (SiC)», «Transformer».

Abstract

This paper presents a system-level EMI investigation in a new 3-phase 1.2kV 100kW insulated DC/DC converter. In this prototype, achieving full operation was prevented by false triggering of semiconductors due to large common-mode current through gate drivers. A passive filter embedded into the structure of the transformer to connect it to the ground is proposed as a corrective and cost effective solution to mitigate the electromagnetic interferences. New grounding layout enabled to reduce the common-mode current through gate drivers by up to 75% without decreasing the switching rate. This allowed to proceed to measurements on the prototype at nominal operation. The method is validated in simulation and extensive experimental results have been obtained from the considered prototype. This proved the feasibility of the proposed solution and showed the effect of the transformer design in EMI behavior of insulated DC/DC converters.

Introduction

Proper electromagnetic compatibility (EMC) design during development process of any type of electronic device is necessary to ensure the stable operation. The proper EMC design is a challenge when power semiconductors generate high-speed voltage and current transients. In switched mode power converters, the high switching speed of power semiconductors constitutes an important source of electro-magnetic interference (EMI). This means that the interference can disturb other devices in the close common electromagnetic environment. Therefore, electromagnetic compatibility (EMC) of the converter is a must to ensure not only its operation but also the proper function of other electronic equipment in its vicinity [1].

The common-mode (CM) current passes through the ground wire and return path which is caused usually by electrical capacitive coupling $\left(C\frac{dv}{dt}\right)$ [2,3]. Due to the complexity of the converter, the existence of many capacitive parasitic elements is unavoidable in the converter layout. These parasitic capacitances provide a low impedance path for high frequency CM current in the converter. These

parasitic capacitances lead to circulating of the CM current in layout [8-10]. In switching power converters, CM current comes from the fact that switching operation involves charging and discharging of capacitances like semiconductor parasitic capacitances or capacitances in the layout of the converter. When compared to Si devices, wide band-gap semiconductors like GaN and SiC allow to operate at much higher switching frequency which leads to reduce the size of the passive components [4-6]. Alos higher switching speed enables converter designs with potentially higher efficiency. However, higher switching speed leads to fast variations of the voltages all over the layout of the converter which generates high CM current $\left(C\frac{dv}{dt}\right)$ [7]. Therefore, CM current mitigation is often a challenge in SiC or GaN based switching based converters.

Several options have been presented for mitigating EMC issues in DC-DC converters including reducing the EMI from the source and reducing the parasitic elements value [11-15]. There are plenty of researches discussing EMI issues in systems with WBG devices. Some of them deal with the package layout of the semiconductors in order to reduce the EMI [16]. Slowing down the switching speed in order to reduce the voltage variation in the layout of the converter is the most common solution but it increases losses. There are some studies focusing on the circulation of the CM current through the coupling paths [17,18]. The effect of coupling paths in redirecting and reducing the CM current from sensitive part of the circuit has been studied through the use of shielding, filtering, interconnection modification or the combination of all of them [17,18]. The coupling paths which correspond to physical layout must be taken into account seriously when it comes to the installation and the prototyping of the converter. The layout of the converter differs in each application which makes it difficult to have a general solution for different converters. Moreover, changing the parasitic elements of each components of the converter as well as the converter structure after prototype completion is time consuming and costly [19].

The CM current circulation is the major concern in this work. This current circulation was disturbing correct triggering of the semiconductors therefore it is considered as an obstacle for achieving the nominal operation of the converter. There are several studies illustrating the CM current circulation at simulation level and for small scale converters [20]. However experimental study of a high voltage/power converter has a great interest since estimating and simulating all the existing parasitic elements in this kind of converter is not an easy task. Hence this work gives an insight into the physical layout which contributes to CM current circulation in a 3-phases insulated converter. This article proposes a method which improves the operation of the converter. The method consists in adding a filter between the transformer star-point and ground. The benefits and limitations of the proposed method are presented.

This paper is organized as follows. The experimental platform is presented in the following section. Then the self-disturbance phenomenon which limited the operation of the converter is explained. After problem statement section, section introduces a solution to optimize CM current loops in the converter. The experimental results obtained from the proposed solution are depicted in this section. Finally, a conclusion is given. The article is finished by perspectives in the last section for improvements in future converter designs.

Experimental platform

The application under test in this work is a 3-phase Dual Active Bridge (DAB) converter (DAB3). In general, in DAB converters, two voltage-sources converters (VSC) are coupled through a medium-frequency transformer (MFT) (Figure 1). The leakage inductance of the medium frequency transformer is used to control power transfer. In a phase shift controlled DAB, the leakage of the transformer also allows soft switching operation with the help of output capacitance of the switches [21-22]. Besides transferring energy, MFT provides galvanic isolation (see Figure 1).

In the DAB3 prototype considered in this work, all legs inside both 3-phase VSCs are controlled to generate high-frequency square wave voltage (50% duty cycle). The voltages created by VSCs are phase shifted with respect to each other to control the power flow through the MFT. Thus the power can be

transmitted from VSC1 to VSC2 (presented in Figure 1 as +P), or vice versa (shown in Figure 1 as -P). The novel 3-phase MFT prototype is presented in Figure 2. The transformer has been designed for 100kW power converter and 1.2kV [22-24]. The transformer ratio is set to 1:1 and the connection of windings is fixed to Yy (Figure 1). The 100kW SiC MOSFET based converter operates at 20kHz switching frequency.

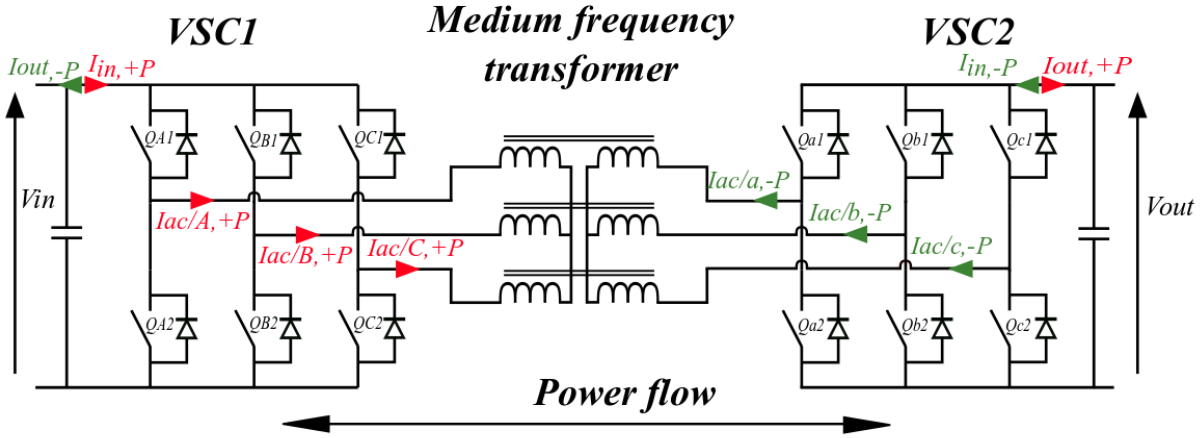

Fig. 1: 3-phase dual active bridge converter schematic

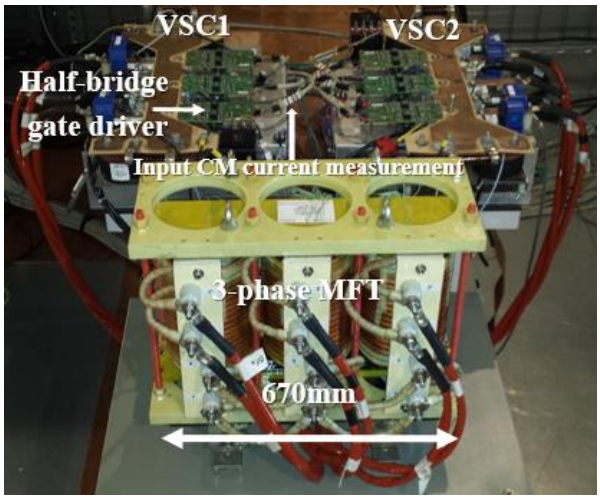

Fig. 2: 3-phase dual active bridge converter prototype [20]

Problem statement

As it has been explained in the introduction, there are many capacitive couplings in the converter layout. The schematic of the studied converter considering major capacitive couplings is shown in Figure 3. In practice, measuring the CM current passing through all the parasitic capacitances in the converter is difficult. In this paper, two groups of parasitic capacitances that contribute to the circulation of the CM current have been targeted. First, the parasitic capacitances in the structure of the transformer which allow the flow of CM current from one VSC to another one and also to the ground ($Cinterwinding$ and Cng in Figure 3). Secondly, there is a capacitive coupling in the isolated power supply of the gate drivers (Cpg in Figure 3) [25].

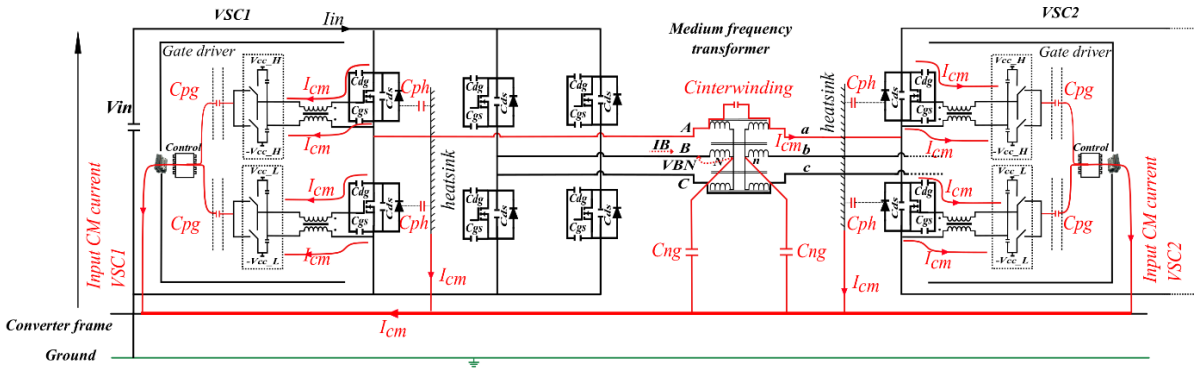

Fig. 3: Some parasitic capacitances and common-mode current paths in the converter.

The gate drivers provide an interface between the control circuit and the power semiconductors. Parasitic capacitances of the semiconductors (C_{dg} and C_{gs} in Figure 3) provide propagation paths to gate drivers for parasitic currents created by $\frac{dv}{dt}$ across the switches. With SiC MOSFETs, the high-speed high-voltage variation across switches induces a CM current which can disturb the gate bias and consequently jeopardize the correct triggering of the switch [26]. A significant amount of the CM current finds the gate drivers as a propagation path. This large CM current can continue flowing to the control circuit through the capacitive coupling in isolation stage of the gate driver. This may lead to disturbances of the control signals. This problem was preventing to reach the nominal operation of the considered converter. The altered control signal which leads to incorrect switching of SiC MOSFET is shown in Figure 4. It can be seen that the high side switch in phase B in secondary VSC at 1200V, 100kW, at the beginning of the period is not turning on which consequently stopped the operation of the converter.

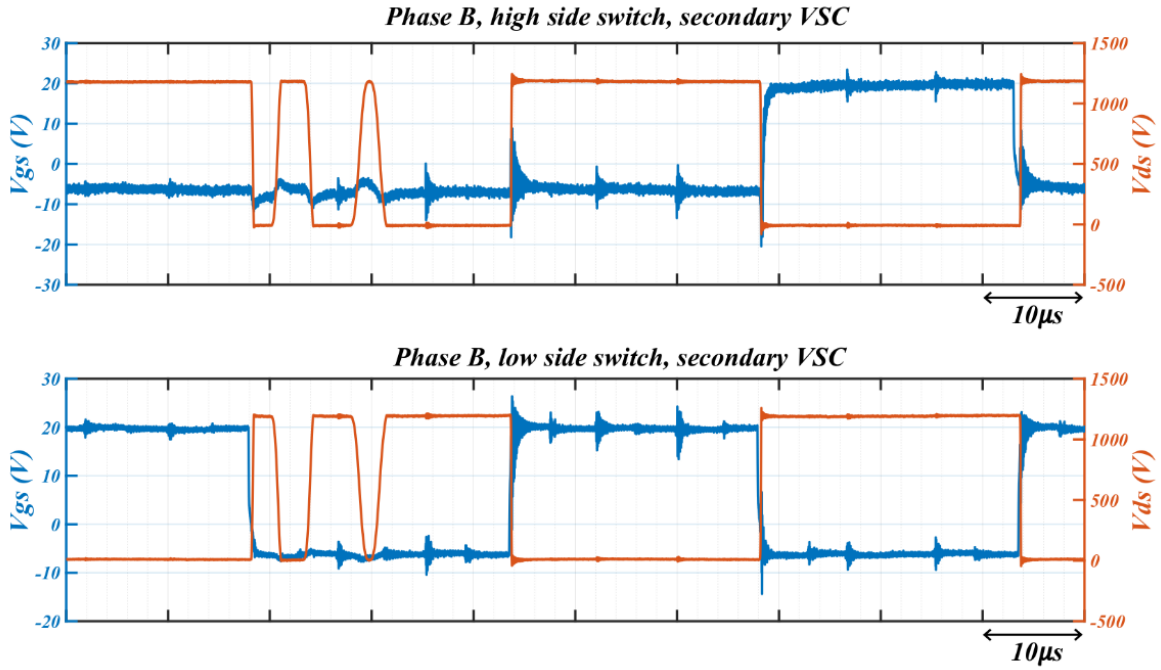

Fig. 4: Experimental result of false triggering of SiC MOSFET in secondary VSC, phase B, 1200V, 100kW.

The phenomenon occurred when the dc bus voltage was higher than 800V and when the transmitted power was reaching 100kW. The CM current of the gate driver (input CM current in Figure 3) of phase B has been measured (Figure 5).

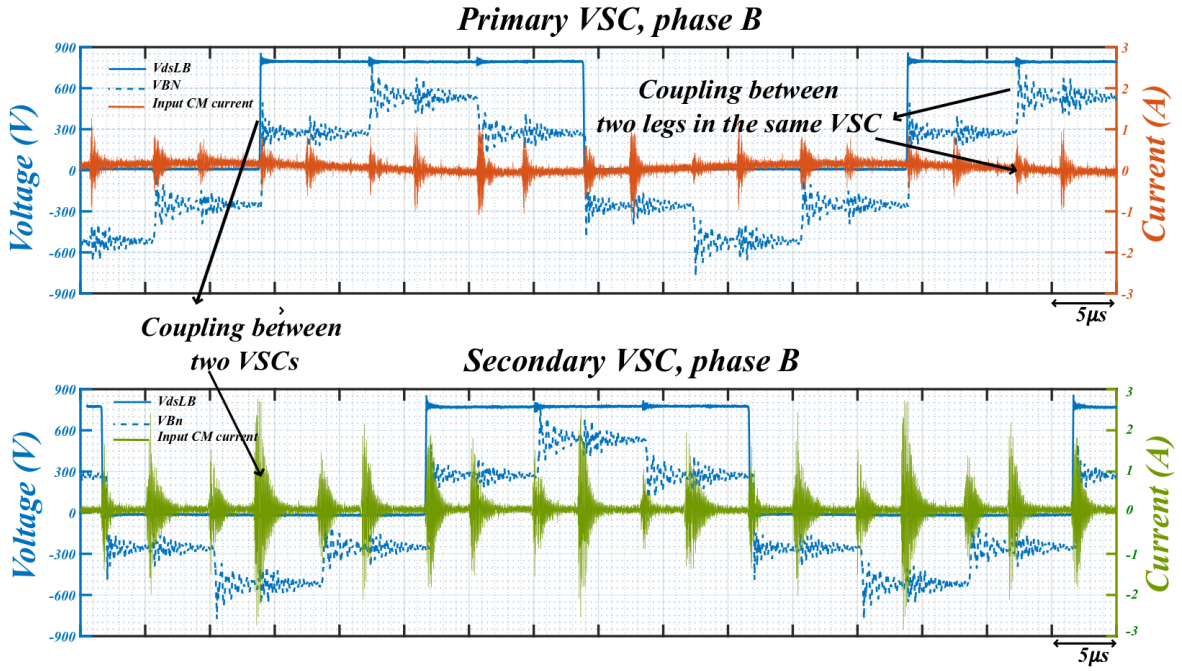

Fig. 5: Experimental results, measured CM current, 800V, 100kW.

The generated CM current pulse is repeated between the turn-on and turn-off transition of the corresponding switch. This shows that the CM current through a gate driver is not only due to the corresponding switch but also to the other switches in the same converter. Moreover, CM current pulses are observed in a gate driver power supply when a leg switches in the other VSC [27]. This shows that a current can pass from a VSC to the other. The presence of MFT parasitic capacitance $(C_{interwinding})$ explains this phenomena.

Based on above mentioned experiments, CM current through gate drivers has been suspected to be the cause of false triggering. The false triggering due to large amount of CM current is called here ‘‘self-disturbance’’ [26-27]. Therefore, in this work, “EMI performance” of the converter is assessed regarding to the magnitude of the input CM current of the gate drivers. In other words, solving the self-disturbance issue is addressed by reducing the magnitude of the CM current through the gate drivers.

Proposed solution and discussion

As it has been explained the parasitic elements in the layout provide paths for CM currents through gate drivers and solving EMI problems after prototyping is a challenge. In an optimized design, the solution has to be anticipated but in a completed prototype, the solution might be to redirect the CM from the victim of EMI to continue the operation of the converter. Adding a new path into the converter in order to divert the CM current from the victim of the EMI could be a better solution since the converter elements remain without changing. The influence of the parasitic elements can be reduced by creating a new circulation path for the CM current. Providing lower impedance path for CM current compared to isolation of the gate driver avoids gate drivers to experience large CM currents.

In order to limit the flow of CM current from the primary VSC to the secondary VSC and to reduce the input CM current of the secondary VSC, it is proposed to modify the electrical ground connection. In this way, the loops of the CM current are minimized. The proposed solution, is to connect the star-points (N in VSC1 and n in VSC2 in figure 3) of the MFT to the ground through a capacitor Cyg (see Figure 6). The main goal is to introduce another path to CM current in order to not pass through the gate drivers.

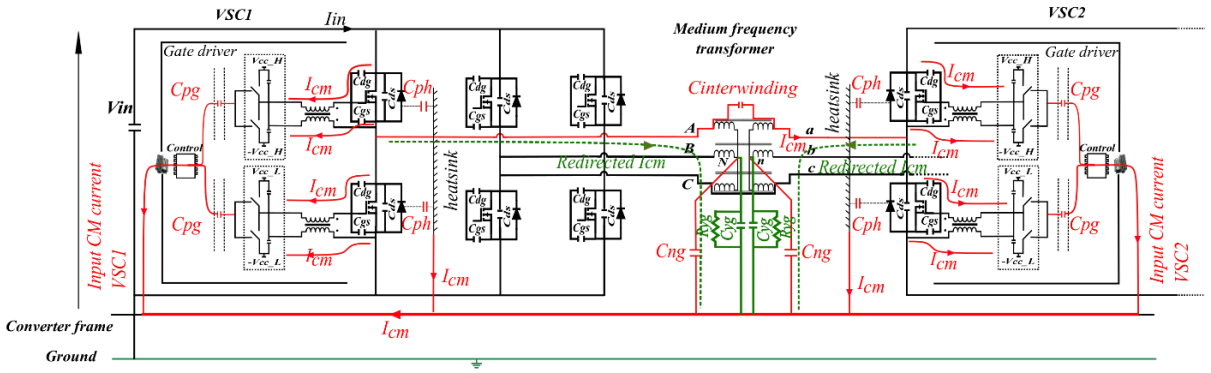

Fig. 6: Proposed solution for ground connection for CM current suppression of gate drivers (Cyg in green).

The MFT model parameters (see Figure 7) have been measured at 20kHz which is the switching frequency of the converter. The measurement has been done for each winding of the MFT with an impedance measurement device (see Table. I).

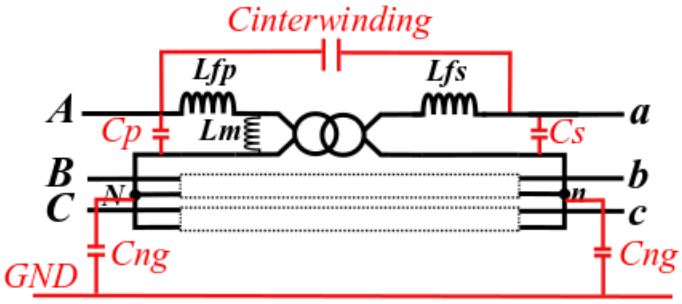

Fig. 7: MFT model [23]

Table I: MFT parameters based on impedance measurement in 20kHz [23]

Parameter	Unit	Value
L_{fp}	µH	17
L_{fs}	µH	17
L_m	mH	1
C_p	pF	30
C_s	pF	30
C_{ps}	pF	80
C_{ng}	pF	30

As it has been depicted in Table 1, the parasitic capacitance between the winding and ground C_{ng} is about 30 pF which is in the same order of magnitude as C_{pg} (20 pF) of the gate driver. The proposed additional star-point capacitor Cyg should have a capacitance high enough compared to the one in the galvanic isolation of the gate drivers. So as, it can provide a path of lower impedance for the CM current. Lower impedance in the ground connection makes the path preferable for the CM current to the ground and redirect the noise that was flowing through the transformer. The star-point connection prevents

propagation of the CM current to the secondary VSC (see Figure 6, dashed line in green). The Cyg value of 100 pF was chosen. The DAB3 has been simulated in Matlab Simulink considering the model of the transformer (see Table. I) and including Cyg. The simulations have been carried out to evaluate the proposed solution in terms of voltage and current across the transformer. The simulation results are presented in Figure 8. The B phase voltage and current correspond to three cases: without Cyg, with Cyg and with Cyg and Ryg. It can be observed a significant voltage oscillation when the Cyg is added. However, adding the resistor Ryg damped the oscillation. The phase current is not influenced by Cyg or Ryg.

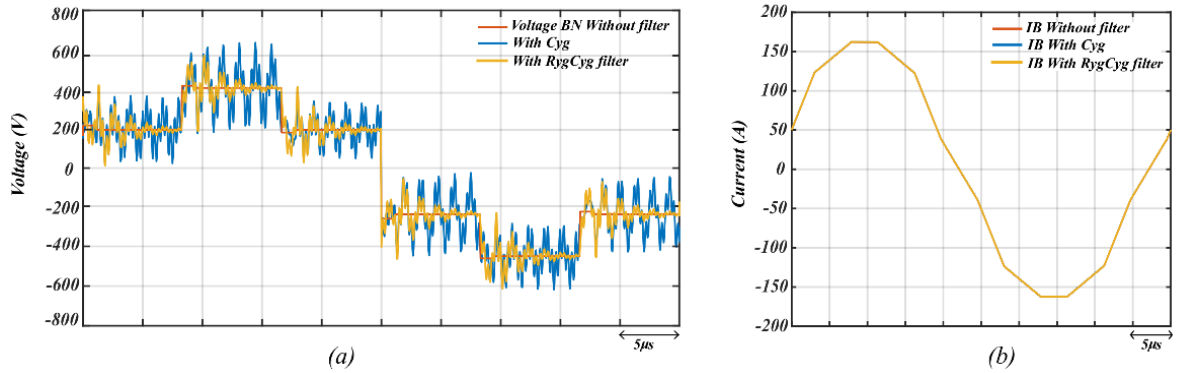

Fig. 8: Simulation results: Waveform with added filter at 1200V, 100kW (a) V_{BN} (b) I_B.

The proposed solution was applied to the prototype in order to verify its effectiveness and to measure the performance of the converter in a continuous test mode. Figures 9 illustrates the effect of the proposed connection in CM current of the gate drivers in VSC2. As it can be seen, the added capacitance shunts the CM current to the ground. Moreover, the magnitude of the transferred CM current from primary VSC to the secondary has been reduced. The peak of the CM current in secondary VSC is significantly reduced (by up to 75%) which allows converter operation above 800V. This confirms that self-disturbance was due to the level of CM current through the gate drivers.

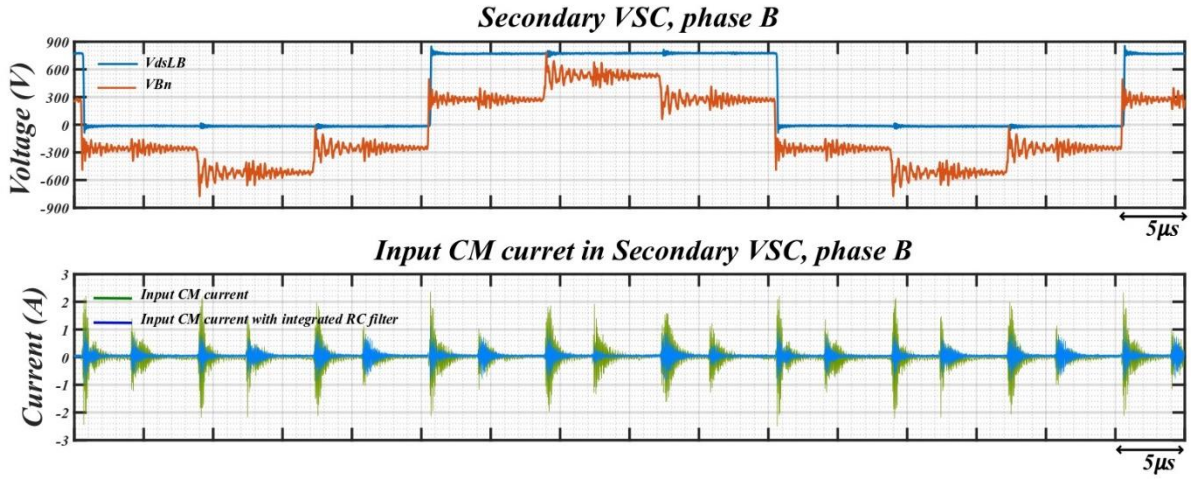

Fig. 9: Experimental results, measured CM current with integrated RC filter, 800V, 100kW.

The current and voltage in phase B have been measured and have been compared with the corresponding waveforms without added filter in order to show that they are not significantly changed due to the proposed solution. Figure 10 illustrates that the added capacitance has not changed the normal behavior of the converter. Moreover, thanks to the proposed solution it is possible to increase the voltage of the converter and reach the nominal operation of the converter (see Figure 11).

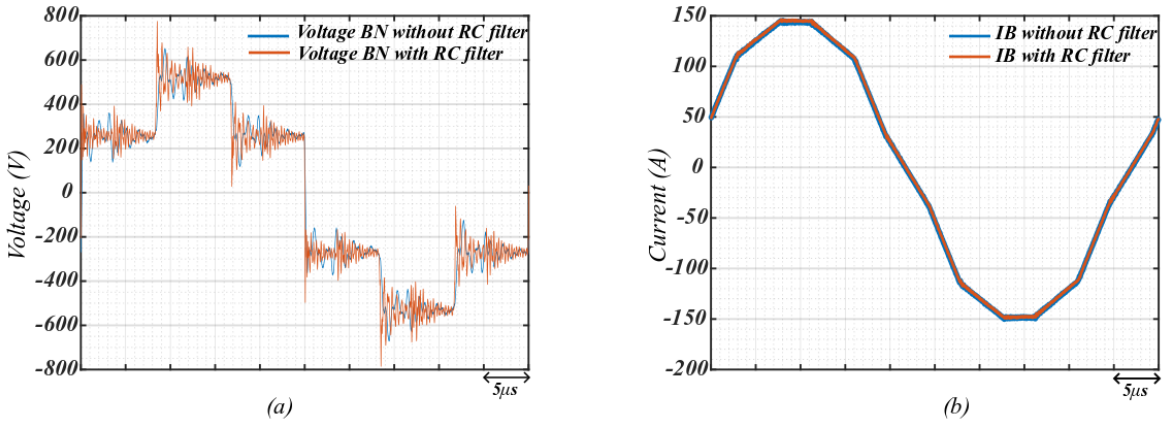

Fig. 10: Experimental results with and without RC filter at 800V, 100kW (a) Voltage in phase B (b) Current in phase B.

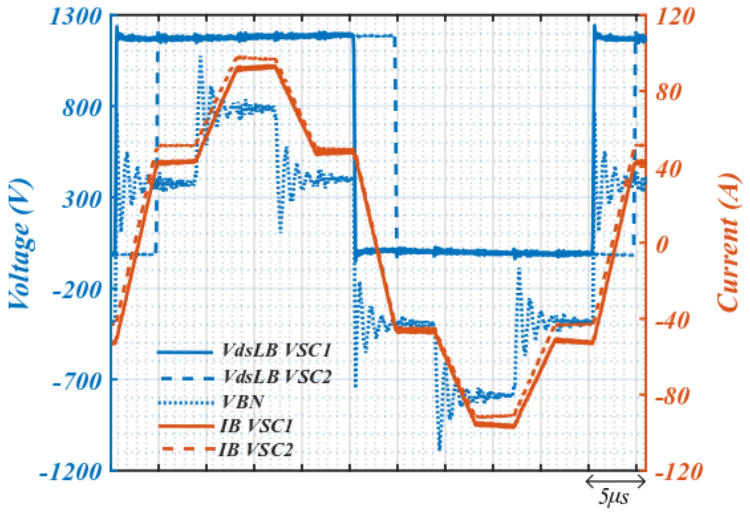

Fig.11: Experimental waveform of DAB3 with RC filter to star point of MFT, 1200V, 100kW.

Conclusion

This work gives an insight into the physical structure and the loops of the CM current in 3-phase dual active bridge prototype (DAB3). The experimental study in this work addressed the EMI problem of a 100kW, 1200V, SiC MOSFET based prototype. The big amount of the input CM current through gate drivers disturbed the control circuit of the converter. Indeed, the isolated supply of the gate drivers provides a propagation path for this current. Therefore, the amplitude of the CM current of the gate driver has been considered here as the indicator of EMI reduction for the prototype. As a corrective solution for a completed prototype, it has been proposed to connect the star-point of the transformer to the ground through a RC filter. This system-level strategy for ground connection of insulated converters allows to divert the CM current circulation from sensitive part of the system and reduce the magnitude of the CM current without decreasing switching speed. EMI behavior of the insulated DAB should be considered in an early stage of converter design, therefore, this work can help converter designer for further prototyping and installation.

The potential limitation of this study is the added resistance to the passive filter. In this specific design, implementing only the capacitance without the damping resistor adds voltage oscillations across the transformer terminals. The damping resistor reduces the voltage oscillations but it adds some power losses. Therefore, for further MFT designs the CM impedances should be considered as design constraints. At present, MFT design procedures rarely include this criteria in the optimization process. Also where the size specification allows to have a screen between primary and secondary windings,

connecting the screen to the ground can minimize the CM current loop and provide a low impedance path for CM current.

References

[1] E. R. Ronan, S. D. Sudhoff, S. F. Glover and D. L. Galloway, "A power electronic-based distribution transformer," IEEE Power Engineering Review, vol. 22, pp. 61-61, 2002.

[2] M. Miloudi, A. Bendaoud, H. Miloudi, S. Nemmich and H. Slimani, "Analysis and reduction of common-mode and differential-mode EMI noise in a Flyback switch-mode power supply (SMPS)," in 2012 20th Telecommunications Forum (TELFOR), pp. 1080-1083, 2012.

[3] M. H. Nagrial and A. Hellany, "Radiated and conducted EMI emissions in switch mode power supplies (SMPS): sources, causes and predictions," in Proceedings. IEEE International Multi Topic Conference, 2001. IEEE INMIC 2001. Technology for the 21st Century., pp.54-61 2001.

[4] G. Aulagnier, M. Cousineau, T. Meynard, E. Rolland and K. Abouda, "High frequency EMC impact of switching to improve DC-DC converter performances," in 2013 15th European Conference on Power Electronics and Applications (EPE), pp. 1-9, 2013.

[5] M. R. Yazdani, H. Farzanehfard and J. Faiz, "Conducted EMI modeling and reduction in a flyback switched mode power supply," in 2011 2nd Power Electronics, Drive Systems and Technologies Conference, pp. 620-624, 2011.

[6] R. T. Naayagi, "Electromagnetic compatibility issues of dual active bridge DC-DC converter," in 2013 International Conference on Energy Efficient Technologies for Sustainability, pp. 699-703, 2013.

[7] J. L. Leslé, R. Caillaud, F. Morel, N. Degrenne, C. Buttay, R. Mrad, C. Vollaire and S. Mollov, "Optimum design of a single-phase Power Pulsating Buffer (PPB) with PCB-integrated inductor technologies," in 2018 IEEE International Conference on Industrial Technology (ICIT), pp. 782-787, 2018.

[8] J. L. Leslé, R. Caillaud, F. Morel, N. Degrenne, C. Buttay, R. Mrad, C. Vollaire and S. Mollov, "Multi-objective optimisation of a bidirectional single-phase grid connected AC/DC converter (PFC) with two different modulation principles," in 2017 IEEE Energy Conversion Congress and Exposition (ECCE), pp. 5298-5305, 2017.

[9] J. L. Lesle, R. Caillaud, F. Morel, N. Degrenne, C. Buttay, R. Mrad, C. Vollaire and S. Mollov, "Optimisation of an Integrated Bidirectional Interleaved Single-Phase Power Factor Corrector," in PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, pp. 1-8, 2018.

[10] E. Rondon, F. Morel, C. Vollaire and J. Schanen, "Impact of SiC components on the EMC behaviour of a power electronics converter," in 2012 IEEE Energy Conversion Congress and Exposition (ECCE), pp. 4411-4417, 2012.

[11] M. R. Yazdani, H. Farzanehfard and J. Faiz, "Classification and comparison of EMI mitigation techniques in switching power converters-A review," Journal of Power Electronics, vol. 11, pp. 767-777, 2011.

[12] D. Hamza and P. K. Jain, "Conducted EMI noise mitigation in DC-DC converters using active filtering method," in 2008 IEEE Power Electronics Specialists Conference, pp. 188-194, 2008.

[13] M. Vilathgamuwa, J. Deng and K. J. Tseng, "EMI suppression with switching frequency modulated DC-DC converters," IEEE Industry Applications Magazine, vol. 5, pp. 27-33, 1999.

[14] Q. Wang, Z. An, Y. Zheng and Y. Yang, "Parameter extraction of conducted electromagnetic interference prediction model and optimisation design for a DC--DC converter system," IET Power Electronics, vol. 6, pp. 1449-1461, 2013.

[15] E. Rondon, F. Morel, C. Vollaire, M. Ferber and J. Schanen, "Conducted EMC prediction for a power converter with SiC components," in 2012 Asia-Pacific Symposium on Electromagnetic Compatibility pp. 1144-1150, 2012.

[16] B. Zhang and S. Wang, "An Overview of Wide Bandgap Power Semiconductor Device Packaging Techniques for EMI Reduction," in 2018 IEEE Symposium on Electromagnetic Compatibility, Signal Integrity and Power Integrity (EMC, SI PI), pp. 297-301, 2018.

[17] D. Fu, P. Kong, S. Wang, F. C. Lee and M. Xu, "Analysis and suppression of conducted EMI emissions for front-end LLC resonant DC/DC converters," in 2008 IEEE Power Electronics Specialists Conference, 2008.

[18] Y. H. Lee and A. Nasiri, "Analysis and modeling of conductive EMI noise of power electronics converters in electric and hybrid electric vehicles," in 2008 Twenty-Third Annual IEEE Applied Power Electronics Conference and Exposition, pp. 1952-1957, 2008.

[19] J. Liu, Y. Wang, D. Jiang and Q. Cao, "Fast prediction for conducted EMI in flyback converters," in 2015 IEEE International Conference on Computational Electromagnetics, pp. 247-249, 2015.

[20] Z. Quan and Y. Li, "Suppression of common mode circulating current for modular paralleled three-phase converters based on interleaved carrier phase-shift PWM," in 2016 IEEE Energy Conversion Congress and Exposition (ECCE), pp. 1-6, 2016.

[21] B.-R. Lin, K. Huang and D. Wang, "Analysis and implementation of full-bridge converter with current doubler rectifier," IEE Proceedings-Electric Power Applications, vol. 152, p. 1193–1202, 2005.

[22] T. Lagier and P. Ladoux, "Theoretical and experimental analysis of the soft switching process for SiC MOSFETs based Dual Active Bridge converters," in 2018 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM), pp. 262-267, 2018.

[23] T. Lagier, L. Chédot, F. W. L. Ghossein, B. Lefebvre, P. Dworakowski, M. Mermet-Guyennet and C. Buttay, "A 100 kW 1.2 kV 20 kHz DC-DC converter prototype based on the Dual Active Bridge topology," in 2018 IEEE International Conference on Industrial Technology (ICIT), pp. 559-564, 2018.

[24] P. Dworakowski, A. Wilk, M. Michna, B. Lefebvre, T. Lagier, "3-phase medium frequency transformer for a 100kW 1.2kV 20kHz Dual Active Bridge converter" 45th Annual Conference of the IEEE Industrial Electronics Society (IES), pp. 4071-4076, IECON 2019.

[25] L. Ghossein, F. Morel, H. Morel and P. Dworakowski, "State of the Art of Gate-Drive Power Supplies for Medium and High Voltage Applications," in PCIM Europe 2016; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, pp. 1-6, 2016.

[26] H. Geramirad, F. Morel, B. Lefebvre, Ch. Vollaire and A. Breard, "Experiemental study of the self-disturbance phenomena in a half-bridge configuration of Si IGBT and SiC MOSFET switches," in PCIM Europe 2020; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, 2020.

[27] H. Geramirad, F. Morel, P. Dworakowski, B. Lefebvre, T. Lagier, P. CAMAIL, C. Vollaire and A. Breard, "Conducted EMI reduction in a 100kW 1.2kV Dual Active Bridge converter," in PCIM Europe 2020; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, 2020.