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Impact of DC fault blocking capability on the sizing of the DC-DC Modular Multilevel Converter

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Keywords

«HVDC», «Modular Multilevel Converter», «DC-DC converter», «Fault blocking».

Abstract

The capability of DC-DC converters of blocking DC faults is an important issue for the development of HVDC meshed grids. This paper analyzes the impact on the converter design of including such characteristic for the DC-DC Modular Multilevel Converter. Steady state and transient analysis are proposed and tested, showing how the converter should be oversized to include this feature. From this analysis it is concluded that including the fault blocking capability has an impact on the power losses and the investment in semiconductors but not in the investment on capacitors. The converter presents better indicators for low DC transformation ratios demonstrating the interest of the topology for these applications. However for those ratios, the impact of including fault blocking capability is the highest.

Introduction

In order to deal with the constant increase of power consumption and the integration of large scale renewable electrical sources, the actual AC system should be upgraded. A hybrid system including AC and HVDC transmission grids appears as a promising solution for the coming upgrade [1]. In order to have a stepwise evolution of HVDC grids, DC-DC converters will be necessary and are considered as a key enabling technology [2], similarly to the AC transformers on the AC system which enabled the incremental evolution of the AC system. The CIGRE studies the subject in the working group B4.76.

DC-DC converters allow the interconnection of HVDC systems that have different characteristics such as voltage levels, technology (VSC-LCC), and line architecture (monopole, bipole) [3], and could provide at the same time various functionalities like power flow control, DC voltage regulation, and fault blocking capability [4]. This characteristic can be understood as the capability of DC-DC converters to prevent the apparition of voltages or currents on one DC grid that could lead to a fault when a fault occurs on the second DC grid. To achieve this, the topology should be capable of breaking the contribution to the fault current from the healthy DC side.

In literature, it has been generally assumed that the required DC-DC converters for HVDC grids should include fault blocking capability [4], given the consequences to the transmission system of a propagation of faults between both DC grids being interconnected with the converter. Some topologies like the Front-to-Front MMC [5], and in general all the circuits that rely in a DC-AC-DC conversion chain [4], include

this feature inherently but the rest of the topologies do not. These last kind of topologies are interesting comparing with those that use a complete DC-AC-DC conversion chain in regard of costs and efficiency [6], [7]. However for those circuits, modifications should be done in order to include the fault blocking capability. For example, adding bipolar sub-modules (SMs), like Full-bridge (FB) SMs, which causes an oversizing in terms of components, increasing power losses and costs. This oversize could decrease the interest on these topologies comparing to the DC-AC-DC approaches.

In this paper, the impact on the circuit design of withstanding DC faults and particularly the converter capability of breaking fault currents is studied for a promising non-isolated topology: the DC-MMC [8], [9]. The recent research on this circuit has increased given its advantages compared to other converters. Some of the works address the topology working principle, its modelling [10], [11], its control [12], the circuit sizing [13], and comparative studies [6]. However on all of these works the fault blocking capability is only mentioned by the inclusion of FB-SMs ignoring the impact on the costs and losses of including such feature. Thus, this paper aims to fill this gap. The analysis is done analytically for steady-state after the fault, as well during transients using simulations.

The Modular Multilevel DC-DC converter (DC-MMC)

The DC-DC Modular Multilevel converter (here denominated DC-MMC, but also known in literature as M2DC[12]) is a non-isolated DC-DC converter formed by the interconnection of several MMC converter legs in parallel, where the AC output ports have been connected together on the low voltage (LV) DC port through an AC filter. The AC filter can be of different types [14] and its principal function is to mitigate the propagation of AC currents into the DC grid and the magnitude of the AC circulating currents. Among the different possible filter technologies for the topology, the simplest solution is a passive filter formed by an inductor per phase as presented in Fig. 1 (a). In the figure, a three phase circuit is represented. However, the DC-MMC can be implemented with any number of phases, but given the power levels considered for the study (700 MW), a three phase DC-MMC is retained.

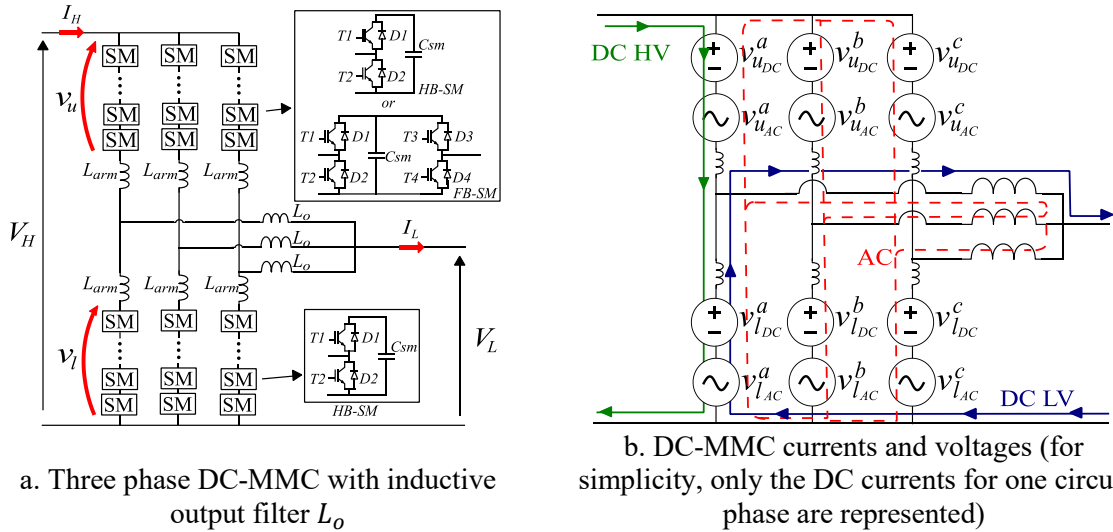


Fig. 1 – DC-MMC topology with three phases.

From the analysis of one phase of the circuit (see Fig. 1), the DC quantities of upper and lower arms are obtained:

$$\begin{aligned} v_{u_{DC}} &= V_H - V_L & i_{u_{DC}} &= \frac{I_H}{3} \\ v_{l_{DC}} &= V_L & i_{l_{DC}} &= \frac{I_H - I_L}{3} \end{aligned} \quad (1)$$

Analyzing the DC power on each arm, assuming no losses on the converter ($P_{DC} = V_H I_H = V_L I_L$), gives:

$$P_{u_{DC}} = \frac{P_{DC}}{3} \left(1 - \frac{1}{n_{DC}}\right) \quad P_{l_{DC}} = -\frac{P_{DC}}{3} \left(1 - \frac{1}{n_{DC}}\right) \quad (2)$$

Where n_{DC} is the transformation ratio V_H/V_L . These equations it is observed that, without any AC power circulating inside the converter, the upper arms absorb energy (positive power) while the lower arms

deliver the same amount (negative power). Thus, to achieve an energy balance on the arms, a circulation of AC power is needed to transfer the excess of energy from the upper arms to the lower arms.

Therefore, the converter working principle is to generate a superposition of DC and AC voltages on each converter arm by the insertion and bypass of the SM capacitors, which makes DC and AC currents to circulate. The DC currents are responsible for the DC power transfer between both DC grids while the AC currents circulate internally to balance the arm energies. Fig. 1 (b) shows the current circulation inside the circuit, highlighting the AC currents and the DC current of each DC side. A more detailed explanation of the working principle of the topology can be found in [12] where an energy based approach [15] for the topology control is proposed.

The required AC power depends of the DC voltage transformation ratio n_{DC} :

$$P_{AC\ circ} = \left(1 - \frac{1}{n_{DC}}\right) \quad (3)$$

Consequently, the topology is particularly interesting for low transformation ratios ($n_{DC} < 2$), since less AC power is required.

In order to achieve the required AC power transfer between arms, they must generate an AC voltage defined by Eq. 5. Note that in this work it is assumed that the AC components are sinusoidal without harmonics.

$$v_{u_{AC}} = |v_{u_{AC}}| \angle \delta \quad v_{l_{AC}} = |v_{l_{AC}}| \angle 0 \quad (4)$$

In order to reduce the converter losses [12], [13], the voltage magnitudes must be equal, i.e. $|v_{u_{AC}}| = |v_{l_{AC}}| = V_{AC}$. The phase angle between both arm AC voltages is determined by the AC power and the circuit inductances, while the voltage magnitude is given by:

$$V_{AC} = \min(V_L, V_H - V_L) \quad (5)$$

Thus, the maximal voltages that each arm must generate for normal operation (no DC faults), and consequently the required number of SMs, are the sum of the DC and AC (peak) components:

$$v_{u_{max}} = V_H - V_L + \min(V_H, V_H - V_L) \quad (7)$$

$$v_{l_{max}} = V_L + \min(V_H, V_H - V_L) \quad (8)$$

Meaning that the total number of SMs required per arm under normal operation is:

$$N_{SMu_{normal}} = v_{u_{max}}/V_{SM} \quad (9)$$

$$N_{SMl_{normal}} = v_{l_{max}}/V_{SM} \quad (10)$$

Where V_{SM} is the nominal voltage of each SM (assuming that all SMs have the same voltage rating).

Steady state analysis of the converter after DC faults

Analyzing the behavior of the circuit when a DC fault occurs on the HV side, once the converter IGBTs are turned off, it is seen that when the DC-MMC is implemented with only HB-SMs, the fault current is propagated between both DC sides due to the direct biasing of the lower diodes on the upper arm HB-SMs, which causes a direct path for the fault current between the healthy side and the fault (Fig 2. (a)).

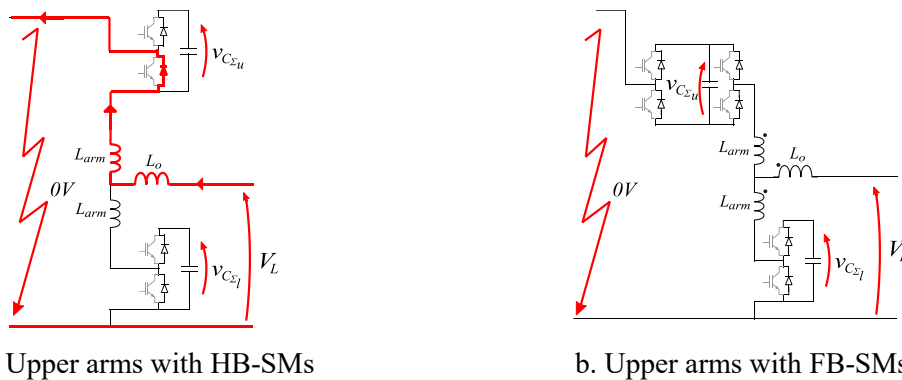


Fig. 2 – DC-MMC after a DC fault on HV side (only one circuit phase and only one SM representing the set of SMs on each arm are represented for simplicity)

When FB-SMs are included (Fig 2. (b)), the upper arms are capable of breaking the healthy side contribution to the fault current if the voltage on the FB-SM capacitors is enough to oppose the voltage difference between the faulty and the healthy sides. Assuming a low fault impedance, the condition on the upper arm FB-SM capacitors voltage is:

$$v_{C_{\Sigma u}} \geq V_L \quad (11)$$

Where $v_{C_{\Sigma u}}$ is the sum of the voltage of all the SM capacitors in the upper arm. When the condition of Eq. (11) is verified, the diodes on the FB-SMs are reverse biased and there is no current flow.

When the fault position is on the LV side (Fig. 3) the fault propagation to the HV side is stopped if the voltage on the upper arm SM capacitors (FB or HB) is enough to oppose the voltage difference between the faulty side and the healthy side given by Eq. 12, assuming low fault impedance. In that case, the diodes on the SMs are reverse biased and there is no current flow.

$$v_{C_{\Sigma u}} \geq V_H \quad (12)$$

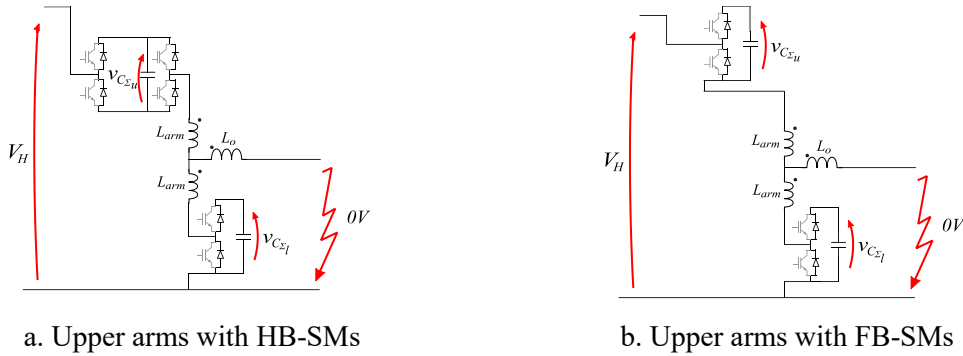


Fig. 3 – DC-MMC after a DC fault on LV side (only one circuit phase and only one SM representing the set of SMs on each arm are represented for simplicity)

If the upper arm SMs are not sized to withstand this voltage, the fault current will continue to circulate between HV and LV DC ports through the upper arm SM capacitors charging them and, thus, generating an overvoltage on the SMs.

From this analysis, it is demonstrated that the capability of the DC-MMC to stop the propagation of DC fault currents depends on certain conditions on the upper arm SMs. Indeed, to stop the propagation of faults when the fault is on the HV side, FB-SMs are needed. The quantity is given by:

$$N_{SM_{FB_u}} \geq V_L/V_{SM} \quad (13)$$

When the fault occurs in the LV side, the upper arm SMs should be sized to support a voltage equal to at least V_H . Therefore, additionally to the FB-SMs, a number of HB-SMs should be added:

$$N_{SM_{HB_u}} \geq V_H/V_{SM} - N_{SM_{FB_u}} \quad (14)$$

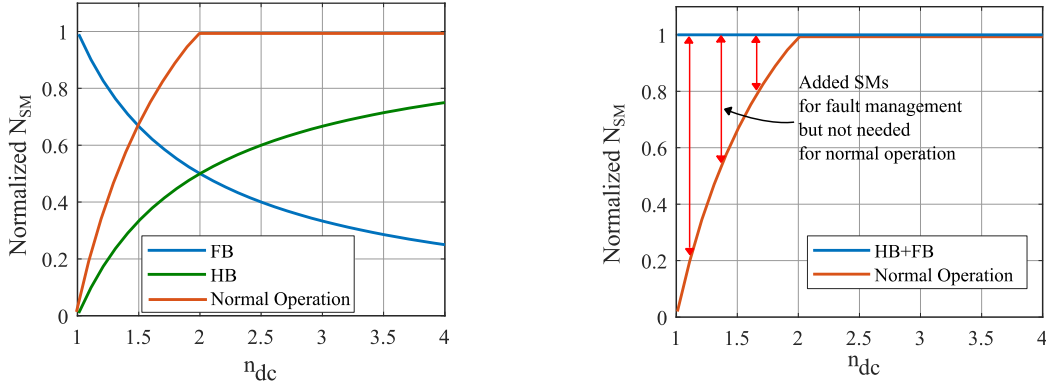
Considering the lower arms, for both DC fault positions (LV or HV side), the required number of SMs is the same that in the normal operation case (Eq. (8) and Eq. (10)).

Impact of including fault blocking capability on sizing and losses

In Fig. 4, the needed number of SMs on the upper arm to withstand DC faults and block the fault current (Eqs. (12) - (13)) are compared with the number of SMs necessary to operate the circuit in normal conditions (only HB-SMs are required according to Eqs. (7) - (10)). It is seen that for $n_{DC} < 2$ the upper arms are highly oversized since HB-SM and FB-SMs are added, while for high transformation ratios ($n_{DC} > 2$), there is no added SMs but there is still an oversizing in terms of components since FB-SMs are required instead of using only HB-SMs.

Concerning the lower arms, as explained in the previous section, there is no particular requirements in terms of number of SMs in order to withstand the voltages in case of faults. Thus, the lower arms are not oversized for the DC fault management.

The difference on the number of SMs required on the upper arms to include fault blocking capability has an impact on terms of cost and efficiency. In order to analyze this impact, the procedure proposed in [6] to compare different converters is used. Three indicators are analyzed: the utilization of semiconductors, the total energy stored in the converter SM capacitors and the power losses.



a. Installed FBs and HBs for fault management and HBs required on normal operation

b. Total installed SMs (FBs and HBs) for fault management and HBs required on normal operation

Fig. 4 – Number of SMs on upper arms

The utilization factor is defined as the ratio between nominal power and the total rating of the semiconductor switches (Eq. (15)). It reflects the investment in semiconductors.

$$U_{SW} = \frac{P_{DC}}{\sum V_{SWpk} I_{SWRMS}} \quad (15)$$

If instead of representing the U_{SW} factor, its reciprocal $1/U_{SW}$ is analyzed, the interpretation could be more straightforward. In this case, the quantity $1/U_{SW}$ can be interpreted as the oversizing in terms of installed power in semiconductors to transmit a given amount of power. In such case the ideal value should be one, i.e. to transmit 1 MW, 1MVA of semiconductors should be installed.

The calculation of U_{SW} , needs the RMS current of each semiconductor device and its peak voltage value. The peak voltage is assumed to be equal to the SM voltage (V_{SM}) and the RMS currents per switch are determined by Eq. (16) [6]. Where T represents the period of the arm current, t_1 and t_2 the times where the arm current changes its sign, and $\alpha(t)$ the average duty cycle of a SM, which depends on the modulation index $m(t)$ given by Eq. (17) and the signs of current. The detailed expressions for $\alpha(t)$ can be found in [6].

$$I_{SWRMS}(t) = \sqrt{\frac{1}{T} \int_{t_1}^{t_2} (i_{arm}(t))^2 \alpha(t) dt} \quad (16)$$

$$m(t) = \frac{v_{arm}(t)}{N_{SM} V_{SM}} = \frac{v_{armDC} + v_{armAC}(t)}{N_{SM} V_{SM}} \quad (17)$$

Concerning the DC-MMC energy requirements, they can be expressed in terms of the energy factor of Eq. (18). This factor reflects the investment in SM capacitors. Lower values of E are preferable.

$$E = \frac{W_{installed}}{P_{DC}} = \frac{\sum \frac{1}{2} C_{SM} \overline{V_{SM}^2}}{P_{DC}} \quad (18)$$

To calculate the SM capacitance required to the estimation of E , Eq. (19) is used [6]. Where V_{DCarm} and I_{DCarm} represent the DC quantities on each arm (Eq. (1)), ϕ is the phase angle between arm current and voltage, N_{SM} is the number of submodules on the arm, f represents the operation frequency, and ε is the allowed capacitor voltage ripple expressed in percentage.

$$C_{SM} = \frac{V_{DCarm} I_{DCarm}}{2\pi f} \left(1 - \left(\frac{\cos \phi}{2} \right)^2 \right)^{\frac{3}{2}} \frac{4}{\cos \phi} \frac{1}{2\varepsilon N_{SM} \overline{V_{SM}^2}} \quad (19)$$

Considering the power losses, only the semiconductor conduction losses are retained for the study. The reason of neglecting the switching losses is that they are heavily influenced by the capacitor voltage balancing mechanisms and the modulation scheme [16], which are out of the scope of the study. The conduction losses on a semiconductor switch (IGBT or diode) are approximated by:

$$P_{cond_{SW}} = V_0 I_{avg} + R_{ON} I_{RMS}^2 \quad (20)$$

Where V_0 represent the saturation voltage if the switch is an IGBT or the forward voltage if it is a diode, and R_{ON} represents the device equivalent resistance in the ON state. Both values can be obtained from the device datasheet (Infineon FZ1500R33HL3 in this study). The RMS current is determined by Eq. (16) while the average current by Eq. (21).

$$I_{sw_{AVG}}(t) = \frac{1}{T} \int_0^T i_{arm}(t) \alpha(t) dt \quad (21)$$

To analyze the impact of including fault blocking capability in the circuit using the presented indicators, the circuit parameters of Table I are used. The output filter inductance L_o has been selected sufficiently large to decrease the circulating currents to an acceptable range and the SM capacitor values have been designed to have a ripple of $\pm 10\%$ at nominal DC power.

Table I: Circuit parameters for analytical study

Circuit Parameter	Value
Nominal DC power (P_{DC})	700 MW
Nominal DC High Voltage (V_H)	640 kV
Nominal DC Low Voltage (V_L)	Determined by n_{DC}
Transformation ratio (n_{DC})	Varied between 1.1 and 4
SM Capacitors (C_{SM})	Designed to have a voltage ripple of 10% for each case
SM nominal voltage (V_{SM})	1.6 kV
Arm inductance (L_{arm})	15 mH
Filter inductance (L_o)	150 mH
AC Frequency	150 Hz

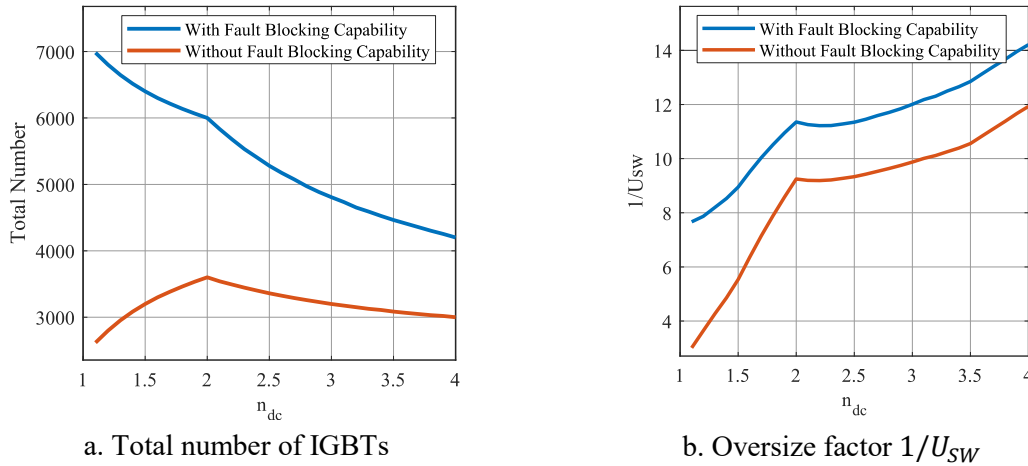


Fig. 5 – Impact on semiconductor investment

Fig. 5 (a) shows the total number of IGBTs on the 3-phase DC-MMC. It is observed that for all the considered transformation ratios (n_{DC}) more IGBTs are needed to include fault blocking capability, mainly for low values of n_{DC} , which is coherent according to the number of SMs (see Fig. 4 (b)).

In Fig 5 (b), the oversize factor $1/U_{SW}$ is presented. It is observed that for low values of n_{DC} , the additional installed power needed to include fault blocking capability is significant. For example, for $n_{DC}=1.1$, 7.6 times of the nominal power is needed instead of 3 times if this feature is not implemented. As n_{DC} increases, the gap is decreased and is almost constant for $n_{DC} > 2$.

Considering the investment in capacitors, Fig. 6 presents the value of C_{SM} on the upper and lower arms in function of n_{DC} . It is observed that, as discussed in the previous section, the lower arms are not affected by including fault blocking capability, then, the same values of C_{SM} are obtained if the feature is included or not. For the upper arms, C_{SM} is influenced by the total number of SMs, which in the case

of $n_{DC} < 2$ is different if the fault blocking capability is included or not (see Fig. 4 (b)). However, observing the energy factor, it is seen that for all the cases the energy requirements are the same. This comes from the fact that even if at $n_{DC} < 2$ less SMs are required when no fault blocking capability is implemented, the value of the individual SM capacitance is higher. Therefore the investment costs in capacitors are expected to be similar if the feature is included or not.

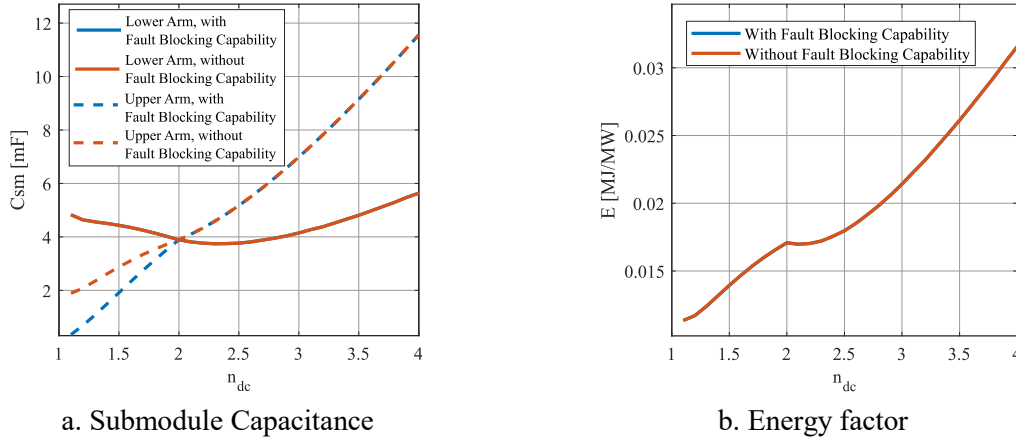


Fig. 6 – Impact on investment in SM capacitors

The conduction losses at nominal power are presented in Fig. 7, as well as the ratio between the case of including fault blocking capability and the case of not including it. It is seen that in all the cases the losses are increased by including this feature, for $n_{DC} < 2$ the losses are considerably increased. For very low values of n_{DC} ($n_{DC} < 1.25$) the losses are even doubled. For $n_{DC} > 2$, the increase in the losses is kept at around 20% independently of the value of n_{DC} .

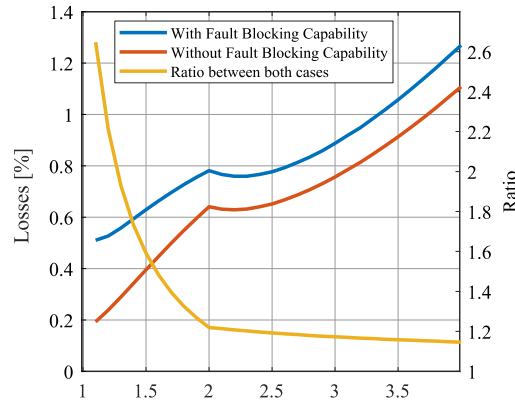


Fig. 7 – Impact on semiconductor conduction losses

From this analysis it is concluded that including the fault blocking capability on the DC-MMC has an impact on the power losses and the investment in semiconductors but not in the investment on capacitors. The DC-MMC presents better indicators for low values of n_{DC} demonstrating the interest of the topology for these applications. However for those values of n_{DC} , the impact of including the fault blocking capability is the highest.

Impact of the transient response on the fault current breaking

In the previous section, the impact of including fault blocking capability on the converter sizing, costs and power losses was analyzed considering the minimal number of SMs required for the DC fault management. In this section the transient response during fault is studied to evaluate if it impacts also the converter sizing. Simulations of the circuit for HV and LV side DC faults are done to analyze this impact. The simulations are done using an average arm model including the model during the blocked state [17]–[19] as shown in Fig. 8. The converter parameters are presented in Table II.

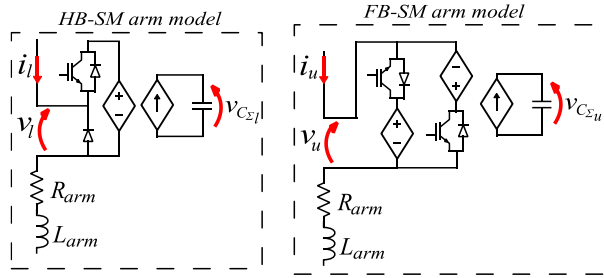


Fig. 8 – Arm average model including blocked state modelling

The simulations are done for HV and LV side faults, considering different power flow directions before the fault (from HV to LV side or from LV to HV side). Once the fault is detected, all the IGBTs in the converter are turned off. These actions are done considering a delay of 50 μ s after the fault detection.

Table II: Circuit parameters for DC fault simulations

Circuit Parameter	Lower Arm	Upper Arm
Nominal DC power (P_{DC})	700 MW	
Nominal DC Voltages (V_H / V_L)	640 kV / 500 kV	
SM Capacitor (C_{SM})	1.2 mF	5.3 mF
SMs per arm (N_{SM})	400 HBs	400 FBs
SM nominal voltage (V_{SM})	1.6 kV	1.6 kV
Equivalent Arm Capacitor ($C_{eq} = C_{SM}/N_{SM}$)	3.1 μ F	13.3 μ F
Arm inductance (L_{arm})	15 mH	15 mH
Arm resistance (R_{arm})	0.5 Ω	0.5 Ω
AC voltage (RMS line-to-line voltage)	137 kV	137 kV
Filter inductance (L_o)	150 mH	
Filter series resistance (R_o)	0.08 Ω	
AC Frequency	150 Hz	

The results for the case of HV side DC fault, are presented in Fig. 10 considering a power flow from LV to HV side before the fault, the dotted line shows the moment of the converter blocking. This power flow is considered the worst case since the fault current has the same direction than the nominal power. Thus, after the fault, the current increases without passing by zero (see I_H curve on Fig. 10). Once the converter is blocked, the current starts to decrease until all inductances in the system are totally discharged. Then, the fault current is stopped, the DC currents I_L and I_H remain at zero after the transient. However, during the process, the FB-SMs on the upper arm absorb the energy stored on the circuit inductances and also the energy coming from the LV grid. As a consequence the capacitor voltage could be highly increased (20% for phase c in Fig. 10, for this example). Thus, the converter should include more SMs to withstand the overvoltage or the capacitors should be oversized accordingly to absorb the excess of energy without a significant overvoltage. The amount depends on the system inductances (including grid inductances), and control delays.

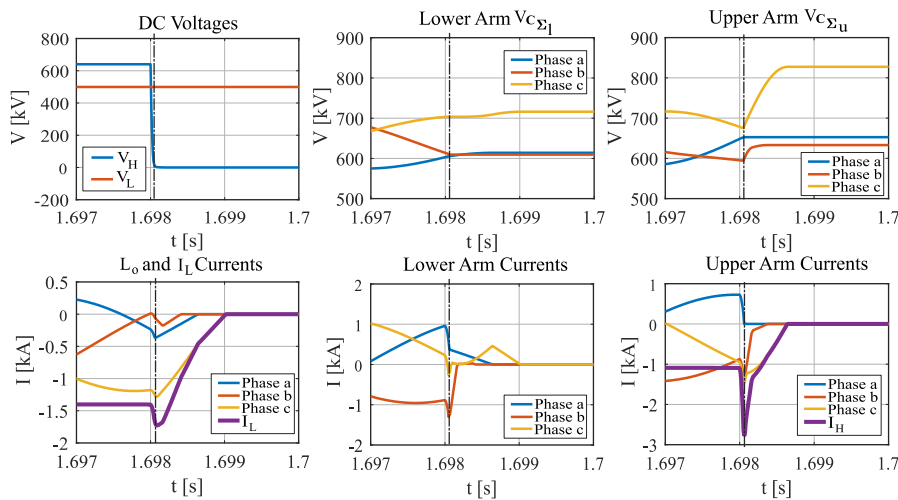


Fig. 10 – Simulation results for HV DC fault case

Fig. 11 shows the results obtained for a fault on the LV side. In this case the considered power flow before the fault is from HV side to LV side. It is observed that similarly to the previous case, the fault current is stopped but the FB-SMs on the upper arm are overcharged during the process (mainly phase *b* on this example). It is observed as well that fault current takes several more time to be extinguished (observe I_L curve on the figure), which in the simulation results was of 83 ms (not shown in the figure). The reason of this long discharge time is the high value of the output inductance filter L_o . In consequence, for a fault on the LV side the upper SMs must be sized to absorb the excess of energy preventing an overvoltage, and the lower SMs freewheeling diodes must be capable of withstanding the fault current during quite long time according to the value of L_o .

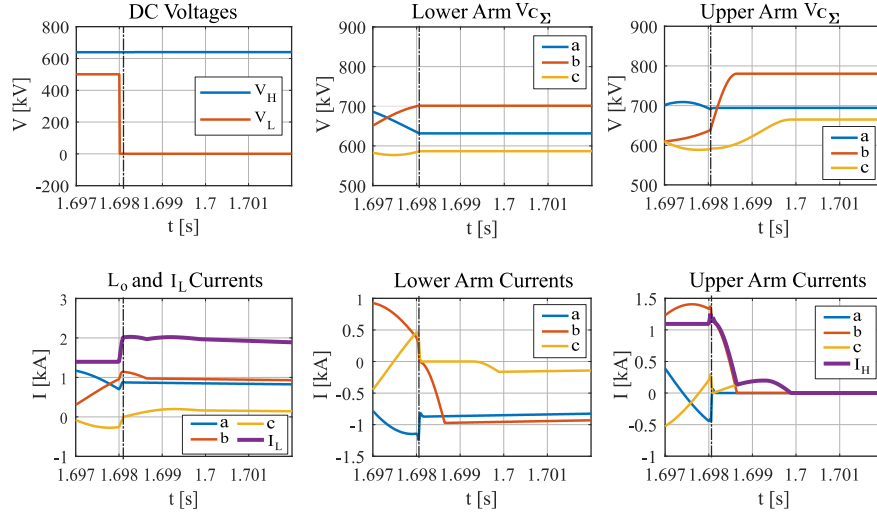


Fig. 11 – Simulation results for LV DC fault

Conclusion

The impact on the DC-MMC of DC fault management has been analyzed. It has been shown that including the fault blocking capability requires FB-SMs and/or (according to the voltage ratio) additional SMs in upper arms. This increases the converter cost and losses, mainly associated to the investment and losses in semiconductors. However the investment costs in capacitors are expected to be similar if the feature is included or not. The impact is worst for low voltage transformation ratios, for which the topology is normally more interesting. The transient response analysis showed that, in order to extinguish the contribution to the fault current, the FB-SMs on the circuit should be able to absorb the energy stored in inductances during faults which can lead to an overvoltage or an oversizing on the SM capacitance. Further works should be done to compare the DC-MMC without fault-blocking capability associated with an external DC circuit breaker, particularly for low voltage transformation ratios. In such cases the additional breaker could have an interest since the costs of including the fault blocking capability on the circuit are considerable. The paper outcomes should also be evaluated with more accurate grids models. Finally, the developed methodology can be generalized to larger set of DC-DC converters for HVDC applications.

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