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A 110mK 295 μ W 28nm FD-SOI CMOS Quantum Integrated Circuit with a 2.8GHz Excitation and nA Current Sensing of an On-chip Double Quantum Dot

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To reach quantum supremacy, quantum computers need >50 logical qubits with <mV accurate biasing, GHz-range signal handling, and μ s readout of thousands of physical qubits at sub-Kelvin temperatures. Silicon-based qubits are a promising approach to scale the qubit number owing to their low footprint (100 nm) and gaining from the CMOS industrial background to reach maturity [1]. Moreover, the quantum silicon choice allows the IC community to integrate large-scale qubit-control electronics directly nearby the quantum silicon core, thus drastically reducing the wire-connection number and qubit-addressing fanout, meanwhile increasing the operation bandwidth for error correction and the spin-readout sensitivity.

Recent publications have already explored electrical performance with, e.g., MHz to GHz signal generation [2,3,4] and analog amplification [4,5] in sub- μ m CMOS technologies around 4.2K. Although cryogenic ICs above 1K have been co-integrated with quantum devices [2,5], systems-on-chip including quantum devices and electronic circuits with operation below 1K remain unexplored and are a key element towards the development of silicon-based quantum processors.

This paper presents a *Quantum Integrated Circuit* (QIC) on a single chip in industrial CMOS technology (28nm FDSOI) integrating a double quantum dot (QDUT) with mixed digital-analog circuits including biasing, signal generation and manipulation, and read-out. The presented QIC is aimed to measure a quantum-effect named charge pumping by i) biasing the two quantum dots from on-chip bias tees, ii) applying GHz-range mV-level modulation from on-chip frequency- and amplitude-controlled clock generators, and iii) measuring the induced current through the QDUT from a multiplexed on-chip transimpedance amplifier (TIA). This work demonstrates the viability of heterogeneous functions (analog, digital, and quantum) down to 110mK on a single industrial chip while sustaining quantum effects.

Figure 19.2.1 depicts the circuit architecture including digital and analog functions with the on-chip QDUT. Voltage-controlled ring oscillators (OSC) at two frequency ranges generate a clock signal sent through a digital multiplexer (DMUX) and a level shifter (LS) followed by a digitally-controlled capacitive divider (CDIV) to control the amplitude of the AC component of the gate voltage of Dot2 (VG2). The OSC frequency is measured at room temperature after division by 1024 with dynamic flip-flops (DFF) and a digital output buffer (BUF). The DC point of QDUT (VG1, VG2) is set by two bias tees. The continuous double-dot current i_{dot} induced by the oscillating VG2 is converted to a voltage by the TIA. An analog multiplexer (ANAMUX) routes multiple QDUT readouts to reduce the number of wires connected to room-temperature. The overall QIC power consumption is 295 μ W when all functions are enabled, leading to a temperature of 110mK in a He3/He4 dilution-type cryostat.

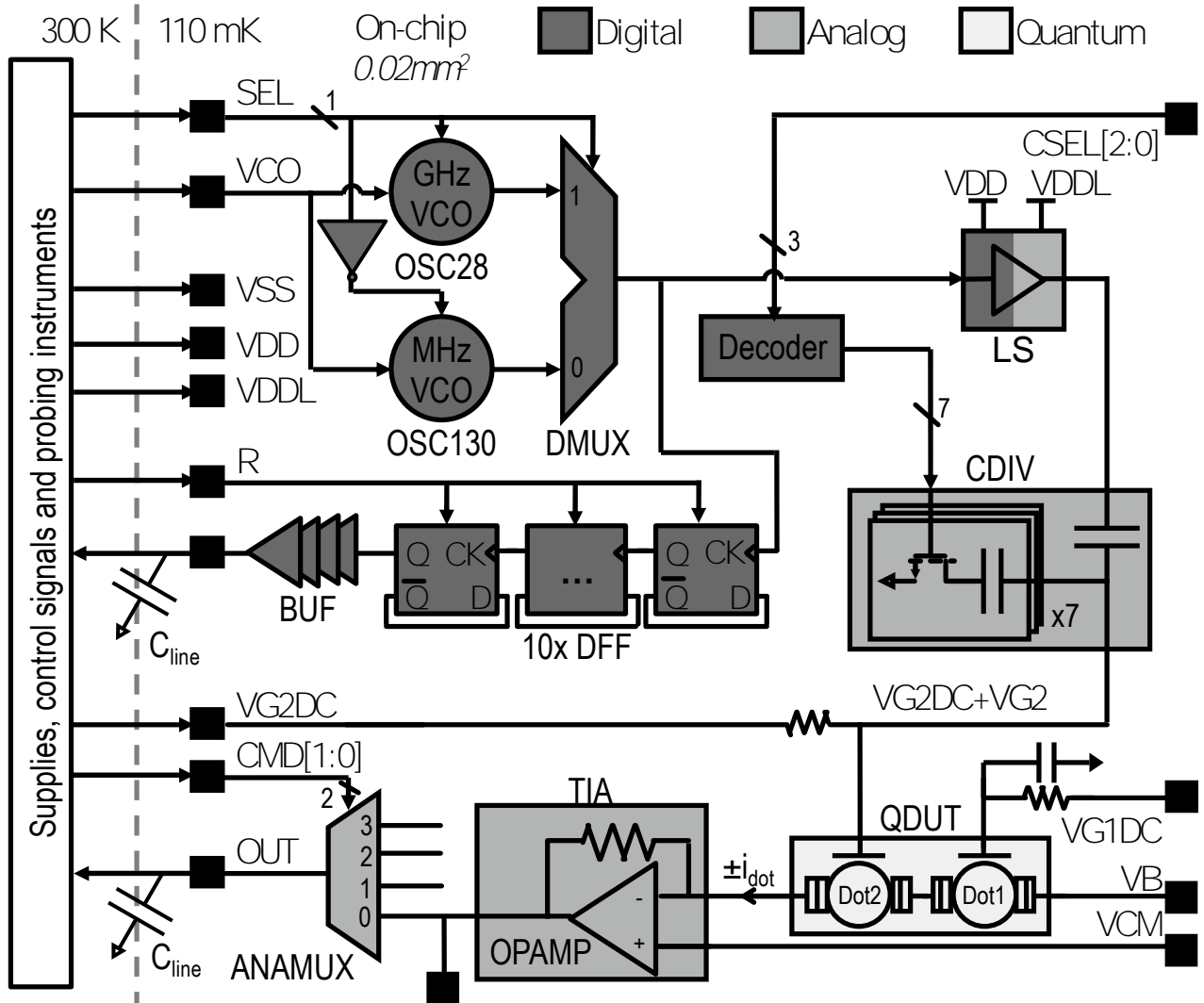


Figure 1: Functional block diagram of the mixed digital-analog signal circuitry interfacing a quantum device at 110mK.

Figure 19.2.2 illustrates the main analog, digital, and quantum circuits at transistor-level. As no cryogenic design-kits are available at 110mK, the FDSOI technology has been selected using the already published transistor-level characterizations at low-temperatures and the back-biasing feature which creates more design flexibility. To enable optimization of the operation point, separate back-biasing can be applied for the two oscillators (OSC28, OSC130), for the other digital parts (LS, DFF, BUF, DMUX), for the analog parts (OPAMP, CDIV), and for the QDUT. A minimal gate length of 28nm and 300-600nm gate widths are chosen for the digital transistors to avoid non-ideal cryogenic transistor characteristics while maintaining a high bandwidth and low-power consumption. OSC28 (28nm gate length) and OSC130 (130nm) achieve, respectively, a GHz and MHz frequency-range via the modulation of current-limited inverting stages. Dynamic flip-flops (DFF) reduce power consumption and operate up to GHz frequencies under a 1V power supply level. To generate a mV-level VG2 signal from the OSC output, LS shifts the 1V pulse train to a lower voltage $VDDL > V_{TH}$ for fine continuous adjustment while coarse step-wise tuning is achieved with CDIV composed of a metal-oxide-metal capacitor bank. At the operating temperature (110mK), the tunneling of electrons through the illustrated potential barriers dominates the current through the QDUT that is continuously sensed by the TIA in the nA-range. The OPAMP is a 333nA-biased two-stage output rail-to-rail amplifier with long transistors for enhanced analog performance in, e.g., gain, noise, and matching. A highly disordered polysilicon $M\Omega$ resistor is used in the OPAMP feedback to achieve a measured 11.3mV/nA transimpedance gain because of its high resistance surface-density and its low variation down to sub-Kelvin temperatures. OPAMP and TIA feedbacks are designed to ensure the signal stability even with large cable impedance towards room-temperature equipment.

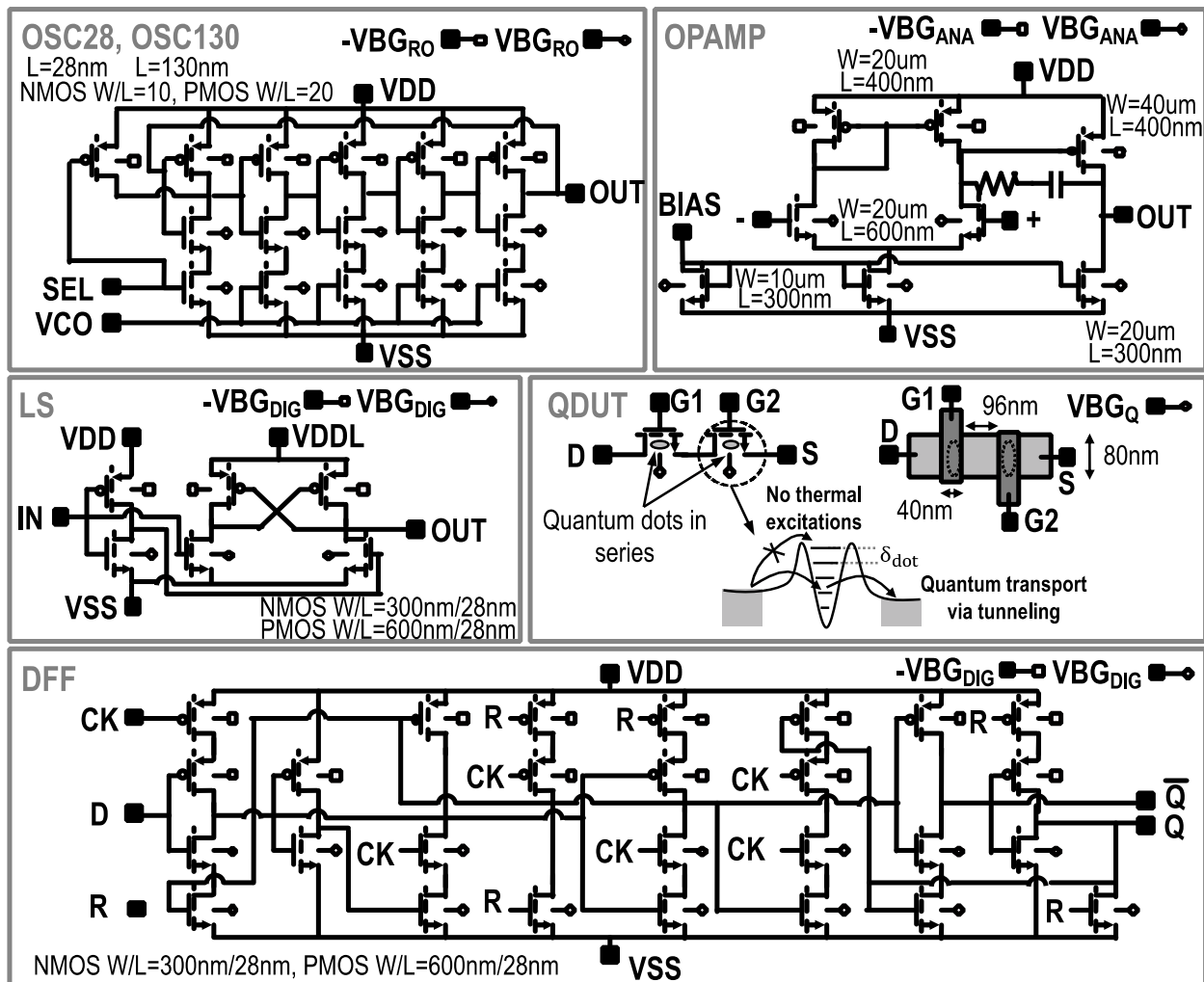


Figure 2: Schematic diagrams of the key digital and analog sub-circuits with independent back biasing nodes made with 28nm FDSOI technology.

Figure 19.2.3 highlights the advantage of back-biasing by compensating the increased V_{TH} ($\sim 650\text{mV}@110\text{mK}$) at cryogenic temperatures. A 2V back-gate (VBG), reducing $|V_{TH}|$ by $\sim 200\text{mV}$, increases the maximum frequency of OSC28 by 2.3x while only increasing the power consumption by 1.5 thus lowering the energy consumption per cycle (14 fJ/c). The back-biasing permits to increase the frequency of the 10xDFF+BUF circuit by 55%, allowing to extract the highest frequency generated by OSC28. Likewise, the LS bandwidth is boosted to 2.8GHz by more than 5.6x by applying 2V VBG. Figure 19.2.4 depicts the performance of the analog circuits (CDIV, ANAMUX, and TIA) at 110mK. The TIA has been designed to dissipate only $1\mu\text{W}$ to avoid local heating of the μm -distant QDUT and to measure nA-range QDUT DC-currents with a 1.1kHz bandwidth and a flicker-limited noise, also given in Fig. 19.2.4. To leave the bandwidth unchanged, ANAMUX pass gates maintain a $183\Omega \pm 14\%$ on-resistance with a 2V VBG, ~ 10 times less than the few k Ω TIA output impedance.

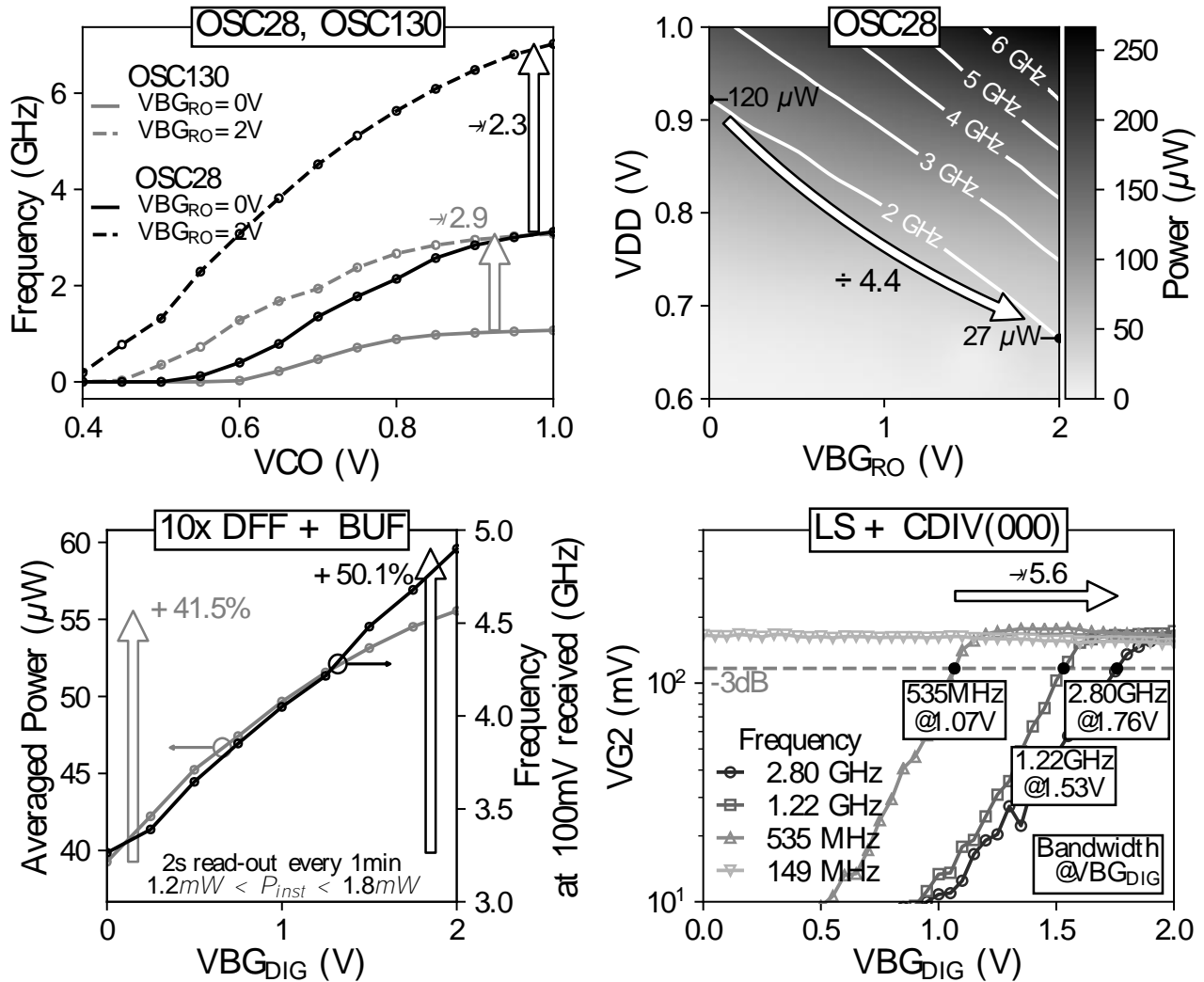


Figure 3: Power efficiency and speed improvement with back-biasing for the digital parts at 110mK.

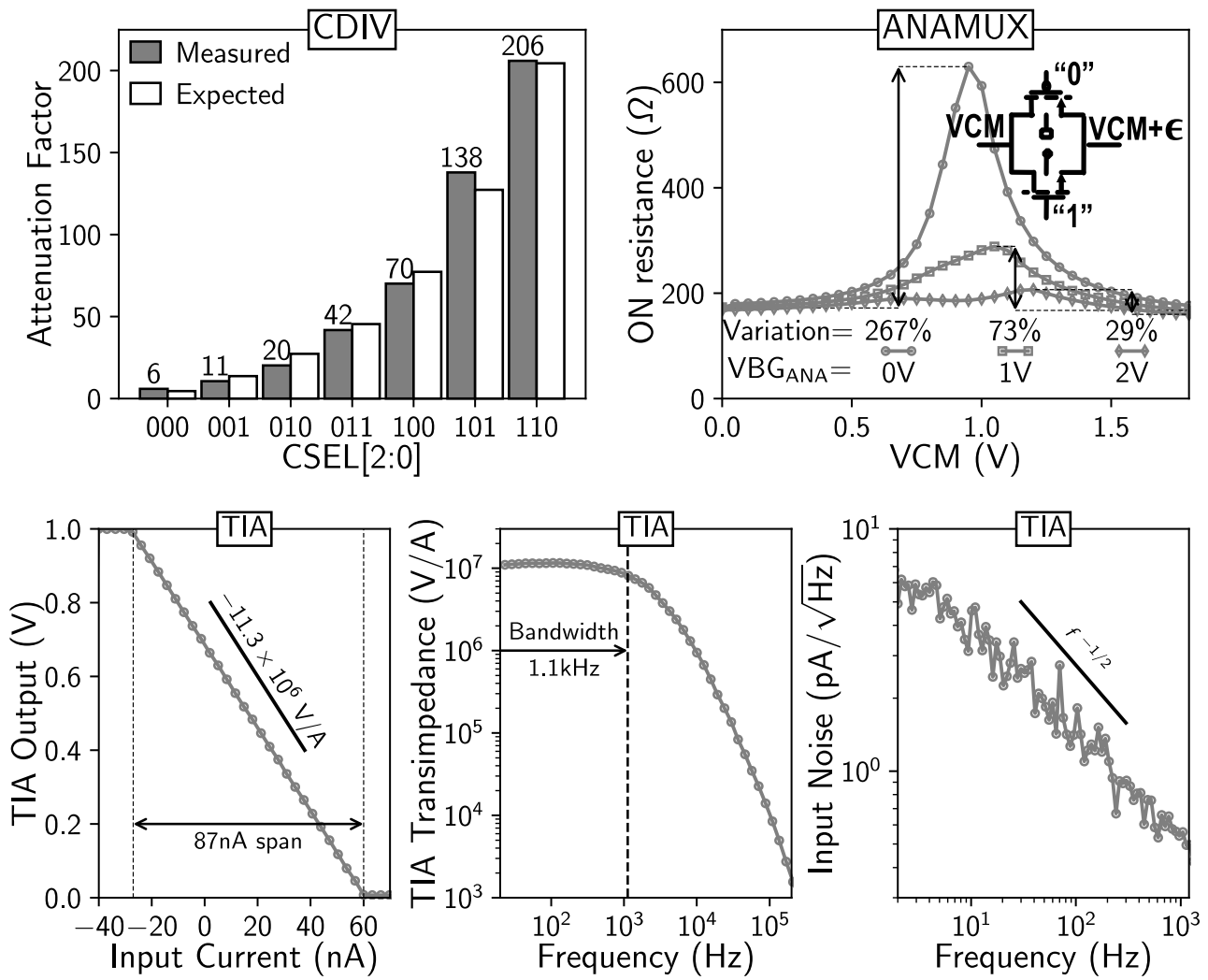


Figure 4: Analog performance at 110mK of CDIV and ANAMUX for signal manipulation and TIA current read-out.

During the QDUT measurements (Fig. 19.2.5), the temperature has been maintained at 110mK with the $300\mu\text{W}$ cooling power of the cryostat matching the maximum power consumption when a 2.8GHz 167mV VG2 signal is generated. The TIA is continuously sensing the current through the QDUT while performing minutes-long 2D sweeps of (VG1DC, VG2DC) at constant VG2 frequency. DFFs and BUF are activated during 2s to avoid heating due to $\sim 10\text{MHz}$ output driving to room-temperature region. At a low bias VB of QDUT, the quantized energy levels in both quantum dots give a 2D pattern of non-zero-current triangles in the (VG1DC, VG2DC) plane with $<10\text{mV}$ asymmetry. New structures appear when applying an oscillating VG2 related to dynamic phenomena such as charge pumping.

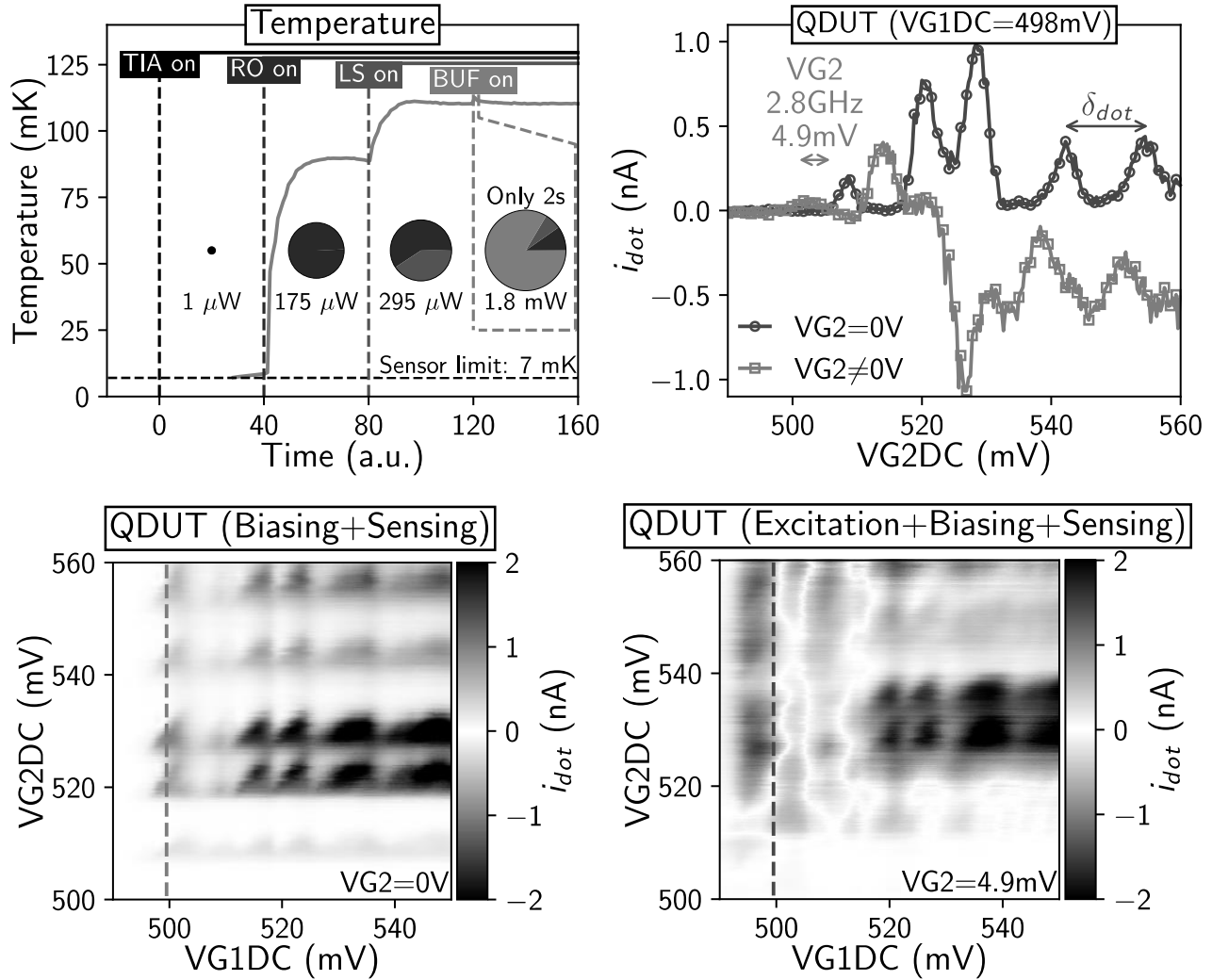


Figure 5: In situ control and read-out of a double quantum dot device using all-integrated circuit elements without and with 2.8GHz excitation.

Figure 19.2.6 gives a comparison to previously reported cryogenic electronics to study *in-situ* quantum device effects. The presented QIC integrates RF digital and analog circuits to bias, manipulate, and read-out a quantum device on the same chip made with industrial CMOS technology operating at 110mK. OSC28 achieves an 8.1x better efficiency for an 18x higher frequency than [3]. TIA occupies a 110x smaller chip area than [5] for only 1 μ W allowing massive parallel sensing within the limited cryostat power budget. This paper has presented to the best of the authors' knowledge, the very first integration of quantum-dots together with digital and analog circuitry. The obtained benchmark of 2.8GHz signal generation and manipulation, highly-sensitive current-to-voltage conversion, and the absence of parasitic cross-coupling to the quantum device for a 295 μ W power dissipation of the complete circuit gives a very promising outlook to integrate *in-situ* electronic control systems for qubits. Cryogenic high-speed ICs will help to reach the quantum error correction threshold with better qubit control and read-out towards the first realization of a large-scale silicon-based quantum processor.

System		[4]	[2]	This work
Temperature		4.2K	3K	0.11K
Application		Future Qubits Experiments	XMON Rabi Experiments	Double Quantum Dot Dynamics
On-chip	Analog	Yes	Yes	Yes
	Digital	No	Yes	Yes
	Quantum	No	External	Yes

Sub-Circuit Specifications	[4]	[3]	This work	[5]	This work	Unit
	Oscillators			TIA		-
Technology	Bulk 40nm	FDSOI 28nm	FDSOI 28nm	Bulk 0.35 μ m	FDSOI 28nm	-
Type	LC	RO	RO	OPAMP	OPAMP	-
Power	7,000	119	268	5,000	1	μ W
Frequency	6.7	0.38	6.9	-	-	GHz
Bandwidth	-	-	-	250	1.1	kHz
Input Noise	-	-	-	30	300	fA/ \sqrt Hz
Temperature	4.2	4.3	0.11	4.2	0.11	K
Footprint	130,000	N/A	10.6	1,100,000	10,000	μ m ²
FoM	1,045*	313*	38.8*	0.5†	1.1†	-

$$* \text{FoM}_{\text{OSC}} = \frac{P_{\text{DD}}}{f} \quad \dagger \text{FoM}_{\text{TIA}} = \frac{\text{BW}}{\text{Noise}} \times \frac{300\mu\text{W}}{P_{\text{DD}}}$$

Figure 6: Comparison with state-of-the-art cryogenic circuitry.

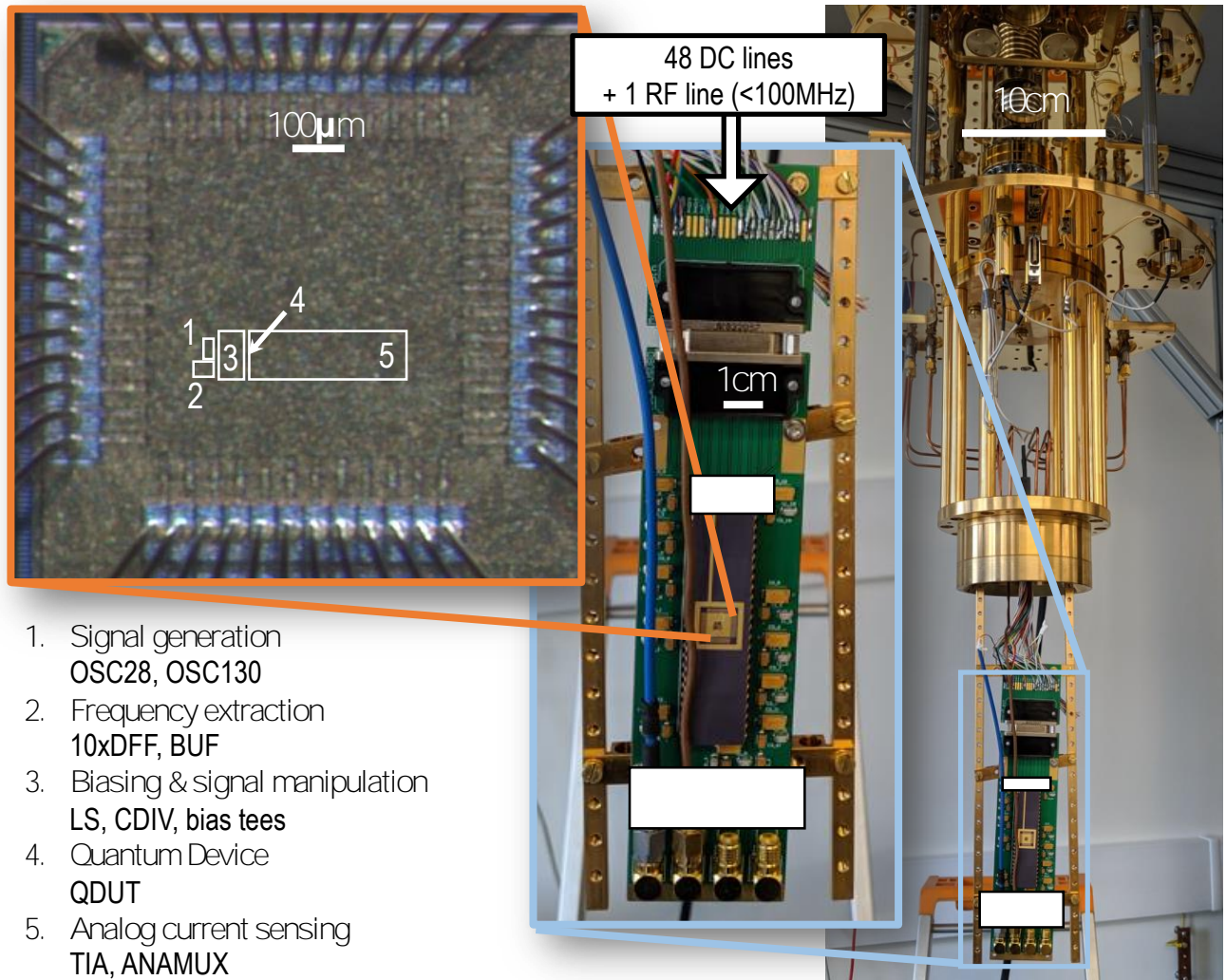


Figure 7: Die micrograph, packaged chip mounting on a PCB with decoupling capacitors, and dilution-fridge mounting.

Acknowledgements:

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