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Gate-damage accumulation and off-line recovery in SiC power MOSFETs with soft short-circuit failure mode

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Abstract –This paper proposes the detailed analysis of the short-circuit failure mechanism of a particular class of silicon carbide (SiC) power MOSFETs, exhibiting a safe fail-to-open-circuit type signature. The results are based on extensive experimental testing, including both functional and structural characterisation of the transistors, specifically devised to bring along gradual degradation and progressive damage accumulation. It is shown that the soft failure feature is associated with degradation and eventual partial shorting of the gate-source structure. Moreover, partial recovery, induced here by ad-hoc off-line biasing, is observed on degraded components. The results indicate that it is a realistic new option for deployment in the application to yield enhanced system level robustness and system-level hopping-home operational mode capability, of great importance in a number of reliability critical domains, such as, for instance, transportation.

1. Introduction

Short-circuit robustness is a key application requirement for semiconductor power devices. The relative performance of silicon carbide (SiC) MOSFETs and silicon (Si) IGBTs has been amply discussed and compared in a number of studies (see [1-3], for example), which have pointed out a somewhat weaker withstand capability of SiC, as opposed to Si, and differing failure mechanisms. In particular, a twofold failure mechanism was highlighted in [4] for SiC, yielding either a fail-to-open-circuit (FTO, or *soft*) or fail-to-short-circuit (FTS, or *hard*) signature, depending on the energy dissipation rate and related temperature increase within the device.

A soft type failure is by far the preferred option in the application. Indeed, FTS behaviour typically implies failure propagation, loss of whole system functionality and potentially destructive events, with explosion-like characteristics; on the other hand, FTO behaviour results in the failed transistor shutting off: an intrinsic fault containment capability, which, in the case of parallel device or multi-chip modules based designs, still enables to operate the system, even if at reduced power ratings, without additional complex or costly circuitry [5]. Such an operational status is usually referred to as *hopping-home mode* and is a highly desirable feature of power conversion systems in some strategically relevant application domains, in particular transportation. For that reason, soft failing devices are of great interest and have already received dedicated attention in the recent past [6]: it was shown in particular that the failure is due to the progressive creation of cracks and aluminium (Al) diffusion leading to the partial shorting of the gate and source terminals, effectively reducing the gate-source bias voltage to values below the threshold voltage, thus turning off the device. Such effect was shown to interest mainly the inter-layer dielectric (ILD), a thicker oxide layer between gate and source terminals, which is directly in contact with the Al top metal

layer,

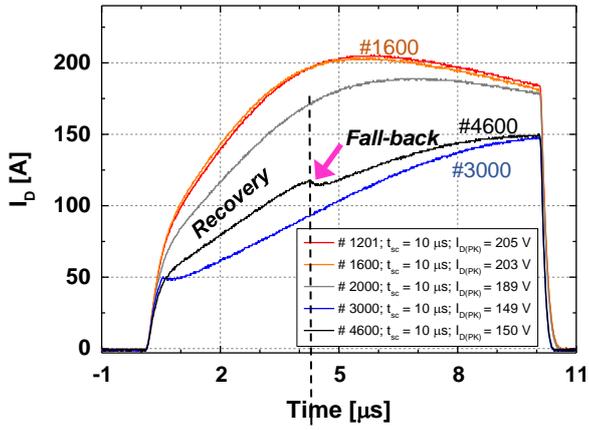
but not the thin field oxide region.

This paper extends the present understanding by more carefully controlling the progressive accumulation of damage and by discussing a very new observation, namely the possibility to recover device functionality after soft failure and re-impose a stable, even if slight degraded, characteristics by ad-hoc gate biasing conditions. Transient and static functional measurements are coupled with device structural analysis to yield in depth understanding of the phenomena and contribute to the development of SiC based power conversion systems with enhanced robustness and operability under critical conditions

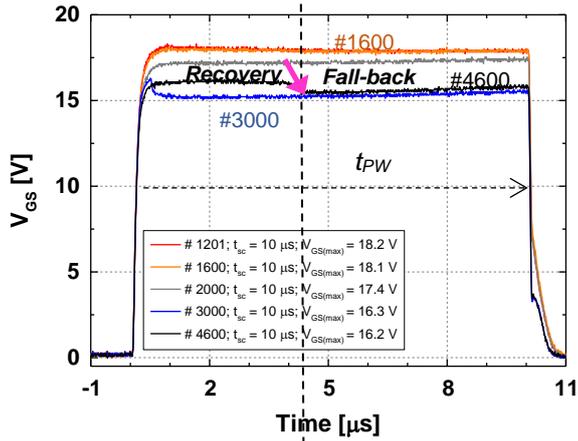
2. Functional characterisation

2.1 Short-circuit ageing analysis

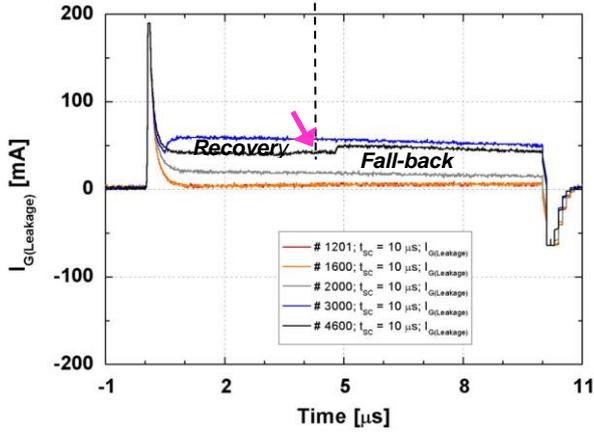
Fig. 1 shows the results of repetitive short-circuit tests on a commercial planar-gate 80 mΩ - 1200 V SiC discrete power MOSFET. Fig. 1 a) shows the drain current, I_D ; Fig. 1 b) the gate-source bias voltage, V_{GS} , and Fig. 1 c) the corresponding gate current, I_G . The pulse width is chosen to include a sufficient safety margin from the maximum device withstand capability ($t_{PW} = 10 \mu\text{s}$ compared to $T_{SC\ MAX} = 14 \mu\text{s}$), so as to avoid failure. Still, the pulse duration is long enough—to produce gradual damage accumulation: typically, for $t_{PW} < 6 \mu\text{s}$, no permanent damage can be detected. As is evident from these results, the device characteristics are progressively degraded during the test: to a reduction of I_D (Fig. 1a), corresponds a decreased V_{GS} (Fig. 1b), as a result of increased gate leakage current (Fig. 1c). As highlighted by the authors for SiC power MOSFETs under short-circuit stress in [7], creation of cracks and metal (aluminium, Al) diffusion lead to the partial shorting of the gate and source terminals. To support this hypothesis, thermal modelling and simulation of the chip temperature were carried out, as detailed in [8, 9]. The model takes into account the



a)



b)



c)

Fig. 1. a), repetitive SC DUT progressive degradation, manifest as a decrease of I_D after #1600 pulses with $t_{PW}=10 \mu s$ @ $V_{DS}=610 \text{ V}$ - $V_{GATE \text{ DRIVE}}=18 \text{ V}$ - $R_{GATE \text{ EXT.}}=47 \Omega$ - $T_{CASE}=25 \text{ }^\circ\text{C}$; b), corresponding V_{GS} waveform; c) corresponding I_{GS} waveform. In the results corresponding to pulse #4600, the device initially exhibits partial recovery, followed by degradation.

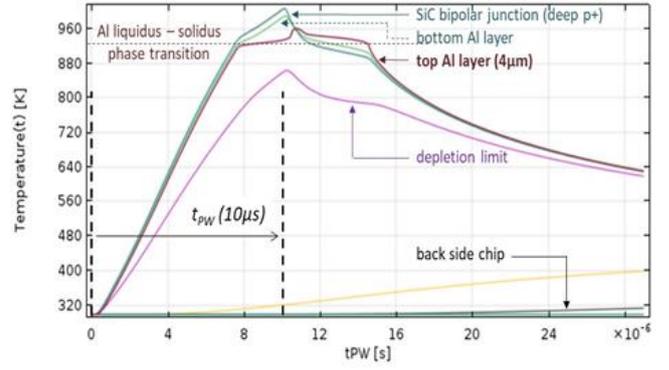


Fig. 2. Fig. 2 1D chip temperature simulation in short-circuit operation for #1600: $t_{PW}=10 \mu s$ @ $V_{DS}=610 \text{ V}$ - $V_{GATE \text{ DRIVE}}=18 \text{ V}$ - $R_{GATE \text{ EXT.}}=47 \Omega$ - $T_{CASE}=25 \text{ }^\circ\text{C}$.

temperature dependence of the conductivity and the mass heat of SiC and aluminium, as well as the solid-liquid phase transition of the Al top layer. Using structural computer aided design tools (specifically, ComsolTM was used here), the model received as input $I_D(t)$ waveform of Fig. 1a), with a constant V_{DS} value of 600 V. Considering pulse number #1600, Fig. 2 shows the temperature rise of all the main layers of the chip during the short circuit. It is clearly visible that the Al layer is above its melting point with a high thermal energy injected into its liquid phase. Furthermore, according to [10], at the Al melting temperature, the thick oxide is already cracked because the mechanical stress at the upper corner greatly exceeds its mechanical strength.

2.2 Gate-source damage recovery

On the side of the gate ageing observation, a new observation can be made in the results of Fig. 1: a partial recovery effect can be observed in going from pulse #3000 to pulse #4600 (in these tests, a KeysightTM B1505A source-meter-unit was used). Here, the recovery is not stable, and half-way through the pulse the device characteristics fall back to the previous degraded status. Because of its potential relevance for the application, this observation triggered further detailed analysis of the effect, specifically of the possibility to *force and control* the recovery and stabilise the device characteristics, even if at a slightly degraded level.

Based on the aforementioned findings of [6], a first attempt was made by statically sweep-biasing the degraded transistor (same device used previously for the tests of Fig. 1) in a V_{GS} range $\leq 12 \text{ V}$, with different limit values of gate pulsed current I_{GSS} . Fig. 3) summarises the results:

- *Step 1* (blue curve) corresponds to the first traced curve, in which the gate current was limited at 10 mA: here, as V_{GS} is increased beyond about 10.8 V, a sudden breakdown like characteristics is entered, with a steep increase of I_{GSS} ;
- *Step 2* (brown curve) is a second sweep carried out straight

after *Step 1* to confirm the breakdown status;

- Step 3 (red curve) is a sweep with increased I_{GSS} limit value

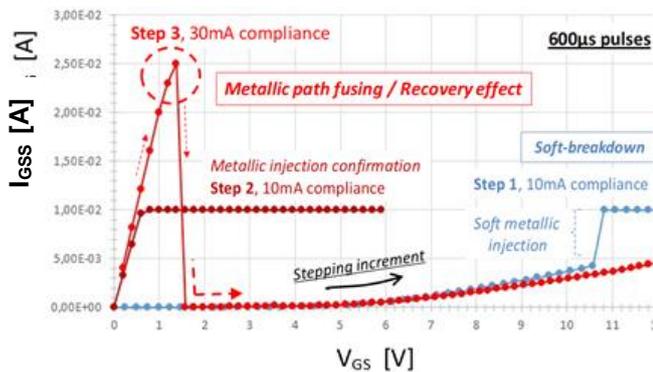


Fig. 3. Static characteristics of device degraded by repetitive short-circuit: first sweeping biasing-gate test highlighting breakdown and recovery effects.

to 30 mA: here, as V_{GS} is increased beyond just 1 V a recovery effect is manifest, with I_G dropping suddenly again.

These results point out that the device gate characteristics can be partially recovered by producing moderate heat generation in the gate region, which is ascribed to a fusing effect taking place, which effectively disconnects degraded portions of the chip from the remaining cells; in this case, the device reaches a new stable, though slightly degraded state. However, if the pulse width t_{PW} is increased closer to the maximum duration $T_{sc\ max}$ of the DUT, the level of damage accumulation is greater and for some devices analysed, the I_G value after recovery was found to be too high for them to be still usable with typical gate-driver designs. In Fig. 3), at the end of the first series of low-voltage gate sweeping, the measured equivalent gate-source resistance was $2.4\ k\Omega$, corresponding to a gate-drive supply of 135 mW at 18 V.

To try and get the entire gate recovery, a second series of transfer characteristics sweeping was carried out, the results of which are given in Fig. 4. Here, the gate bias voltage is increased up to the nominal voltage of 18 V at first and beyond such value subsequently. For reference, a Keysight™ B2902A SMU with 600 μ s pulse duration was used for these tests; the effect of the pulse duration is discussed at the end of this section.

Fig. 4a) shows that, for V_{GS} higher than 12 V and lower than 16 V, a chaotic transient behaviour appears when the limit gate current is moved from 5 to 12 mA (step 1 to step 6): a first metallic injection effect appears in the form of a soft breakdown of the oxide, following a fusing effect and a second metallic injection effect.

In Fig. 4b), by gradually increasing the limit gate current up to 30 mA and increasing the bias voltage from 16 V to 30 V, the chaotic behaviour disappears, giving way to a stable ohmic transfer characteristics. From an equivalent $R_{GATE} \cong 1.8\ k\Omega$ at 12 V in step 1, $R_{GATE} \cong 1.3\ k\Omega$ at 18 V in step 18, giving an acceptable gate-drive over-supply of 250 mW at 18 V to continue operation of the device in *hopping-home* mode.

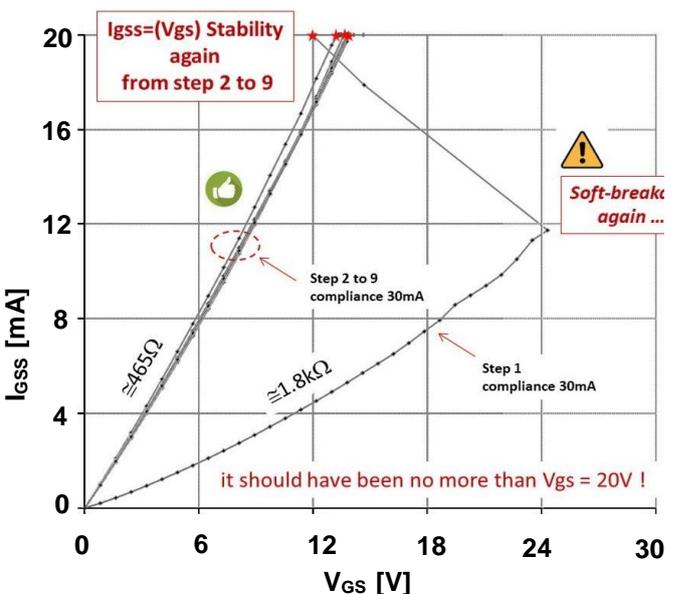
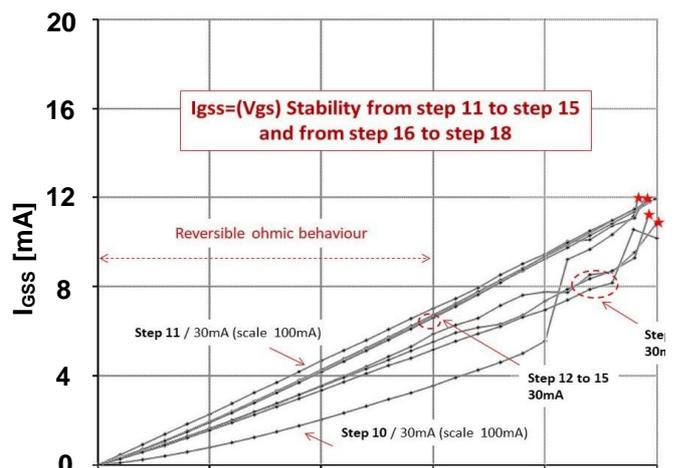
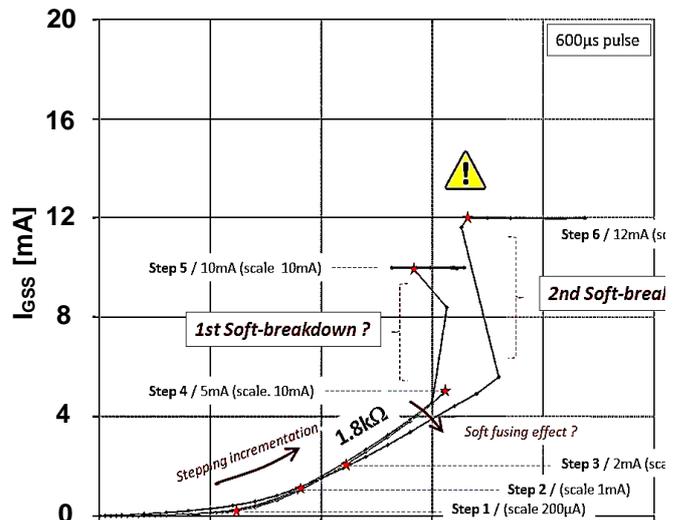


Fig. 4 $I_{GSS}(V_{GS})$ gate ohmic restoration analysis: a) 5 mA to 12 mA, b) 30 mA, c) high gate-source bias and final metallic crack. All graphs share the bottom x-axis and scaling, not repeated for better readability.

However, in Fig. 4c), in an attempt to further restore the gate oxide, the sweeping was repeated with a voltage bias higher than 18 V up to 30 V. A new stable ohmic state appears in this case with a lower $R_{GATE} \cong 465\Omega$ at 15V. Unfortunately, such value is too low, giving a gate-drive over-supply of 480mW at 15V. The preliminary qualitative conclusion can be drawn that the bias voltage and injected restoration energy values should be high enough to eliminate the main ohmic paths for the device to be usable at nominal gate voltage, but they should not be too high, so as not to re-metallize again the cracked oxide.

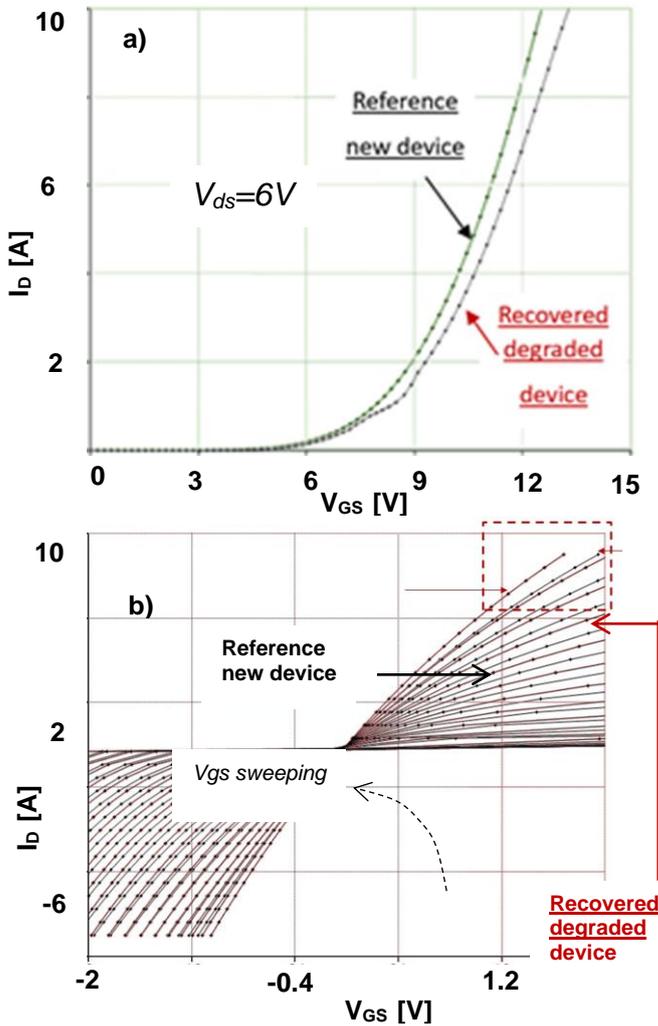


Fig. 5 Transfer and direct behaviour comparison @ $T_{CASE} = 25^\circ C$: a) $I_{DS}(V_{GS})$ @ $V_{DS} = 6 V$, b) $I_{DS}(V_{DS})$ curve.

Finally, in Fig. 4c), a final attempt was made to induce gate recovery by increasing the pulse duration from 600 μs to 600 ms. Even in this case of high energy injection, the ohmic state of the gate remains stable and, although the equivalent gate resistance is lower in this case, it remains nevertheless at a value which makes the device further use in a real circuit still possible,

as demonstrated in the next section.

2.3 Characteristics of partially recovered device

The device was then characterized with the same SMU for re-using. Fig. 5a) shows the transfer characteristics at $V_{DS} = 6 V$, comparing a new device and the recovered device from Fig. 4c). For illustration, at $V_{GS} = 12 V$, the comparison shows a decrease of only 20 % in I_D for the recovered device. The same behaviour is visible in Fig. 5b) on the output characteristics, which proves the potential re-usability of the device.

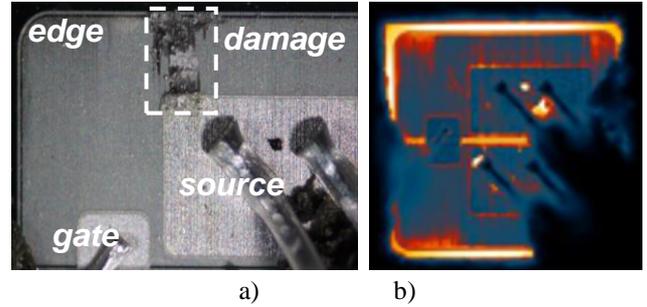


Fig. 6 a) Photograph of degraded device chip featuring damage accumulation at the boundary between gate-ring and source metal, b) LIT analysis @ $V_{GS} = 10 V$, $I_{GSS} = 10 mA$, $I_{DS} = 1 A - 25 Hz$.

3. Structural characterisation and partial recovered device operation

The plastic case of the device was opened by laser ablation followed by terminal chemical etching on the encapsulation resin. Fig. 6 a) shows the degraded die, with a very clear indication of severe damage to the top metal having accumulated in the proximity of the external gate-ring source-metal structural boundary. Lock-in-thermography analysis was also carried out, Fig. 6 b), which confirmed the abnormal heating of the cracked gate fingers around the corner region, where mechanical stresses are likely to be highest during the short-circuit. After opening, the device was re-used within a circuit, at reduced drain-source bias, and it was still able of correct transient operation, as demonstrated by the results in Fig. 7, which refer to a single short-circuit pulse. It can be seen that the channel saturation current is reduced of 37 % after the recovery gate-source process described above, as a result of the lowering of the $I_{DS}(V_{GS})$ curve presented in Fig. 5 a).

4. Conclusion

The possibility to implement self-healing capability, remindful of film capacitor behaviour, in SiC power MOSFETs by ad hoc design and biasing is a new and very appealing feature, which can greatly change the present way to look at semiconductor device and power converter robustness, reliability and availability in application. This paper has shown that, following short circuit ageing stress and damage

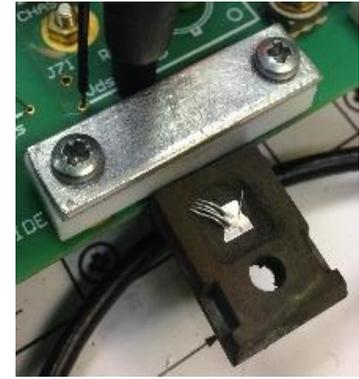
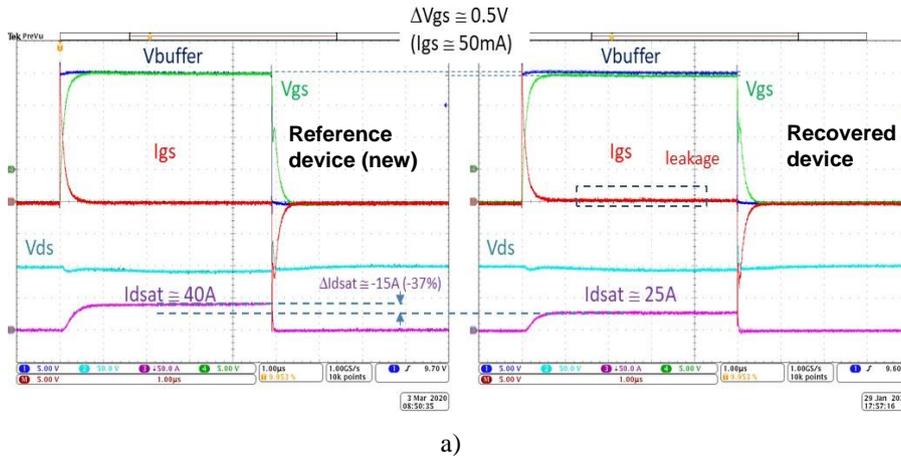


Fig. 7 Single-pulse short-circuit test ($V_{DS} = 100\text{ V}$; $V_{GS} = 15\text{ V}$, $R_{GATE} = 10\ \Omega$, $T_{CASE} = 25\text{ }^\circ\text{C}$): a), comparison of new reference device (left) and degradation-recovered device (right); b), photograph of recovered device in partly decapsulated TO247 package.

accumulation, it is still possible to partially restore the integrity of the gate structure by proper electrical biasing for a particular class of devices and contained stress and damage levels. Here, device recovery was implemented in an off-line setup by means of a simple pulsed mode source-meter-unit, by progressively increasing the gate current limit. This operation is only possible if the gate is not already damaged too severely. In addition, it was shown that the voltage and injected recovery energy should be high enough to eliminate the main ohmic paths to be used at nominal gate voltage, but not so high as to cause excessive metal diffusion within the cracked oxide, which would yield a permanent short-circuit between the control terminals. Further studies are being dedicated to the online implementation of the recovery capability in a real power conversion system.

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