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# Reliability, power losses and volume comparison for isolated DC/DC converters using Si and GaN devices

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**ABSTRACT** –This paper presents a comparison of four different isolated DC-DC converters: the Dual active bridge, the LLC resonant, the series LC resonant and the Phase-shift converter. The comparison evaluates three characteristics for a 3kW high/low voltage application: efficiency, power density and reliability. Time domain simulations are carried on each topology with Simetrix and Octave environmental to integrate the reliability analysis based on an output power profile yielding to select a converter topology as a function of these parameters. The difficult in to determine an accurate model to estimate the reliability of GaN power transistors is also discussed and by using the FIDES model, three different transistors are compared, two GaN power transistors and one Si mosfet. The analysis and simulation results identify, when designed with one of the GaN, the LC resonant and the Dual Active Bridge as the most efficient converters, and the LC resonant converter as the more reliable.

**Keywords**—DC-DC isolated converter, FIDES reliability guide, reliability models for GaN switches, MTF, power density, power efficiency.

## 1. INTRODUCTION

The demand for lower CO<sub>2</sub> emissions increases the request for high power density converters and higher efficiencies. The isolated DC/DC converters are present in a wide range of applications such as low voltage power supply for electric and hybrid vehicles, but also in the more electrical aircrafts. Four of the most common isolated topologies used for these applications are the resonant LLC, the series resonant LC, the Dual Active Bridge (DAB) and the Phase-shift converters. The converter's power density is inherently associated with the switching frequency that can be increased by using wideband gap materials, such as GaN. In this scenario, the lifetime must also be considered in the conception process. Indeed, reliability is a big challenge for GaN power transistors and FIDES, considered in Europe as the best prediction for reliability in power electronic systems, allows take into account this parameter [1]. Some research has been focused on the comparison of isolated DC/DC converters [2], but most of the studies do not focus on lifetime, which is relevant and should be evaluated in order to choose the best converter. In [3] the integration of reliability is also used in the pre-design of non-isolated interleaved Buck converter in order to help the selection of the most adapted converter. In [4] the reliability is used to compare different grid-connected converters composed by IGBT and diodes for wind energy conversion. The reliability applied for power converters connected to photovoltaic systems is discussed in [5]. These studies use the reliability as a tool to evaluate the converters in the pre-design stage, but use components that have a mature time life model, but, for components as GaN power transistors, the analysis becomes a little more complicated.

When higher power density is required, GaN transistors presents enormous advantages concerning not only volume but also efficiency; however, they present a challenge concerning time life because contrarily to Si MOSFET, there's no a well

established accelerated lifetime model based on years of experience for those components. In [7], it's discussed the construction of predictive models for the emerging technologies in FIDES, that are possible if the reliability tests are executed close to the extreme operating conditions. Despite the difficult in to identify the main failure mechanism in the new transistors, the use of activation energy seems to be a good parameter to include them in acceleration factors from reliability models [6].

The objective of this paper is to compare the efficiency, volume and time life of HV/LV isolated converters based on different power transistor technologies. These parameters normally can be used to help engineers to choose the best topology in a pre-design stage. The analysis of reliability from GaN devices is then discussed and integrated in the FIDES methodology to evaluate the time life of these components. This paper is organized as follows: Section 2 present the main difference between the isolated DC/DC converters, the choice of the components required in each topology for a specific application and the total power losses and volume estimation. In section 3, the FIDES model is then used in order to estimate the failure rate of each component and the Mean time to failure of each topology. It's also explained how the new GaN power transistors can be integrated in the FIDES methodology taking into account the difference between the structures: a direct enhancement mode and a cascode structure. In section 4, time domain simulations are then carried on each topology with an equivalent model for the power switches. A script in Octave using FIDES model, inserts the power profile in the simulation environment and a comparison of the reliability for an output power demand profile is obtained and discussed in section 5.

## 2. DESIGN AND COMPARISON OF CONVERTER TOPOLOGIES

For this study, isolated DC/DC converters are designed for a 3kW high/low voltage, typical application presented in electric vehicles, according to Table 1:

Table 1. DC/DC power converter requirements for the application example.

V <sub>in</sub> (V)	V <sub>out</sub> (V)	P <sub>out max</sub> (W)	F <sub>sw nom</sub> (kHz)
290-400	10-14	3500	100

The four studied converters are illustrated in (Fig. 1).

The LLC resonant converter (Fig. 1A) and the LC series resonant converter (Fig. 1B) are designed by using the equivalent First Harmonic model [9]. The main difference between the two resonant converters is the role of the transformer magnetizing inductance: the LLC is composed by a series inductance (L<sub>r</sub>) and a series resonant capacitor (C<sub>r</sub>) but also it uses the magnetizing inductance (L<sub>m</sub>) to obtain a second resonant frequency. In the case of the LC series resonant, only the series inductance L<sub>r</sub> and capacitor C<sub>r</sub> are used in the resonance; the magnetizing inductance could be considered infinite in this converter. In the design of the LLC converter (Fig. 1A), the series inductance and the magnetizing inductance

have similar magnitudes characterizing two closers resonance frequencies, but in the LC (Fig. 1B)  $L_r$  is too small when compared with  $L_m$  and normally the frequency variation range to regulate the output voltage is higher. Both converters are designed to operate under variation of the switching frequency, but the main resonant frequency is fixed at 100 kHz for both converters in the application example.

The DAB converter (Fig. 1C) operates with a fixed switching frequency, but the output regulation is made by adding a phase delay angle between the voltages on the transformer sides. Different command modes can increase the efficiency of this converter by realizing Zero Voltage Switching (ZVS) over an expanded output voltage range [10].

The Phase-shift converter (Fig. 1D) also operates under fixed switching frequency, but differently from the DAB, the output regulation is made by an internal phase delay angle used between the two half-bridges on the primary side. The secondary structure consists in a current doubler that also could be placed by a full-bridge as in the other topologies; however, the first structure allows reducing the conduction power losses and has a series of advantages over other structures [11], being also recommended for high current operation.

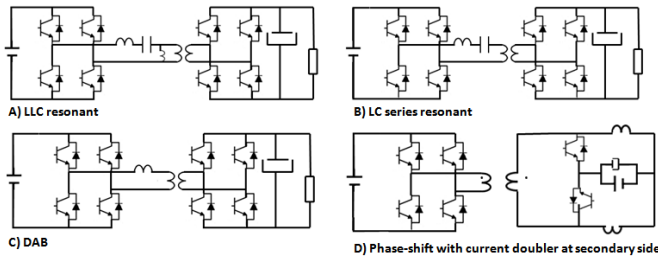


Fig. 1: DC/DC isolated converter topologies.

In the design of the LLC and the LC resonant converters, keeping the switching frequency always higher than the resonance frequency, is possible to ensure ZVS in the primary side and ZCS in the secondary side. In the case of the DAB converter, the converter is designed with the methodology presented in [12] with optimal operation at nominal conditions; however, under light output power and high output voltage the converter loses the capability of soft-switching and the same occurs with the phase-shift converter.

The converter designs are presented in Tableau 2.

Tableau 2: The design parameters for 3.5 kW.

Volume	LLC	LC	DAB	P-Shift
F <sub>sw</sub> (kHz)	85-115	75-125	100	100
Cr (nF)	34.5	68	-	-
L <sub>r</sub> (uH)	73	37	57	10
L <sub>m</sub> (uH)	110	-	-	-
N <sub>ab</sub>	28	28	28	26
I <sub>p</sub> rms (A)	15.5	14.7	12.5	7.75
I <sub>s</sub> rms (A)	441.9	429.1	357.1	168
ΔI <sub>out</sub> (A)	187.5	120.9	110.1	35.6
C <sub>out</sub> (uF)	432	268	505	178
V <sub>sd2</sub> max (V)	34	49	32	42

## 2.1. Volume and total power losses estimation

The total volume occupied by the converters is considered as the sum of the volume occupied by the output filter (capacitors, inductors), the volume occupied by the transformer, including the magnetizing inductance in the case of the LLC resonant converter (if the inductance is not integrated in the transformer), the volume of the series inductance, the power switches and the heat sink.

The output capacitor volume for each converter depends on the RMS current, capacitance and maximum voltage. For this example, solid tantalum capacitors are selected and used in parallel to reduce the current ripple. The Phase-shift converter is the converter that requires the smallest output capacitance due to the presence of the two inductors in the secondary side that smooth the output current.

Tableau 3: Output capacitance: C<sub>base</sub> = 82 uF/35 V (12 Arms / cap - ESR = 10 mΩ @ 100 kHz).

	LLC	LC	DAB	Phase-shift
Δ I <sub>out</sub> (A)	187.5	120.9	110.1	35.6
Cap (uF)	268	432	506	178
Vol (cm <sup>3</sup> )	29.69	19.73	17.90	1.79
Loss (W)	7.25	4.38	3.99	0.26

The power losses in the capacitors are presented in Table 3 and are calculated with the datasheet information:

$$P_C = \Delta I_{out_{RMS}}^2 \times ESR_{equivalent} \quad (1)$$

The volume occupied by the transformer is estimated by the product between the effective magnetic core section area  $A_e$  and the winding area  $A_w$ . This product establishes the closest available magnetic core to construct the transformer and it's determined by knowing the applied voltage waveform, the RMS current in the windings, the number of turns, the peak flux density  $B_{max}$ , the current density  $J$ , and a feasible window utilization factor  $Fu$  [13], that normally for discrete transformer can be settled between 0.35 and 0.40.

$$A_e A_w = \frac{V_{Pmax}}{2 F_{sw} N_p B_{max}} \left( \frac{N_p \left( \frac{I_{pRMS}}{J} \right) + N_s \left( \frac{I_{sRMS}}{J} \right)}{Fu} \right) \quad (2)$$

Ferrite core E shape from Magnetics is considered with a same magnetic material for the four converters. The inductor volume estimation is similar to that used for the transformer, but its effective magnetic core section area is directly proportional to the peak current, due to the maximum stored energy:

$$A_e A_w = \frac{L \Delta I_{max}}{N B_{max}} \left( \frac{N \left( \frac{I_{LRMS}}{J} \right)}{Fu} \right) \quad (3)$$

The power losses are estimated in the inductor and in the transformer. The magnetic core power losses are calculated by Steinmetz equation [14] and by using the information available on the datasheet considering the volume of the core. The winding power losses are estimated by the product between the RMS current and the equivalent resistance. In the case of the phase-shift converter, the output filter inductances are also considered, but in this case only the power loss due to the DC winding resistance is considered.

Tableau 4: Volume and transformer power losses at nominal operation conditions, 3.5 kW and 100 kHz.

	LLC	LC	DAB	Phase-shift
Vol. (cm <sup>3</sup> )	141.2	123.7	122	88.52
Losses (W)	10.5	8.75	9.62	5.25

In the case of the power transistors, the power losses are evaluated and a heat sink is calculated to prevent that the component has its junction temperature higher than the maximum allowed temperature. The total power losses, divided between conduction and switching power losses, are evaluated in Simetrix and compared with analytical expressions considering ZVS turn-on on the primary and ZCS on the secondary sides for the resonant converters and hard-switching at light load for the Phase-shift and DAB converter. It's also

considered that the converters are synchronously rectified in order to prevent the reverse conduction power losses on the low voltage side. Reverse recovery energy is also considered for the ZVS turn-on condition.

$$P_{Cond} = R_{on} I_{DS_{rms}}^2 \quad (4)$$

$$P_{SW} = \frac{1}{2} V_{DS} I_{DS} (T_{on} + T_{off}) F_{SW} + Q_{rr} V_{SD} F_{SW} \quad (5)$$

The junction temperature is determined by the product between the total power losses produced by the device and its thermal resistance between case and junction  $R_{thjc}$ , added to the case temperature,  $T_c$ . If it's necessary,  $T_c$  is reduced by increasing the size of the heat sink. It's also considered individual's heat sinks for high and low voltage sides considering the ambient temperature of 40°C.

$$T_j = P_T R_{thjc} + T_c \text{ (Heat sink volume)} \quad (6)$$

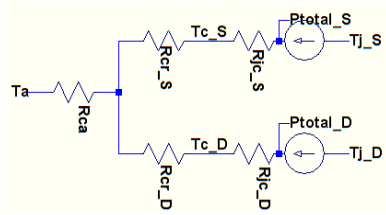


Fig. 2: Thermal equivalent model to estimate the mosfet junction temperature.

The thermal and electrical main characteristics of the three different 650V power transistors are presented in the following table.

Tableau 5: Power transistors characteristics.

	IPx65R099	TPH3205WSB	GS66516T
Rdson (mΩ)	99	49	32
Rth JC (°C/W)	0.45	1.0	0.3
Tfall (ns)	6	8.6	22
Trise (ns)	9	7.6	12.4
Trr (ns)	615	40	0
Qrr (uC)	14.8	0.136	0
Vsd (V)	0.9/12Vgs	1.6/8Vgs	2.0/6Vgs

### 3. RELIABILITY USING FIDES GUIDE MODEL

In order to estimate the lifetime of the converters, FIDES methodology was investigated.

The methodology FIDES described in [15] and [16] is a result of a study began in 2001 by 8 companies in France and proposes a methodology for electronic system reliability. The methodology takes into account failure rates from the manufacturing process, design process and from the system's life profile, where the constraints as thermal, electrical and mechanical over stress are also evaluated. Its' also possible, include new technologies in the methodology because of its characteristic.

The failure rate ( $\lambda$ ) is a constant and is based on the useful life of the system containing also the contribution of each individual component in the power converter, represented by the equation (7):

$$\lambda_{Converter} = \sum_i \lambda_{Component_i} \quad (7)$$

For each component,  $\lambda$  is the product of three factors, as represented in equation (8): the part manufacturer acceleration factor,  $\pi_{PartMan}$ , representing the manufacturing quality of the component and the manufacturer qualification; the process acceleration factor,  $\pi_{Process}$ , that includes quality and technical control in the product lifecycle; and the physical failure rate,  $\lambda_{Physical}$ , which includes the base failure rate and physical constraints during its operational useful life, as temperature, humidity and mechanical vibrations [15] [16].

$$\lambda_{Component} = \lambda_{Physical} \pi_{Process} \pi_{PartMan} \quad (8)$$

The load profile presented in (Fig. 3) is used to determine the failure rate of the converters.

The failure rates obtained by the FIDES methodology are expressed in a calendar of a yearly profile (8760 hours) where each phase described in (Fig. 3) must be weighted by the phase's duration. It's considered in this application example that the demanded power profile applied on the converters occurs 365 times during a year.

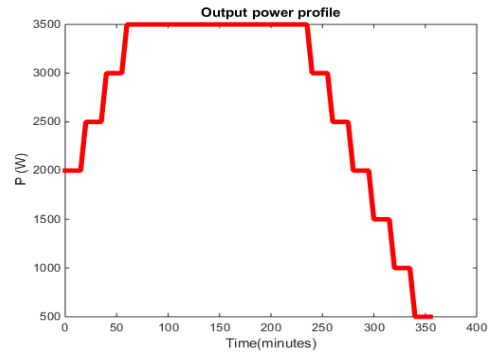


Fig. 3: Power load profile application required once by day.

Three groups of components in each converter are submitted to the power load profile from (Fig. 3): the magnetic components consisting of the high frequency transformer, the resonant inductance and power inductors, as well the output filter inductances; the output capacitors and the semiconductors from high and low voltage sides. In the high voltage side are considered three different transistors: a 650V MOSFET CoolMOS technology (IPx65R099-TO247), a 650V GaN FET normally- off device in a cascode structure (TPH3205WSB-TO247) and a 650V enhancement mode GaN direct-driven power transistor (GS66516T topside cooled type package) presented in Tableau 5. On the low voltage side, a same Si MOSFET is considered for all the converters, the IPT007N06N.

#### 3.1. The reliability of active components

In this section, the failure rates associated with the power transistors are determined. It consists in to find the elements described in (8) for the three different semiconductors.

The physical part has 3 contributions:

$$\lambda_{phy} = [ \sum_{PhyContribution}^N (\lambda_0 \pi_{acceleration}) ] \pi_{induced} \quad (9)$$

$\pi_{induced}$  is the overstress due to the physical position of the final converter, due to the most influence overstress on the application, due to the sensitivity to the overstress and the influence of the policy for taking into account those overstresses during the system development phase. These

parameters are resumed in equation (11). The audit questionnaire proposed in FIDES [15] (page: 50-54) is used to evaluate the criteria for mechanical and thermal overstresses being differentiated for the power transformer, capacitors and inductors, but not for the three different high voltage side power transistors.

$$\pi_{induced} = (\pi_{placem} \pi_{appl} \pi_{rugg})^{0.511 \ln(C_{sensitivity})} \quad (10)$$

For each component presented in the power systems, the product between the acceleration factor ( $\pi_{acceleration}$ ) and its base failure rate ( $\lambda_o$ ) has the influence of five constraints: the thermal constraints related to the junction temperature, casing and solder joints, respectively and the influence of humidity and mechanical vibrations, as presented in equation (12).

$$\lambda_{phy} = \sum_i^{Phases} \frac{t_{annual}}{8760} (\lambda_{OTH} \pi_{TH} + \lambda_{THCasing} \pi_{THCasing} + \lambda_{THSolder} \pi_{THSolder} + \lambda_{Hum} \pi_{Hum} + \lambda_{Mech} \pi_{Mech}) \pi_{induced} \quad (11)$$

The thermal acceleration factor  $\pi_{TH}$  is modeled by Arrhenius equation and one of the physical tests associated with this model is the High Temperature Operating Life (HTOL) executed according to the JEDEC EIA JESD-22-A108A standard:

$$\pi_{TH} = e^{\frac{E_a}{k} \left( \frac{1}{T_{use}} - \frac{1}{T_{stress}} \right)} \quad (12)$$

In FIDES,  $E_a$  is assumed as 0.7eV because it's considered as the activation energy associated with the thermo-electrical failure mechanism for Si FETs;  $k$  is the Boltzmann constant,  $8.617 \times 10^{-5}$  eV/K.  $T_{use}$  is the reference temperature of the component and  $T_{stress}$  is the temperature achieved due to the stress.

The thermal acceleration factor of the case  $\pi_{THCase}$  and of the solder joints  $\pi_{THSolder}$  use the Norris-Landzberg model and represents the fatigue mechanism due to temperature variation. In FIDES it appears with an equivalent  $E_a$  of 0.122 eV for both parts, case and solder joints:

$$\pi_{THX} = \left( \frac{12 N_{Cyannual}}{t_{annual}} \right) \left( \frac{\min \theta_{cy}}{2} \right)^P \left( \frac{\Delta T_C}{\Delta T_o} \right)^m e^{\frac{E_a}{k} \left( \frac{1}{T_o + \Delta T_o} - \frac{1}{T_{Cm}} \right)} \quad (13)$$

$N_{Cyannual}$  and  $t_{annual}$  are the annual n° of cycles and the annual duration of the phase respectively.

$\Theta_{Cy}$  is the cycle duration in hours.

$T_{Cm}$ ,  $T_o$ ,  $\Delta T_o$  and  $\Delta T_{Cy}$  are the maximum cycle temperature, the reference temperature, the reference thermal amplitude and the thermal amplitude of the cycle respectively.

$m$  is the fatigue coefficient of the material

$P$  is the acceleration power of duration factor, 1/3 in FIDES.

The relative humidity  $\pi_{Hum}$  and mechanical vibrations  $\pi_{Mech}$  factors are based on Peck's and Basquin's models; and a same influence of those parameters is considered for the three power devices. The complete equation can be verified in [15], [16].

The information concerning the Silicon MOSFET reliability is a result of mature qualification experience and the particular MOSFET IPX65R099C is qualified according to the JEDEC (J-STD20 and JESD22). The qualification of Silicon power transistors normally consists of avalanche and Safe Operating Area testing, but the GaN materials have different failure

modes which difficulties the development of a single evaluation methodology for those components.

According to [17] the qualification of the GaN transistors should be done differently for their specific failure modes instead of using the same tests used for Silicon transistors and a switching mode test should be used in order to evaluate the failure mechanisms in hard –switching. However, as can be verified by the reliability report from TPH3205WSB [18], the activation energy determined by JEDEC procedure matches with the activation energy determined by the acceleration high temperature switching operation test for this particular device. This result can be explained by the cascode structure of the device.

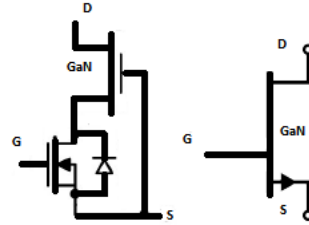


Fig. 4: Enhancement mode device structures a) TBS3205WSB b) GS66516T.

In the cascode structure of the TPH3205WSB (Fig. 4A), the voltage drive is applied to the Si mosfet in series with the GaN transistor, contrarily the other GaN device (GS66516T receives directly the drive voltage). This characteristic helps to understand why the qualification tests applied to the first device present similar results, since the operating conditions in the off-state and on-state have more similarities with the Si mosfet behavior, contrarily of the enhancement mode direct drive device represented in (Fig. 4B). Furthermore, as explained in [18], the distribution of the voltage between the parasitic capacitances in off-state can generate an avalanche effect that also characterizes one of the failure mechanisms represented by the well established models.

Despite the difficult in to establish a model to describe the failure modes of GaN transistors, an attempt is made by considering only different thermal acceleration factors in the physical part for the three different power transistors. It consists in to determine different activation energies for  $\pi_{TH}$ ,  $\pi_{THCase}$  and  $\pi_{THSolder}$ .

The activation energy ( $E_a$ ) in the three first acceleration factors is well defined for Silicon mosfets. For the qualified cascode GaN device, this information is available in the reliability report [18], as 1.84eV due to the thermal-electrical stress (used in the term  $\pi_{TH}$ ) and 0.09 eV for  $\pi_{THCase}$  and  $\pi_{THSolder}$  acceleration factors.

A previous study shows that the activation energy for GaN devices is between 1.05 and 2.5 eV [19]. An equivalent energy of 2.0 eV is used for the non-qualified device. In [20], a multi-parametric BAZ model shows the increasing in the probability of non-failure if the energy associated is also increased and the role of humidity and voltage are used to predict the necessary energy.

In order to differentiate the GaN and Si semiconductors, not only the physical part is evaluated, but also the manufacturer acceleration factor  $\pi_{partMan}$  in equation (8). The part manufacturer acceleration factor is determined by using equation (14).  $QA_{manuf}$  is the description of the manufacturer quality assurance level,  $QA_{comp}$  is the description of the component quality assurance level and  $RA_{comp}$  is the risk level of the component associated with the test performed. For those three factors, the highest assurance level is equal to 3, when the assurance level obtained is higher than the reference state of the



art or ultra passes the expectation; and 0 in the worst case, when there's no available information or when any qualification test was performed.

$$\pi_{PartMan} = e^{1.39[1 - (\frac{QA_{manuf} + QA_{comp}RA_{comp}}{36})\epsilon] - 0.69} \quad (14)$$

$\epsilon$  is the experience factor that the component buyer may have with his supplier and in the studying case is considered the same for all the three devices.

### 3.2. Capacitor, transformer and inductor reliability

The failure rates of capacitors, transformer and inductor are also determined according to equation (8).

For the output capacitors, the RMS current is one of the most important specifications for its reliability and it also affects the converter's efficiency resulting in a different impact for each topology studied. The most part of power converter designers combine technologies such as Tantalum, Aluminum and Tantalum Polymer in order to reduce cost and attend the requirements of current ripple and a lifetime; in some cases is necessary to investigate different combinations to find the best configuration. In this study only Tantalum capacitor is considered.

The part manufacturer factor and process are determined as in the case of active components. The physical part associated includes mechanical, thermal and thermo-electrical acceleration factors and in the induced factor, the relative sensitivity is defined for the solid tantalum capacitor for electrical, thermal and mechanical overstress as indicated in the FIDES guide[15], [16].

The physical failure rate is presented in equation (15). This same equation is also used for transformer and inductors. The voltage applied ( $V_{applied}$ ) on the capacitor, the maximum voltage specified by the supplier ( $V_{rated}$ ) and the board temperature, are the factors contributing to physical stresses in the capacitors. The thermo-electrical acceleration factor is calculated in equation (16):

$$\lambda_{phy} = \lambda_{cap} \sum_i^{Phases} \frac{t_{ann}}{8760} (\pi_{TH} + \pi_{TCy} + \pi_{Mec}) \pi_{ind} \quad (15)$$

$$\pi_{THCap} = 0.94 \left( \frac{V_{applied}}{0.4 V_{rated}} \right)^3 e^{\frac{E_a}{k} \left( \frac{1}{293} - \frac{1}{T_{boardamb} + 273} \right)} \quad (16)$$

$$\pi_{THTrafo} = 0.15 e^{\frac{E_a}{k} \left( \frac{1}{293} - \frac{1}{T_{boardamb} + \Delta T + 273} \right)} \quad (17)$$

$$\pi_{THInduc} = 0.09 e^{\frac{E_a}{k} \left( \frac{1}{293} - \frac{1}{T_{boardamb} + \Delta T + 273} \right)} \quad (18)$$

The estimation of the magnetic component reliability, transformer and inductors are also described with the same acceleration factor models as in the capacitor study, but the temperature rise relative to the ambient temperature is used as recommended in the FIDES methodology (30°C for high power transformer), if there's no other available method. In order to evaluate the variation of temperature in the transformer due to the winding power losses, an equivalent thermal resistance was estimated considering the nominal power losses and the maximum allowed temperature. In [27] has established an empirical formula to associate this thermal resistance with the volume of the magnetic core. It's also assumed that the core

loss corresponds to the half of the total transformer loss, which is acceptable for a good designed transformer.

$$P_{trafo} = \left[ \left( \frac{\Delta T_{max}}{\sqrt{V_{core} (cm^3)}} \right) 24 \right] \quad (19)$$

In [21] the thermal stress in a power transformer is evaluated with a focus on a mission profile. A more precise analysis is recommended for planar transformers because the heat flow exchanged is not always performed as expected due to its physical placement on the board.

## 4. INTEGRATION OF THE RELIABILITY USING FIDES GUIDE MODEL

For each power converter, the demanded power profile is inserted in Simetrix, where the converter is simulated for the different input conditions. The power profile is defined in a script in Octave environmental that runs the transient simulation in the first environmental and recovers the information after each cycle of the simulation. In Simetrix, the power switches are modeled by a switch that contains the information provided by the manufacturer. The model available on their websites could also be used for the simulations; however the simulation takes more time to achieve the steady-state.

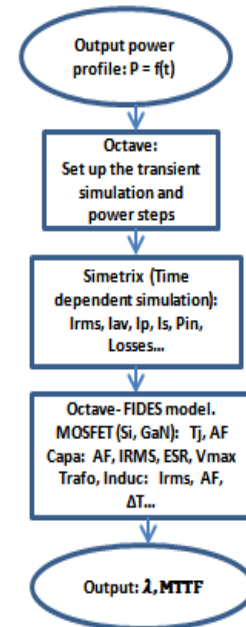


Fig. 5: Flowchart of the platform that integrates the FIDES model with time dependent simulations.

The simulation results, consisting of current and power losses in each power transistor and the current in the primary and secondary transformer winding are then loaded with Octave and the thermal equivalent model of the power switches and the reliability model for all the evaluated components, are used to determine the Mean Time to failure (MTTF) of the converter, presented on (Fig. 5). The total stress is derived from the rain flow counted cycles over a year [22].

After obtaining the failure rate of each component, the total failure rate of the converter is obtained by equation (7). This failure rate is the number of failures per unit of time. The equivalent Mean Time to failure in years is obtained by considering the FIT of the converter, which consists in the measure of failure rate in  $10^9$  device hours.

$$MTTF_{years} = \frac{10^9}{\lambda_{converter}} \frac{1}{8760 \text{ hours}} \quad (20)$$

## 5. SIMULATION RESULTS AND LIMITATIONS

Results in (Fig. 6) and (Fig. 7) show the volume and efficiency for the different topologies considering the power profile presented in section 3. It's necessary to recall that the volume occupied by the resonant topologies and also for the DAB converter can be reduced by increasing the switching frequency without reducing the efficiency due to lower power losses generated in the GaN devices. Not only because the transformer can be reduced, but also the series inductance. The same does not occur with the same proportion for the Phase-shift converter due to the two output inductors. Comparing its efficiency with the LLC resonant converter, the first one has the smaller circulating energy and smaller rms currents justifying its better performance.

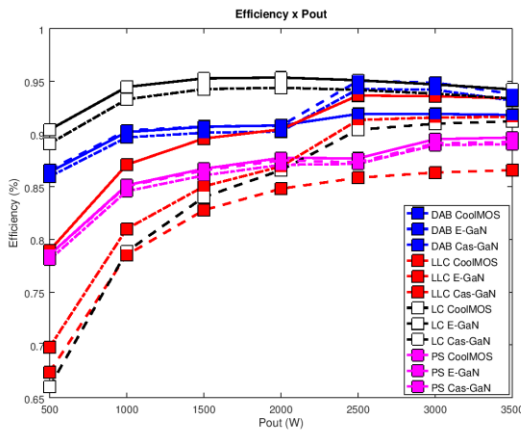


Fig. 6: Estimated performance of the LLC, LC, DAB and Phase-shift. Converters designed with different power switches.

Although the cascode GaN has better  $\pi_{PartMan}$  than the E-mode GaN and can achieve the same  $T_{jmax}$  as the other devices, the topologies DAB and LLC occupy more volume with the first device. Indeed, as its thermal resistance is higher, we need to increase the heat sink size in order to decrease its junction temperature and increase its lifetime. The LC series resonant and the DAB converters with HEMT GaN look the most efficient topologies for this configuration. Furthermore the LC presents the highest lifetime.

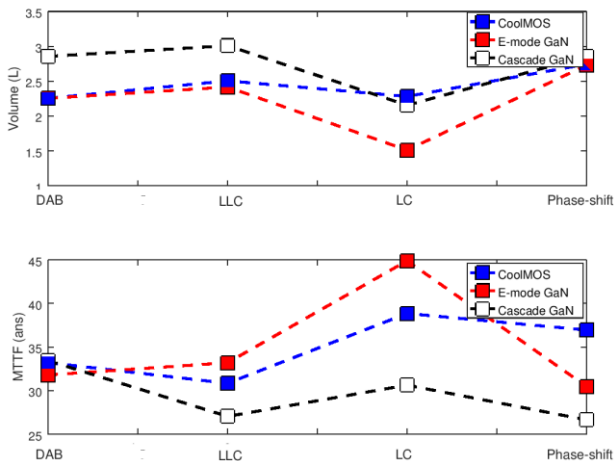


Fig. 7: Volume, MTTF- LLC, LC, DAB and Phase-shift. converters.

In (Fig. 8) the failure rate obtained for a single power transistor connected at high voltage side is presented. It confirms the

BAZ prediction model in [20] that the non-failure probability increases with the activation energy, but also shows the role of junction temperature in the failure rate. The higher the temperature elevation between junction and case of the device, higher needs to be the additional heat sink in order to reduce the probability of failure. Furthermore, the fact that the GaN transistors support higher temperature has an impact in their reliability model.

It's necessary to remark that the reliability study is only applicable in the range for which the components are qualified. In the case of the non-qualified GaN power transistors, it's assumed that its characteristic assumptions are enough to this application range. The FIDES Guide is applicable only for ambient range temperature between  $-55^{\circ}\text{C}$  and  $125^{\circ}\text{C}$ .

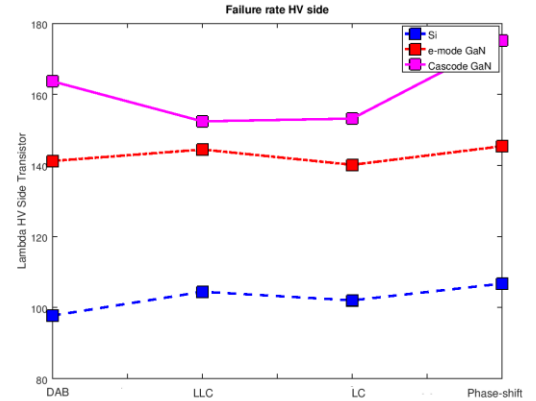


Fig. 8: Failure rate of a single power transistor connected at High Voltage side.

## 6. CONCLUSIONS

The comparison of four different DC-DC isolated converters considering efficiency, reliability and volume was investigated. The comparison of three different power switches, including a Si CoolMOS, a cascode GaN and an E-mode GaN, showed the importance of its thermal characteristics in the lifetime prediction. At 100 kHz, the LC resonant followed by the DAB converter designed with the E-mode GaN transistor are most promising topologies considering efficiency, but the LC resonant seems more robust with respect of the lifetime. The difficulty in obtaining more data concerning the reliability of the non-qualified transistors can be surpassed using the FIDES guide and estimated base failure rates associated with the device. However, the activation energy and the use of the part manufacturer factor are not enough to estimate their reliability with accuracy comparing with Silicon mosfet. It could be used for comparing similar technologies, as used for both GaN structures, but it's necessary to include different acceleration factors to evaluate the most influent failure mode of a particular GaN structure, either for the cascode structure or for the direct-drive enhancement mode transistor. From the results is also possible to verify that the MTTF is a compromise between volume and  $T_j$  and can be increased by using a larger heat sink.

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