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► **To cite this version:**

S. Ahmad, S. Blin, S. Callier, J.B. Cizel, S. Conforti, et al.. OMEGA SiPM readout ASICs. SiPM workshop: from fundamental research to industrial applications, Oct 2019, Bari, Italy. pp.164628, 10.1016/j.nima.2020.164628 . hal-02981274

HAL Id: hal-02981274

<https://hal.science/hal-02981274v1>

Submitted on 17 Oct 2022

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OMEGA SiPM readout ASICs

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Abstract

The paper describes various multi-channel ASICs designed by OMEGA laboratory and WEEROC company to readout SiPM or MPPC-based detectors used in particle physics or astrophysics experiments.

Keywords: SiPM, Photo Detectors

1. Introduction

The use of SiPMs has been very early associated to readout ASICs as they were often used in large numbers to cover a sizeable area. OMEGA laboratory started in 2004 to design readout ASICs for calorimetry in High Energy Physics, with chips as SPIROC or EASIROC/CITIROC. The performance and compactness provided by these ASICs helped to make the SiPM arrays performant and easy to use. The excellent timing properties of SiPMs were quickly recognized and there again fast ASICs allowed to exploit this feature and were used in time of flight PET medical applications. More recently, LHC upgrades at CERN make use of large quantities of SiPMs and need new ASICs to read them out at high rate.

2. ASICs for SiPM calorimetry : SPIROC and CITIROC

SiPM were quickly seen as an alternative to photomultipliers for calorimeter readout, in particular for the readout of scintillating fibers for which the small sensor area was not a drawback. The first large scale detectors were built in the CALICE collaboration [1], aiming at a large hadronic calorimeter for the International Linear Collider (ILC) built with scintillating tiles readout by SiPM to sustain the large magnetic field. For this application, OMEGA has designed and fabricated SPIROC ASIC described below [2].

2.1. SPIROC

SPIROC is a 36 channels readout ASIC for SiPM hadronic calorimetry developed for the CALICE collaboration. It measures the charge up to 2000 photoelectrons (320 pC) in two gains, digitized with two internal 12bit ADCs. It is designed to auto-trigger on 1/3 photoelectron (50 fC) and stores up to 15 samples in an analog memory before the events are digitized and readout. A timing information with a 100 ps TDC is also

included. A power pulsing capability has been implemented to reduce the power dissipation by 99% when there is no beam, taking advantage of the bunched accelerator. This allows to embed the chips inside the detector, while reducing drastically the cooling necessity, as they dissipate only 25 uW in average.

The schematic diagram of the chip can be seen in Figure 1.

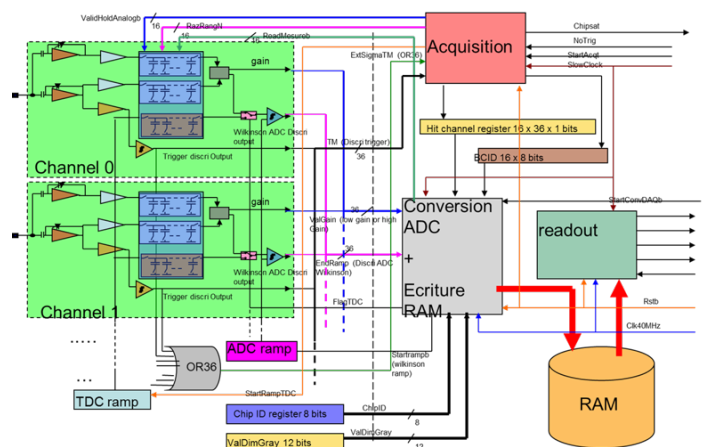


Figure 1: Schematic diagram of SPIROC aASIC designed to readout SiPM based hadronic calorimeter in CALICE.

Two voltage sensitive preamplifiers in parallel cover the large dynamic range. A fast shaper on the high gain path drives a fast discriminator, which provides the auto-trigger function and generates the hold signal in the analog memory. Once the acquisition cycle is complete, the analog data are converted in 12bit Wilkinson ADCs and TDC and stored in an SRAM memory. The data are then serialized and output at 40 MHz.

The performance has been measured extensively on test bench and in test beam. All the results can be found in the references of [1] and [2]. An emblematic plot is shown in Figure 2, which represents the few photons spectrum obtained in the testbeam setup by the DESY team with a calibration LED pulser. The individual photoelectron peaks are well separated, showing a single photoelectron to noise ratio larger than 10.

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SiPM SPECTRUM with Autotrigger

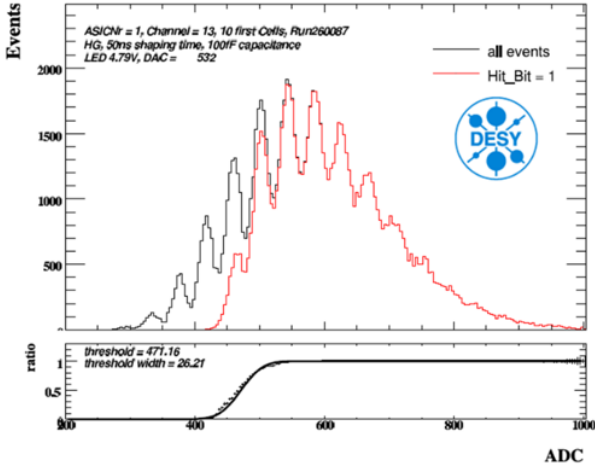


Figure 2: Low light spectrum obtained with the CALICE prototype readout with SPIROC2B.

More than 2000 chips were produced and equip a large size calorimeter prototype, extensively studied in test beam by the CALICE collaboration.

2.2. CITIROC

A variant of the chip has been designed for the ASTRI collaboration who develops SiPM-based telescopes for the Cerenkov Telescope Array (CTA) experiment [3]. The analog part of SPIROC has been conserved, while the digitization and digital part were removed and are performed externally in order to reduce the dead time. A peak sensing holder has been introduced in order to be un-sensitive to the dispersion in the time of arrival of the different photons from the Cerenkov image [4].

The block diagram of the chip is shown in Figure 3. It follows a similar architecture than the SPIROC chip, without the digitization, which is performed outside the chip at 2 MHz [5].

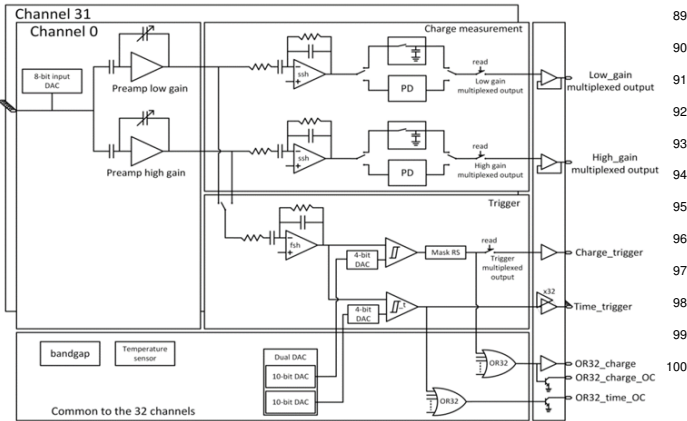


Figure 3: Block diagram of CITIROC ASIC.

A large telescope prototype has been produced, equipped with SiPM 8x8 arrays, readout by CITIROC ASICs. Good results are obtained [6], as shown in Figure 4.

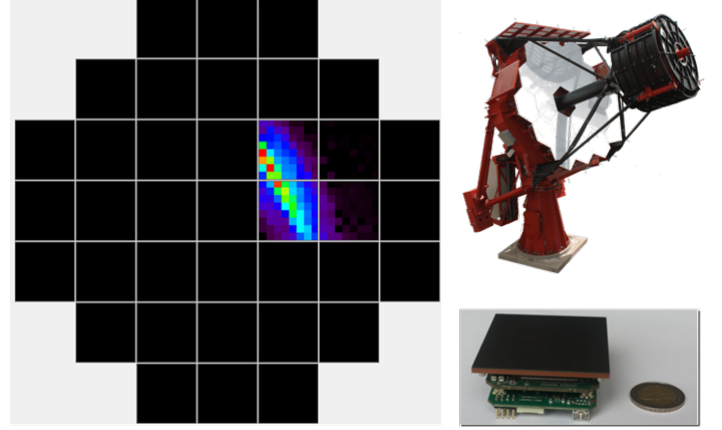


Figure 4: ASTRI telescope prototype for Cerenkov imager equipped with CITIROC ASICs.

3. ASICs for timing: TRIROC and PETIROC

The growing interest for sub-nanosecond measurements combined with the fast response of SiPMs make them ideal sensors for timing detectors. However, for small amounts of light and therefore small signals, the timing accuracy is dominated by the electronics jitter and there is a strong push for getting very high speed readout ASICs.

3.1. General considerations for timing

The timing accuracy of a detector depends on several factors, but is usually dominated by the electronics jitter at small amplitude. The electronics jitter (j) is the translation in the time domain of the electronics noise (N) when crossing the threshold of a discriminator due to the finite signal slope (dV/dt). To first order, the jitter is simply the ratio of the rms noise over the signal slope and is expressed in ns or ps. As the signal slope is proportional to the bandwidth (BW) and the rms noise scales as the square root of the bandwidth, it is often believed that the jitter improves by increasing the bandwidth, the jitter scaling as $1/\sqrt{BW}$.

This is however not really the case for capacitive sensors which produce current pulses, such as SiPMs (as well as many other photodetectors). In that case, the current signal which has a finite duration (t_d FWHM) gets integrated on the sensor capacitance (C_d) for the highest frequency components and the risetime on the preamplifier input is simply t_d . Having a very fast preamplifier only increases the output noise but does not change the output rise time. Conversely, if the preamplifier is too slow, the output risetime is the convolution of the current duration (t_d) and the preamplifier risetime (t_{PA}), which is usually simplified as the quadratic sum of the two time constants. The signal amplitude scales as Q/C_d .

Therefore the jitter can be expressed as:

$$j = \frac{N}{dV/dt} = \frac{e_n}{\sqrt{2}t_{10-90,PA}} \cdot \frac{C_d \sqrt{t_{10-90,PA}^2 + t_d^2}}{Q_{in}} = \frac{e_n C_d}{Q_{in}} \cdot \sqrt{\frac{t_{10-90,PA}^2 + t_d^2}{2t_{10-90,PA}}}, \quad (1)$$

in which e_n is the preamplifier noise spectral density, C_d the detector capacitance, t_d the signal duration (FWHM), t_{10-90_PA} the preamplifier alone rise time (10-90%) and Q the signal charge.

As can be seen in Figure 5, the jitter can be minimized by choosing a preamplifier rise-time t_{PA} equal to the current duration t_d , however the optimum is rather shallow and it has to be balanced with the reduced sensitivity, as the minimum threshold increases when increasing the speed. Indeed, being twice faster increases the minimum threshold by 40%, whereas being twice slower reduces the minimum threshold by 30%, while deteriorating the optimum jitter by only 10%. It is therefore usually preferable to be slightly too slow than too fast.

At the optimum preamp speed, the jitter is simply given by:

$$j = e_n \cdot C_d \sqrt{t_d} / Q.$$

For SiPMs, the jitter benefits from the large charge collected (hundreds of fC per photoelectron) and from the very short current duration (<100 ps). It is however penalized by the large sensor capacitance (in the 100 pF range), especially for large area photosensors. It is thus expected to obtain the best timing resolution for the smallest devices and measurements in Figure 8 show that this is indeed the case.

As an example, for a 300 pF SiPM with a gain of 10^6 , assuming a good preamplifier with a noise spectral density of $1 \text{ nV} / \sqrt{\text{Hz}}$, a jitter of 20 ps for single photoelectrons could be expected. With a current pulse duration of 100 ps, the optimum preamplifier risetime is equal to 100 ps, which corresponds to a bandwidth of 3.5 GHz.

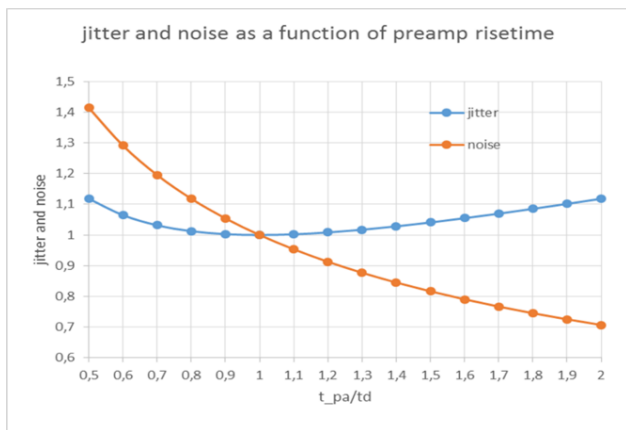


Figure 5: Jitter and noise as a function the ratio of preamplifier rise time over input current duration.

3.2. TRIROC

TRIROC is a 64 channel ASIC designed for tri-modal PET/MRI/EEG brain imaging in the framework of the Trimage European project [7]. Its architecture is similar to PETIROC described below, but with twice the number of channels and a slightly lower speed [8]. For lack of space, the paper will concentrate on PETIROC.

3.3. PETIROC

PETIROC is a 32 channel ASIC which has been optimized to provide 1 GHz bandwidth for timing applications and PET

imaging [9]. The block diagram is shown in Figure 6. It is composed of a high speed voltage sensitive preamplifier coupled directly to a high speed discriminator. The chip takes full advantage of the SiGe technology to achieve high speed and low noise. The input preamplifier impedance is 200Ω for high frequencies and a 50Ω impedance can be obtained by adding a 68Ω resistor outside if needed. An 8-bit DAC allows to adjust the input voltage channel-wise over 1 V span, in order to compensate the dispersion in overvoltage in SiPM matrixes. The discriminator outputs can be used directly to drive an external TDC which allows to reach the lowest time resolutions and highest rates. An internal TDC is also available for lower rate applications, providing a time resolution around 50 ps.

A slower channel also provides charge information for the energy measurement in PET applications. Otherwise time-over (threshold technique (TOT) can be used for timewalk correction on smaller signals.

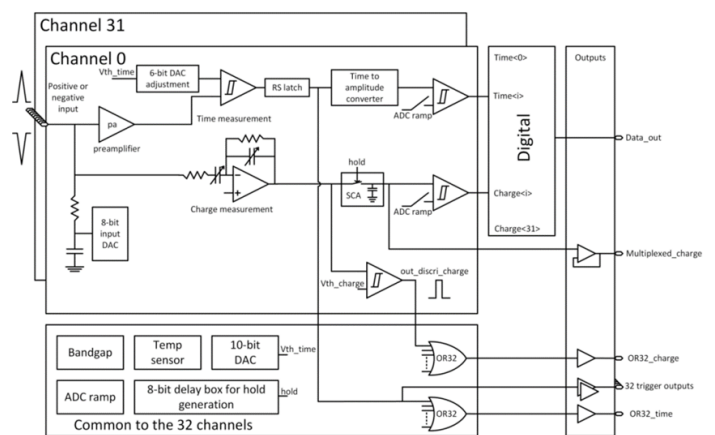


Figure 6: Bloc diagram of the PETIROC ASIC.

The ASIC speed is in good agreement with expectations, with a measured bandwidth of 0.9 GHz for the full chain, from input to discriminator output. The noise is also very low, allowing to set a minimum threshold at 1 mV on the input, as shown in Figure 7, corresponding to 100 fC on 100 pF. The best jitter performance, down to 15 ps, is obtained with external TDC as the digital noise from the internal TDCs increase the jitter to 45 ps.

The performance for single photoelectrons jitter with various SiPM is shown in Figure 8, where values down to 90 ps FWHM, corresponding to 40 ps rms are achieved.

4. Conclusions

The use of high performance ASICs has been a key element for getting the best performance of SiPMs and has allowed their successful use in large detectors. OMEGA and WEEROC have developed several multi-channels chips such as SPIROC, CITIROC, TRIROC or PETIROC which allow to get compact performant photodetectors used in several large experiments.

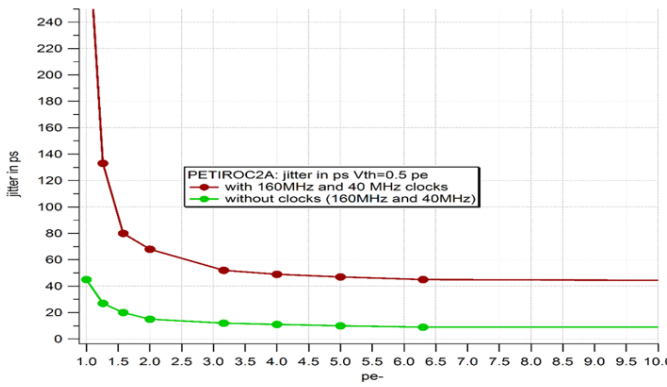


Figure 7: Jitter as a function of signal amplitude measured with PETIROC ASIC.

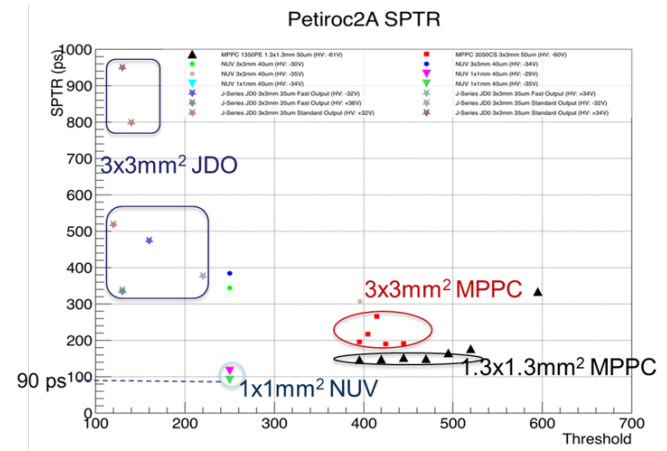


Figure 8: Single photon time resolution (SPTR) measured with PETIROC on various SiPMs.

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174 The help of WEEROC and CAEN companies is gratefully
175 acknowledged.

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