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To cite this version:

Amirouche Oumaziz, Emmanuel Sarraute, Frédéric Richardeau, Abdelhakim Bourennane. Fail-safe switching-cells architectures based on monolithic on-chip fuse. 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe), Sep 2020, Lyon, France. pp.P.1-P.10, 10.23919/EPE20ECCEEurope43536.2020.9215608 . hal-02980784

HAL Id: hal-02980784

https://hal.science/hal-02980784v1

Submitted on 27 Oct 2020

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Fail-safe switching-cells architectures based on monolithic on-chip fuse

Amirouche Oumaziz
LAAS-CNRS & LAPLACE
2 rue Camichel, 31500
Toulouse, France
a.oumaziz@laplace.univ-tlse3.fr

Emmanuel Sarraute
LAPLACE
2 rue Camichel, 31500
Toulouse, France
e.sarraute@laplace.univ-tlse3.fr

Frédéric Richardeau
LAPLACE
2 rue Camichel, 31500
Toulouse, France
f.richardeau@laplace.univ-tlse3.fr

Abdelhakim Bourennane
LAAS-CNRS
7 ave colonel Roche 31400
Toulouse, France
a.bourennane@laas.fr

Keywords

«On-chip fuse», «Power Converters», «fuse design», «electro-thermal behavior», «3D finite elements method».

Abstract

In this work, we propose a new concept of fail-safe switching cells based on the use of integrated fuses. These fuses allow the circuit to be partially isolated and reconfigured, which therefore becomes fault tolerant and prevents total shut down. We focused our work on the design and 3D simulation by finite elements method of monolithic fuses integrated on silicon substrate, taking into account static and dynamic specifications. Thermal management in steady state is improved by dielectric epoxy thermal insulation under each constriction of the fuse. Implementation and preliminary practical tests at medium voltage are reported. The effect of a coating using silicone gel around the fuses is analyzed to improve the cut-off capability.

Introduction

Nowadays, especially for applications related to electric mobility, it is very important to improve the availability of electronic power devices in order to guarantee fault tolerance and continuity of service. For this, we worked on a new concept of switching cell associated with fuses integrated on silicon substrate. This association makes it possible to electrically isolate a damaged cell and to reconfigure the power circuit to ensure continuity of service. In this article, we focused our work on the design and 3D simulation by finite elements method of monolithic fuses integrated on silicon substrate. The dimensioning must take into account both the electrical and thermal specifications in steady state and in cut-off case. For this, we studied several series or parallel fuses constrictions configurations and compared their compactness. A first series of fuses was manufactured and tested in medium voltage. The results are compared with commercial SMD fuses.

Fail-safe topologies using single-fuse or dual-fuse function

With the growing of the power electronic converters, power semiconductors need more preventive protections from damages. Passive protection as fuses can be used due to their high integration, low cost and reliability capability. But, these ones should be optimized and integrated on-chip or in-package to reduce size. In this paper we describe main fail-safe half-bridge topologies with single-fuse or dual-fuse function and possible auxiliary switch.

The first and simple single-fuse circuit is presented in Figure 1.a. A half-bridge is connected to the DC source through a fuse. A thyristor, connected in parallel with the half bridge, is used to blow up the fuse [1]. In a converter, this first configuration secures the DC source only in case of short-circuit default, with all inverter-legs being separated from the DC bus without redundancy capability.

The second configuration is given in Figure 1.b. It considers a serial fuse with each half-bridge, that offers a selectivity property in fault case. This configuration avoids the isolation of the whole

converter and thus enabling a post-fault reconfiguration based on N-1 half-bridges. However, in this configuration, the output of the faulty half-bridge is not isolated giving a malfunctioning for active load.

A well-known configuration is shown in Figure 1.c, using gate-drive embedded electronic protections. The fuse is connected between the leg's midpoint and the load. An auxiliary switch is used to provide the load disconnection from the faulty half-bridge and its re-connection to the DC midpoint. This topology enables an interesting post-fault continuation through the DC midpoint tap as in inverter operation. However, the switch must support the switching dv/dt at the cell output.

Figure 1.d offers same properties as Figure 1.c using a high side / low-side dual-fuse without gate-driver electronic protection. Although, the fuses should be well designed and blow up quasi simultaneously, thus with a low mismatch of I²Tp clear feature. In this case also, the switch must support the switching dv/dt at the cell output.

The configuration in Figure 1.e uses a parallel switch and two fuses in high side and low side to disconnect DC source and load from the faulted half-bridge. The switch is used to blow up the fuses regardless of the transistors failure mode. But there is no post-fault current path from the DC source and the load. Consequently, in Figures 1.f and g, a dual-diode coupler is introduced [2] [3] which can be used to take over the current path once the thyristor is triggered.

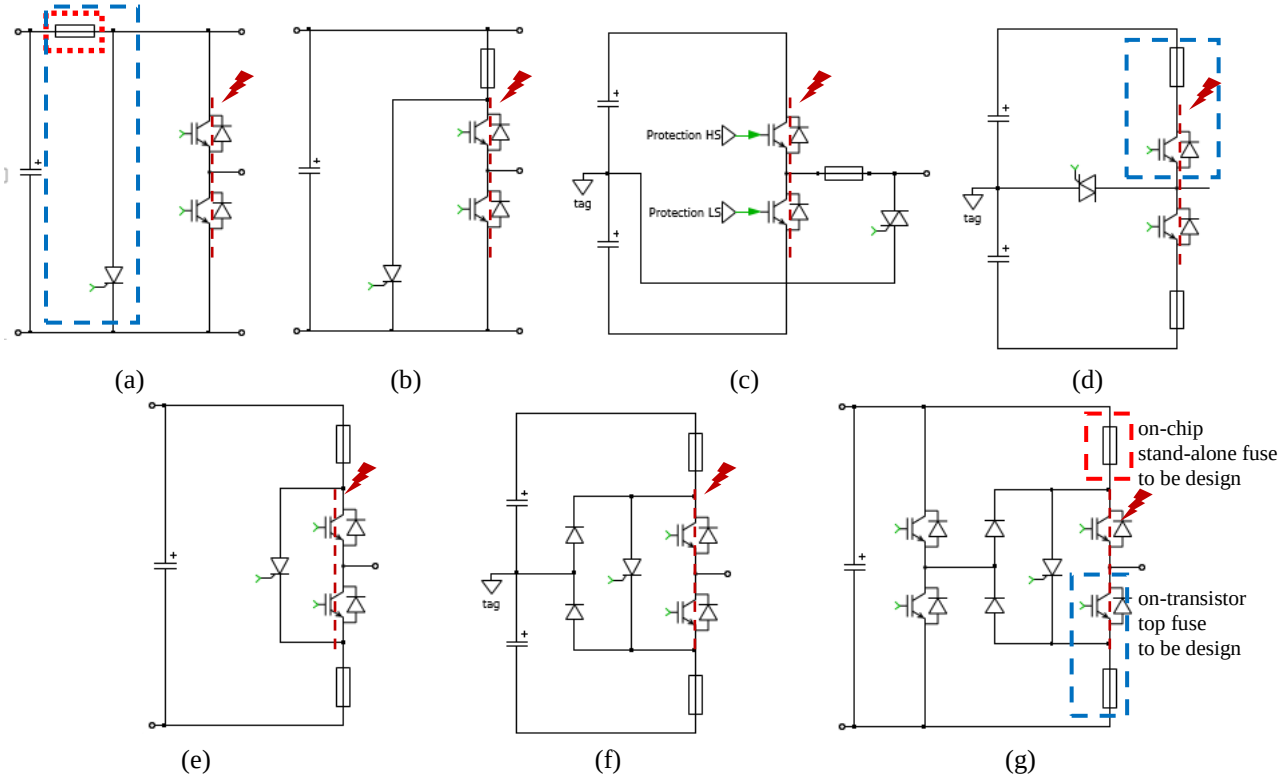
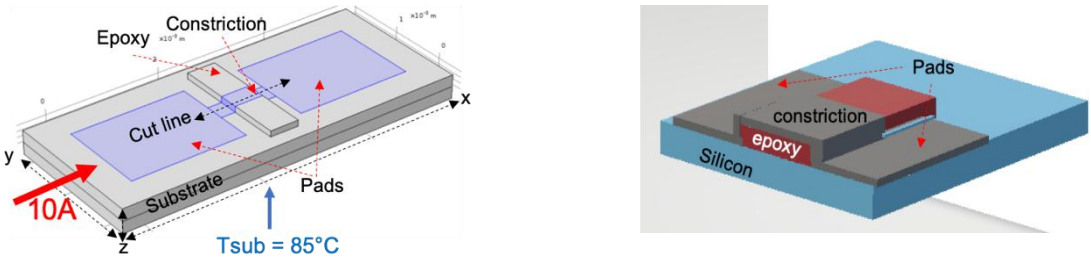


Figure 1 : Fail-safe capabilities and new safety functions to be designed.

The last and enhanced configuration considers replacing the DC midpoint by a back-up half-bridge (Figure 1.g) which allows converter's post-fault reconfiguration at full power [4]. The monolithic combination of an on-transistor top fuse on RC-IGBTs (Figure 1.g, blue dashed box) would be very promising, auto-secured IGBTs can be provided, which will increase their applications. In this paper, we will focus only on the on-chip stand-alone fuse (Figure 1.g red dashed box) integration on silicon substrate. Fuses design and optimization will be discussed below.

Characteristic of the targeted monolithic fuses

Fuses are simple, passive and inexpensive components, capable if they are well designed to protect electrical devices in the event of short circuits. Usually, to protect semiconductor components, fuses are made from thick or thin metal films (copper or aluminum) on Direct Bond Copper (DBC) or printed circuit board (PCB) substrates [4] [5] [6]. The ones we have designed consist of a thin (18µm) film of copper deposited on a massive 400µm silicon substrate. Fuses are composed of one or more reduced width tracks, called constrictions, arranged in series (Ns constrictions) or in parallel (Np constrictions). Each fuse is designed to withstand the rated current in steady state and to melt (open) in case of short circuit current (defined by I^2T effect). When the metal constituting the constriction evaporates under the effect of the heat produced by a current peak, the remaining open area must be sufficiently long (1mm here) to support the supply voltage (up to 400 Vdc). The evaporation must be irreversible, thus minimizing the presence of metal particles on the surface of the substrate, in order to avoid re-arcing phenomena. A fuse's design example and a structure's cut line are disposed Figure 2 below.



(a) (b)

Figure 2 : Example of an on-chip fuse design (a) and a cross section (b).

The proposed designs are studied using "Comsol Multiphysics™" simulations. The fuses have been designed for a 10A nominal current at 85°C substrate's maximum temperature and 115°C maximum constriction's authorized temperature. Thin film Nitride layer was added below the copper layer in order to passivate it and avoid leakages currents after the constriction's copper blows.

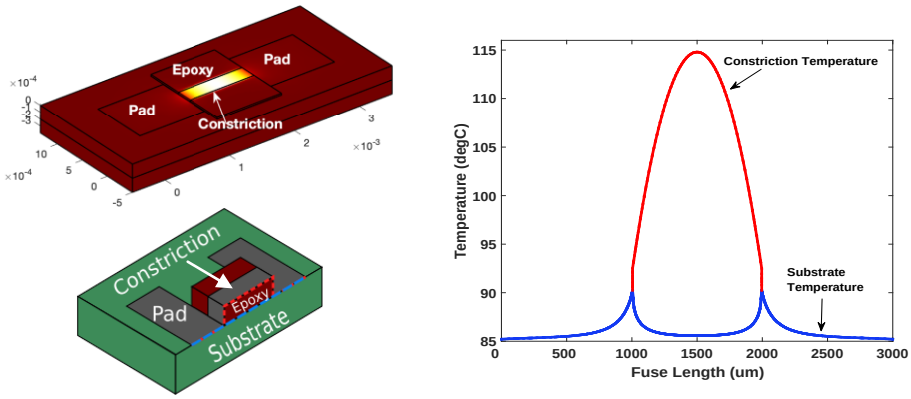
The epoxy, with its low thermal conductivity insulates the constriction from the substrate (higher thermal conductivity) which allows to focus and keep the energy on its center (hot point).
When the thermal conductivity decreases, the temperature increases. The aim is to focus the energy on the constriction's center to ensure an optimum metal evaporation in the case a fault occurs. For this reason, theoretically, a fuse constriction's temperature profile should look like a Dirac's function, which enhances the melting operation and makes it as quick as possible.

Comsol™ "AC/DC" and "Heat Transfer" modules have been used to analyze heat transfer throughout the fuse structures.

Design using 3D Comsol simulations

In fault case, short-circuit current can causes the fuse to blow. For this reason, a 1 mm length between the metallic pads is chosen to prevent the silicon substrate from any breakdown caused by the voltage across fuse once the constriction melts (from the previous experimentation [4]). The length and thickness of the constriction being fixed, the fuses are designed according to their let through current and the constriction's allowed maximum temperature by setting its width to fit those parameters. Figure 3 shows the first fuse's design (Ns=Np=1), a 2D view according to the cut-line and results of the constriction and longitudinal substrate temperatures distribution. The fuse's design shown above (Figure 3.a) is composed of only one constriction and will be considered the reference design for other designs comparisons. A preliminary theoretical calculation from the Fourier's law, allowed us to set up the initial constriction's width value at 240 µm. As expected, its maximum temperature is situated at the constriction's center (Figure 3.b). Furthermore, the optimized epoxy's thickness (25 µm) ensures thermal decoupling between the constriction and the silicon substrate. The estimated power

loss through the constriction is about 394 mW, which is the average losses in substrate fuses at this rated current.



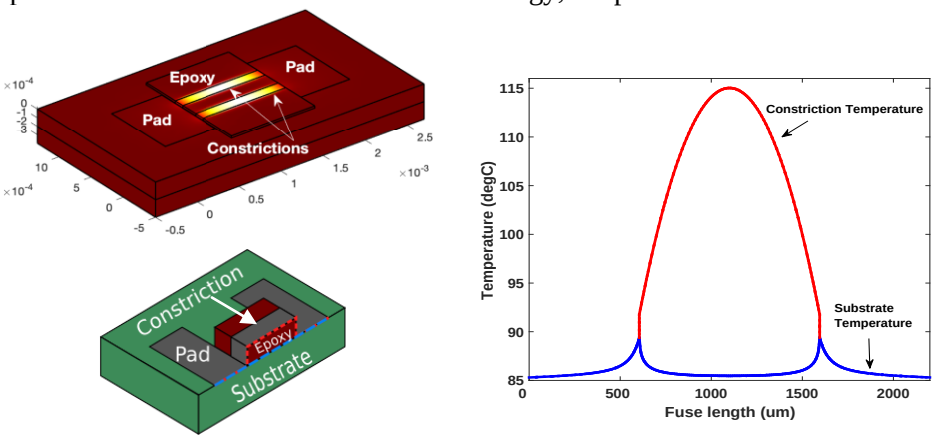
(a) (b)

Figure 3 : 10A fuse design with one constriction (a), substrate (blue) and constriction (red) temperatures (b) for: 1.61 A^2.s clearing time, 1 x 0.42 mm² constriction, 2(1 x 0.84) mm² pads and 3 x 0.84 mm² silicone substrate.

In order to minimize the fuse's chip area, we added a parallel constriction (Ns=1 Np=2) to the first model. As a consequence, we have improved the pads power dissipation due to an improved heat distribution. To fit the specification of 115°C constriction's maximum temperature at the rated current, a 117µm constriction's width was required. The result of the improved fuse's design is shown in Figure 4. The spacing between the two parallel constrictions is chosen so the temperature distribution is close enough to substrate's temperature (85 °C) to avoid thermal coupling.

This improved configuration (Figure 4.a) afforded a gain of 37 % as compared to the reference fuse design (Figure 3) described above with approximatively the same power losses (404 mW). The substrate and constrictions temperature profiles (Figure 4.b) are the same as those of the reference design.

The improvement in the occupied is noticeable, but in order to enhance the thermal behavior with thin temperature profiles in order to concentrate the heat energy, we put in series the constrictions.

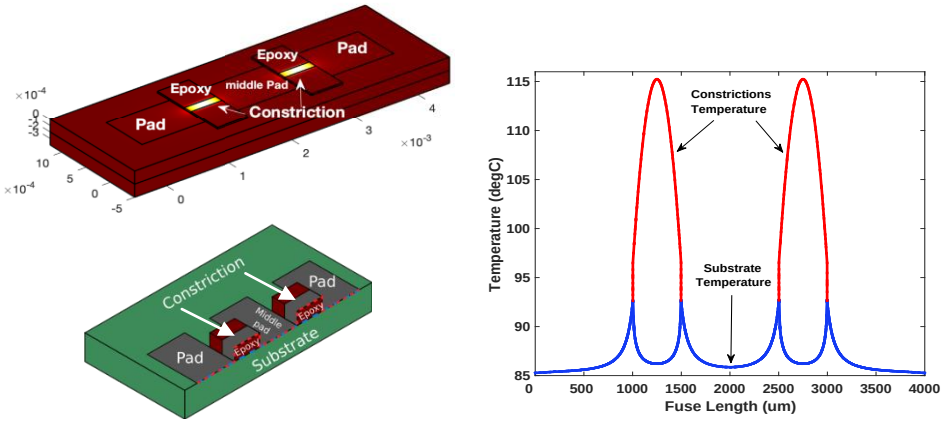


(a) (b)

Figure 4 : 10A fuse design with two parallel constrictions (a), substrate (blue) and constrictions (red) temperatures (b), for: 0.59 A^2.s clearing time, 1 x 0.117 mm² constriction, 2(0.834 x 0.6) mm² pads and 2.2 x 0.6 mm² silicone substrate.

A serial constriction is added to the reference design (Ns=Np=1) to build up a two serial constrictions fuse (Ns=2 Np=1), as shown in Figure 5.a. Thanks to this new configuration, the constriction's length (1 mm before) is split into two equal constrictions of 500 µm. This model comprises a middle pad separation between the two constrictions to avoid thermal coupling and thus insulate thermally the two

constrictions. The length of the middle pad is chosen so its local temperature is close enough to substrate's temperature (85 °C). The simulation results of the serialization are shown in Figure 5.b.

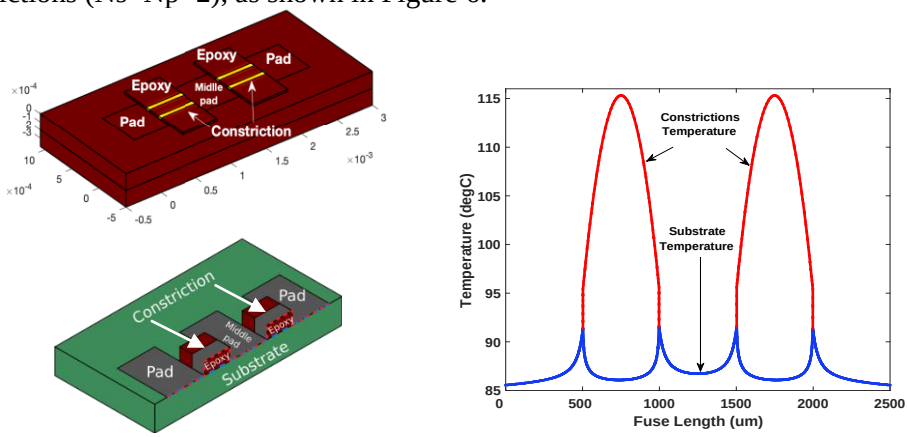


(a) (b)

Figure 5 : 10A fuse design with two serial constrictions (a), substrate (blue) and constrictions (red) temperatures (b), for: 0.41 A^2.s clearing time, 0.5 x 0.138 mm² constriction, 3(1 x 0.738) mm² pads and 4 x 0.738 mm² silicone substrate.

Figure 5.b shows a dissociate constrictions temperatures profile thanks to the middle pad. On the other hand, this configuration increases fuse's occupied surface, the estimated loss is about 15 % compared to the reference model. Only 138 µm constriction's width is required to reach the constriction's maximum temperature specification with power losses estimated to 684 mW.

The last configuration combines the advantages of parallelization and serialization in a structure made of four constrictions (Ns=Np=2), as shown in Figure 6.



(a) (b)

Figure 6 : 10A fuse design with four parallel/serial constrictions (a), substrate (blue) and constrictions (red) temperatures (b), for: A^2.s 0.5 x 0.067 mm² constriction, 3(0.5 x 0.584) mm² pads and 2.5 x 0.584 mm² silicone substrate.

Parallelizing and serializing give noticeable improvement on the fuses area. Indeed, the estimated gain is about 73 % as compared to the reference design (Ns=Np=1). Only 67 µm constriction's width was required to reach the maximum allowed temperature of 115 °C. This configuration shows an estimated power loss about 705 mW, which is still in the average as compared to the commercially available substrate fuses. A review of the compared commercially available substrate fuses at 10A rated current is reported in the Table 1 in comparative with our designed silicon substrate fuses. The fuses are sorted according to their rated voltages, melting integral, occupied area, resistance and power loss. Most of the compared fuses are rated for very low voltages (<125 V), with areas more important than our designed "Stand-alone fuses". Also, the required nominal melting energy I^2T for the compared fuses are higher than our designed fuses (2.3 to 2.8 A^2.s).

Table 1: Comparative review between our "Stand-alone" designed fuses and commercially available substrate fuses

Part Designation	Rated Voltage (V)	I^2T ($A^2.s$)	Area (mm^2)	R(mΩ)	Power loss (mW)
AEM (F1206HC10A0TM)	35	15	3.2 x 1.6	5.5	550*
BEL (0685P9100-01)	50	28	3.2 x 1.6	5.2	520*
KOA SPEER (CCF1N10)	60	27.7	6 x 2.5	7.5	750*
BUSSMANN (1025FA10-R)	60	457	10.3 x 2.7	7.2	720*
TE conn.2410SFV10.0FM/125-2	125	29.2	6.86 x 3.15	6.6	660*
Littelfuse (R451 010)	125	26.46	6.1 x 2.7	5.6	560*
Littelfuse (Nano 451/453 Series)	125	26.46	6.1 x 2.7	5.6	560*
Designed Stand-alone fuses	130	2.3 to 2.8	3 x 0.84	6.7	750

(*) Calculated from datasheets, using the given resistance at 10 % of the rated current (10A).

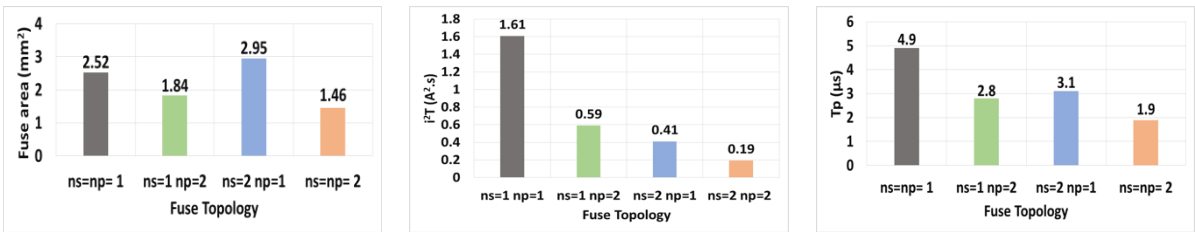
In the case of fault occurrence, the current increases ($I_{cc}(t) = \left[\frac{di}{dt}\right] t$) to reach the maximum value $I_{cc\,max}$ that results fuse melting. Given the expression of the I^2T_p quantity in relation (2) and the current curve expression ($I_{cc}(t) = \left[\frac{di}{dt}\right] t$), we obtain the expression (3) of the pre-arcing delay time Tp:

$$I^2T_p = \int_0^{Tp} I_{cc}^2(t)dt \qquad (2) \qquad\qquad T_p = \left(\frac{3[I^2T_p]}{\left[\frac{di}{dt}\right]^2}\right)^{1/3} \qquad (3)$$

Where I_{cc} represents the maximal default current through the fuse element defined by the relation (4).

$$I_{cc\,max} = \left(3\frac{di}{dt}[I^2T_p]\right)^{\frac{1}{3}} \qquad (4)$$

We noticed that designs improvements made very fast fuses. Figure 7 shows the fuses surfaces, the pre-arcing time (Tp) and the quantity I^2Tp for each fuse topology.



(a) (b) (c)

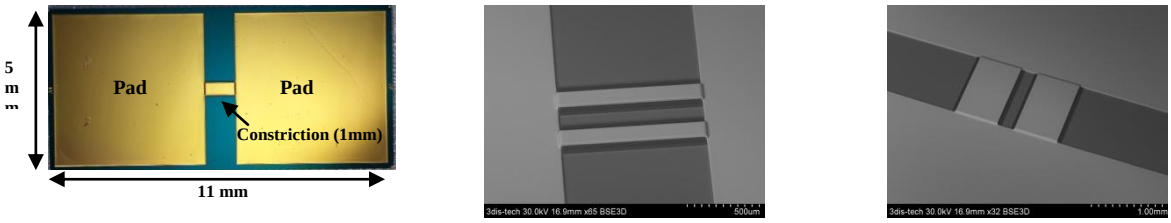
Figure 7 : 10A fuses surfaces (a), I^2Tp (b) and Tp (c) versus fuses topologies @ $I_{Nominal}$=10A, fuse's maximum temperature = 115 °C, substrate's maximum temperature = 85 °C, copper's thickness = 18 µm and epoxy's thickness = 25 µm.

Both parallelization and serialization made very fast fuses (2.8 and 3.1 µs at 1420 A and 630 A respectively) with lower I^2Tp (0.59 and 0.41 $A^2.s$ respectively) melting energy requirement compared to the reference design. The serial configuration presents more occupied area, because of the middle separation pad. The highest improvement is achieved when both parallelization and serialization are combined simultaneously. The last design shows improvements in both occupied are and energy breakup requirements I^2Tp (0.19 $A^2.s$) with mainly low pre-arcing time (1.9 µs at 770 A).

Fuses realization

After the design step, simulation and size optimization, on-chip fuses have been realized by 3DiS™ [7] using facilities of the micro and nanotechnology platform of LAAS-CNRS laboratory. The pads are oversized (5x5 mm^2) in order to ease the measurements and experiments. A mono-constriction fuse picture and a microscopic view of some parallel fuse constrictions are shown in Figure 8.

Two wafers were realized, the second one showed better resolution thanks to a well-managed clean room process.

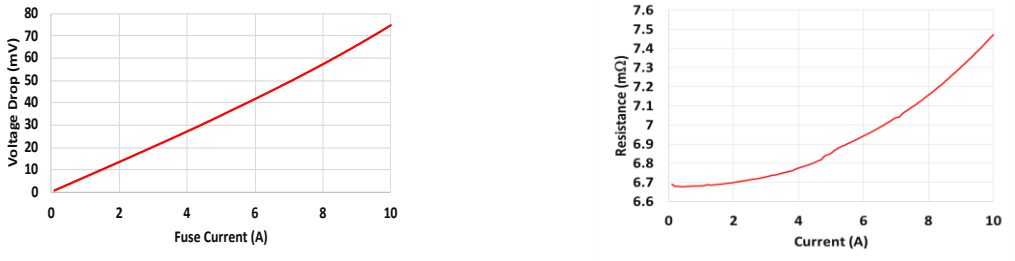


(a) (b) (c)

Figure 8: microphotography of the realized 10A/150V mono-constriction fuse (a) and a microscopic view of some parallel fuses constrictions (b and c).

Experimental characterization results

The characterization process and experimental tests were realized at Laplace laboratory. Only mono-constriction fuses were investigated at ambient initial temperature. A four wires method was used to characterize each fuse. Fuses voltage drop and their resistance versus current are shown in Figure 9.

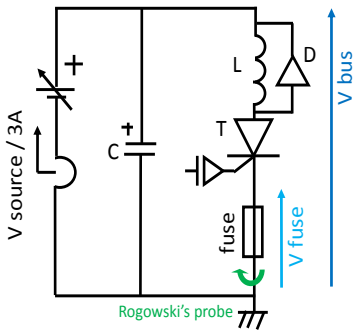


(a) (b)

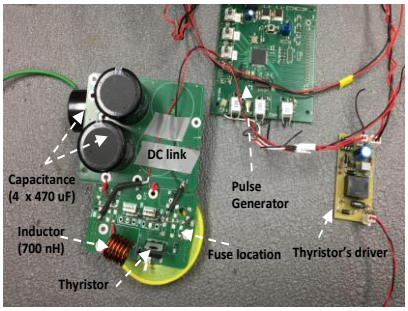
Figure 9 : Fuse's drop voltage (a, c) and constriction's resistance (b, d) versus current.

The measured voltage drop involves a part of the pads resistance due to the contacts placements. In addition, a voltage drop of 75 mV at 10 A is an acceptable average value (theoretically, we have estimated 65 mV on Comsol ™).

The experimental test circuit (Figure 10) is mostly composed of a current-limited voltage source, four parallel capacitors which makes a total capacitance of 1880 µF. In order to limit the energy and to avoid the failure of the thyristor, a 700 nH inductance was added. The fuses were fired by triggering a serial thyristor, the stored energy is sufficiently high to achieve a fuse blow. Figure 10 shows a schematic representation of the experimental test circuit and a picture of the experimental bench. A freewheeling diode is included in parallel with the inductance as in real switching cell.



Capacitor (C)	4 x 470 uF
Inductor (L)	700 nH
Diode (D)	BYT30Pi1000
Thyristor (T)	IXYS CS45-16io1



(a) (b)

Figure 10 : electrical schematic of the fuse's test circuit (a) and a picture of the experimental bench (b)

Results and discussion

When the thyristor is triggered, all the capacitors stored energy is partially discharged through the fuse, which increases its voltage and current until the required constriction's melting point energy is

reached, resulting in its interruption. Finally, the initiated arc persists until the current reaches zero. This current cancellation must remain indefinitely and mustn't restrikes. The first fuses interruption process studies were carried out on non-passivated mono-constriction fuses in order to study the electrical behavior. The results of the interruption tests on two fuses, obtained for 50 V with a current limitation to 3 A, microphotographs of the interrupted constrictions and the measured leakage current are presented in Figure 11 below.

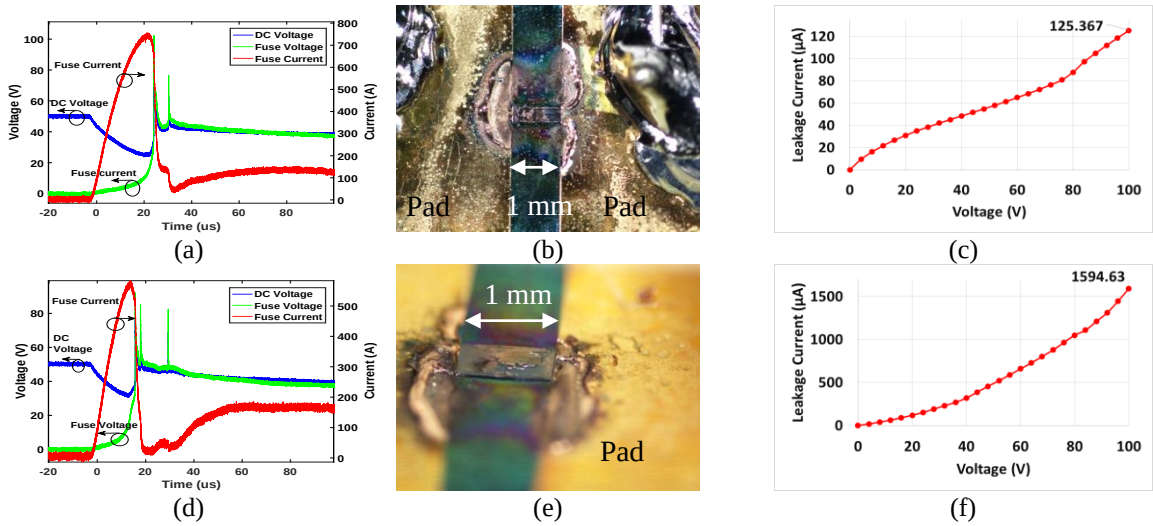


Figure 11 : results of the interruption tests from mono-constriction fuses at 50 V (a) and (d), microphotography of the interrupted constriction (b) and (e), the measured leakage current (c) and (f).

The tests are conducted using the experimental circuit described in Figure 10, DC-bus and fuse voltages are measured using oscilloscope probes and a Rogowski's probe was used for the current. Unfortunately, the results (Figure 11.a, Figure 11.d) showed current restrike during the arcing period. As a result, both pads adjacent to the constriction were damaged. We explain that by an excess of energy and without any top fuse passivation, it spreads over the pads.

In order to achieve a satisfactory and controlled interruption without any pads damages, we decided to passivate the fuses by adding silicone gel taken from a used power module. The results of the interruption tests on two fuses, obtained for 100 V and 130 V with a current limitation to 3 A, as well as a microphotography of the interrupted constrictions and the measured leakage current are presented in Figure 12 below.

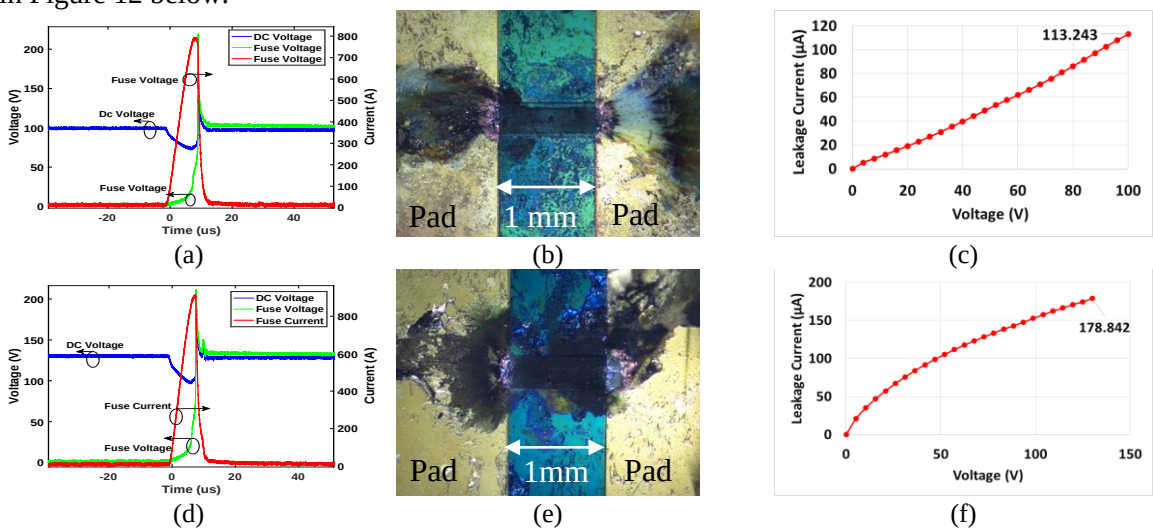


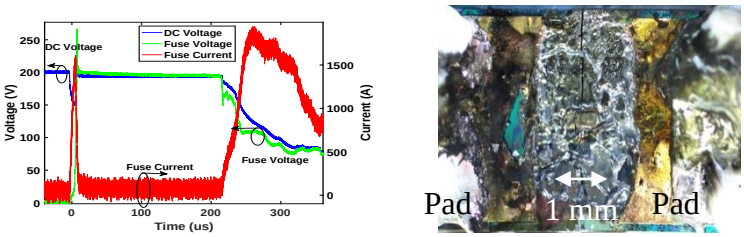
Figure 12: results of the interruption tests obtained with mono-constriction fuses at 100 V (a) and 130 V (d), microphotography of the interrupted constriction (b) and (e), the measured leakage current (c) and (f).

In this case, after pre-arcing periods of 8.5 µs and 8 µs (respectively at 100 V and 130 V) the arcing periods ended with a current cancellation for both tests, satisfactory clearance was achieved (Figure 12.a and Figure 12.d). The interruption was controlled, no important damages were observed on the pads, the constriction vaporized entirely (Figure 12.b and Figure 12.e). The measured leakage currents showed small values (Figure 12.c and Figure 12.f), with 120 µA and 180 µA (respectively at 100 V and 130 V).

Calculated versus measured I^2Tp

The required melting energy to induce the fuse blow are comprised between 2.3 and 2.8 A^2.s, against 1.61 A^2.s theoretically, which represents a difference of 30 to 42 %. This may be due to the processing program using trapezoidal method which may lead to some irregularities.

Since the passivation process improved the fuses reliability in achieving satisfactory interruption, we decided to increase the voltage test to 200 V. Unfortunately, the used passivating gel wasn't suited to sustain higher breaking voltages. The results of the interruption test are presented in Figure 13.



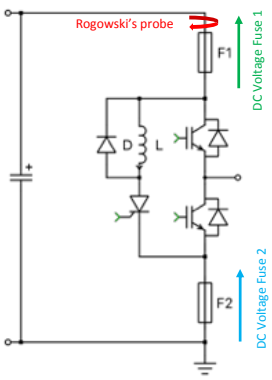
(a) (b)

Figure 13 : results of the interruption test obtained with mono-constriction fuse at 200 V (a) and microphotography of the interrupted constrictions (b).

The interruption process ended by current restrike, this is related to an unsuited passivating material and due to that, the arc couldn't be contained by only the silicone gel, so the pads absorbed this energy which caused their damage.

Dual-fuse leg

In order to exploit the fuses on a fault-tolerant inverter leg topology, we first did an experiment on a dual mono-constriction fuses leg under a DC link of 160V/3A using the same experimental bench described in Figure 10, including a second fuse. The equivalent electrical circuit is presented Figure 14.



Capacitor (C)	4 x 470 uF
Inductor (L)	700 nH
Diode (D)	BYT30Pi1000
Thyristor (T)	IXYS CS45-16io1

Figure 14 : The dual fuse electrical circuit

A Rogowski's probe (30 kA caliber, 0.2mV/A) is used to measure the electrical current through the fuses and high voltage differential probes (Tektronix, TMDPO200) are used to measure separately the dc voltage across the fuses. A Keysight oscilloscope (DPO4034B) is connected to all the probes and display all the measured values.
The shaded area is not experimented yet and will be the subject of another work. The same electrical configuration will be tested by causing a default in the inverter leg IGBTs and observe how the fault will be isolated and avoid its propagation.

The experimental results are presented in Figure 15. From Figure 15.a and 15.d we can observe a perfect current quenching after a pre-arcing time of 10 µs, although the fuses voltages are unbalanced for the recorded interrupting sequence, but the difference still acceptable. This suggest that an experiment using a fault-tolerant inverter leg is possible.

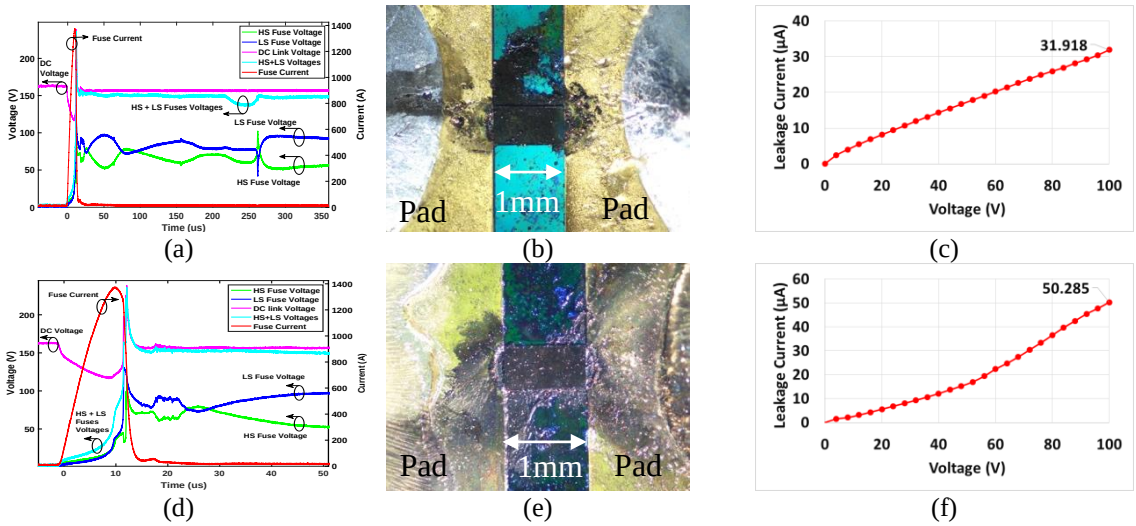


Figure 15 : results of the interruption tests obtained with dual mono-constriction fuses leg at 160 V DC link (a), a zoom on the arcing time (d), microphotography of the interrupted fuses constriction high side (b) and low side (e), the measured leakage current for the high side fuse (c) and the low side fuse (f).

The leakage currents at 100 V are respectively 32 µA and 53 µA for the high side and the low side, which is still low for the tested voltage.

Conclusion

In this work, we have designed, simulated and tested integrated fuses used for new fail-safe power converters. These fuses, manufactured by conventional silicon process, consist of thin copper layer constrictions deposited on a thick isolating epoxy layer. Different series or parallel configurations have been studied to fit both static and dynamic requirements. Samples of fuses were manufactured and tested under medium voltage conditions. Static measurements showed expected results like fuse's resistance and temperature under rated conditions. Successful electric current cut-off tests were achieved on a dedicated test bench. The use of a classical power module silicone gel deposited on fuses constrictions showed very good cut-off results and acceptable leakage currents. These good results suggest that it is now possible to design dedicated integrated fuses which can lead to more compact fault-tolerant inverters. For the future, we will work on better integration and compactness of fuses within power modules and the impact of different passivation gels to improve their cut-off capabilities.

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