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Implementation of Control Strategy for Step-down DC-DC Converter Based on Piezoelectric Resonator

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Keywords

«DC-DC converter», «Power conversion», «Piezoelectric Resonator», «Soft Switching», «Control Strategy».

Abstract

With the growth in demand for miniaturization in power electronics, the current solutions are starting to display their limits in dimensions, power densities and efficiency. To meet the previous demands, the new piezoelectric materials achieving high power densities and efficiency could be the solution to ensuring the requirements. The piezoelectric resonators (PRs) and the piezoelectric transformers (PTs) have been used previously. Unlike the PTs, the use of PRs in power electronics has not been fully explored, and their use has been limited to operating as switched capacitors. However, a new operating principle using PRs based on energy and electrical balance exhibits good performances in steady state. In this paper, our motivation is to investigate in the capability to control a dc-dc converter based on PRs using this operating principle. Indeed, this paper presents the control strategy of a new step-down DC-DC converter based on a piezoelectric resonator (PR), which is used as an energy storage element. The operating principle of the converter is also presented. Moreover, the control algorithm has been implemented in field programmable gate array (FPGA) to regulate the output voltage. The control principle is validated experimentally for input-output voltages 120 - 48 V, and achieving an efficiency up to 94% for large operating power range.

Introduction

In last decades, miniaturization, integration and high power densities became a serious challenge for power electronics designers. Various solutions on power electronics have been proposed for these objectives using magnetic components, switched capacitors and variable capacitors [1-3]. Magnetics components are widely used in power electronics, but their integration on silicon is difficult and the performances become limited by magnetic core at high frequency [1]. Variable capacitor converters can be integrated on silicon but need high chip area, and their efficiency is sensitive to load variations [2-3]. Concerning switched capacitor converters, their operations are limited to specific output/input voltages ratios [4].

To overcome the abovementioned limits of traditional solutions, an alternative storage technique is emerging. It is based on piezoelectric resonators (PRs) or piezoelectric transformers (PTs) which store the transient energy in a mechanical form. Indeed, the piezoelectric components can offer a high quality factor (up to 2000 inducing low losses), and it can operate at high frequency (up to 30 MHz or more

inducing a high power densities). Their integration on silicon is widely achieved and continuously improved [5-6]. In addition, the low profile of piezoelectric components can be interesting for integrated converters in thin devices as smartphones, laptops and other connected things (IoT). In literature, most of the proposed converter topologies use PTs in order to replace the magnetic transformers, but these topologies need an additional inductor to increase their performances [7]. So, suppressing this additional inductor in such converters is the aim of several research works [8-13].

In this paper, we present a new conversion principle and our DC-DC converter-using PRs that operate on energy and electrical charges balancing over a mechanical resonant period of the piezoelectric material. The conversion cycle is composed of six steps, which alternate constant voltage steps (connected PRs to a voltage level), and constant electrical charge ones (isolated PRs). In fact, in steady state, the PR takes energy from the input source equal to the one restituted to the output load plus the one dissipated, maintaining mechanical oscillations of constant amplitude. The energy exchange operates during the constant voltage steps. Therefore, the isolated stages (constant charge operation) allow natural evolving of the PR's voltage up to the next constant voltage level. This enables to operate with zero voltage switching (ZVS), leading to reduce power losses and EMI level [14]. A full design of step down DC-DC converter based on a similar principle is presented in [9-10]. The concept is validated by simulation and experiments with efficiency up to 98.4 % at 160 mW for low voltage conversion [9-10]. Recently, various topologies are presented based on the similar principle [10]. The first results show good performances in terms of power densities and efficiency for low power conversion and expect to be competitive compared with traditional converters.

The main objective of this paper is to introduce a new topology of DC-DC converter dedicated to applications at low output/input voltage ratio and its related control strategy. This paper demonstrates the feasibility of controlling a DC-DC converter based on PR, which operates on a six phases conversion cycle. The aim of this control is to regulate the output voltage, ensuring the soft switching and the energy balancing. The load variation should also be compensated. This paper is organized as follows: in the first part, we present the new topology of the converter and the operating principle. In the second part, we analyze and identify the various parameters aiming to control the energy balance and to regulate the output voltage. Then, we present the regulation mechanism for each control parameter. In the experimental results part, we exhibit our prototype, and the dynamic response for $V_{in} = 120 V$ and $V_{out} = 48 V$ at $P_{out} = 10 W$ is experimentally validated. Moreover, the waveforms in steady state are displayed. Then, we validate the regulation against the load variation. Finally, we conclude about this present and future works.

Topology description

The DC-DC converter is presented in Fig. 1. As shown, the converter is composed of a high quality factor piezoelectric resonator (PR), four diode $D_{\{1,2,3,4\}}$ and two NMOS FET switches S_1 and S_2 . The PR is modeled by a capacitance C_p in parallel with a $L-C-R$ motional branch, the electrical equivalent circuit is displayed in Fig.2a. The material of the PR used in this converter is Lead Zirconate Titanate (PZT), this ceramic offers high quality factor and high coupling factor (see Table I). In inductive region (near the resonant frequency) [9], the motional LCR branch can be modeled by a sinusoidal current source i in series with the resistance R_p (Fig.2b). Because we consider a step-down converter, the input-output voltage gain should not exceed 0.5 ($V_{in} > 2V_{out}$). This topology allows establishing three possible voltages on the PR: $V_{in} - V_{out}$, $-V_{out}$ and $+V_{out}$. During these connections, the PR exchanges energy with the input source and the output load. Moreover, the PR can operate in open-circuit mode. In this mode, no electrical charges are exchanged with the outside and the motional branch's sinusoidal current charges/discharges the parallel capacitance C_p and makes the voltage V_p progressively change, as show in Eq.1. Thanks to this mode, the voltage V_p evolves naturally to the next constant voltage level and permit to switch-on S_1 and S_2 when the voltage across them reaches $0 V$ (soft switching operation), leading to reduced switching losses. Indeed, in steady state, the PR stores electrical energy when connected to $V_{in} - V_{out}$ as an increase of mechanical energy. This mechanical energy is then released as electrical energy when PR is connected to V_{out} or $-V_{out}$ (depending on the sign of current).

$$V_P(t) = -\frac{1}{C_P} \int i(t) \cdot dt \quad (1)$$

$$i(t) = I \cdot \sin(\omega \cdot t) \quad (2)$$

V_P is the PR's voltage, i is the motional branch internal current, I is its amplitude, ω (rad/s) is the pulsation of the conversion period.

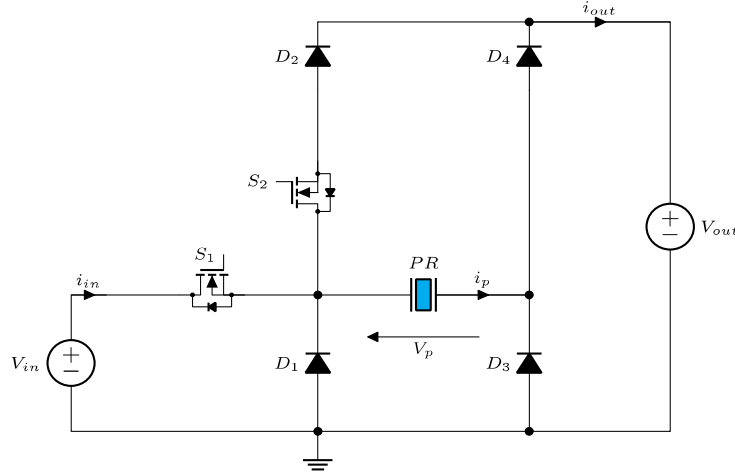


Fig. 1: Converter topology.



Fig. 2: Electrical model for PRs, (a) Circuit model [15], (b) Electrical model in inductive region.

Energy conversion cycle

The conversion cycle is presented in Fig. 3. It is composed of 6 steps, which alternates constant voltage and constant charge. Each stage is represented in Fig.3 with the cycle timeline. We separate step 6 in steps 6.a and 6.b in order to separate the part before and after the sign of the current i changes. The 6th step has for objective to let the piezoelectric voltage V_P goes from V_{out} to $V_{in} - V_{out}$, then as soon as V_P reaches $V_{in} - V_{out}$ the switch S_1 should be closed. However, the Drain-Source voltage of S_1 is not null but equals to V_{out} which induces power losses, since the diode D_3 was in conduction just before. To overcome that limitation and ensure ZVS condition, we let V_P goes up to V_{in} before going back to $V_{in} - V_{out}$ during the stage 6.b with a voltage approaching 0 across D_4 and across S_1 at $t = t_0$.

In Fig. 4, we represent the voltage V_P in function of the transfer electrical charges for a single conversion cycle. In the diagram V_P vs Q , the horizontal displacements correspond to the connected phases since V_P is constant, and the vertical displacements correspond to the isolated phases since no electrical charge is exchanged with the input source or output load. Moreover, for a displacement in positive sense, the transferred electrical charge is positive value, and for displacement in negative sense, the transferred electrical charge is negative. The area under the curve represent the electrical energy exchanged with the PR, as shown in Fig.4. The diagram V_P vs Q allow to more understanding the operating principle. Using the V_P vs Q representation enable to construct any switching sequences by alternating horizontal

displacement and vertical displacement with ensured closed diagram. This representation allow to easily visualizing and understanding the energy and electrical charge transferred.

In steady state, over a full conversion cycle, the energy and electrical charges are balanced, inducing a constant oscillation amplitude. The energy transfer with the PR operates during constant voltage V_p . Therefore, the conservation of energy (CoE) during each cycle is given by Eq.3, while E_{in} is the electrical energy stored when the PR is connected to $V_{in} - V_{out}$. E_{out} is the electrical energy restored to the load, when the PR is connected to $-V_{out}$ and $+V_{out}$. Energy losses due to the PR's resistance are taken into account by Eq.3 and Eq.4.

$$E_{in} + E_{out} + E_{PR_{losses}} = 0 \quad (3)$$

$$E_{PR_{losses}} = -\frac{1}{2}R_p I^2 T \quad (4)$$

T: conversion cycle duration. (All values are algebraic)

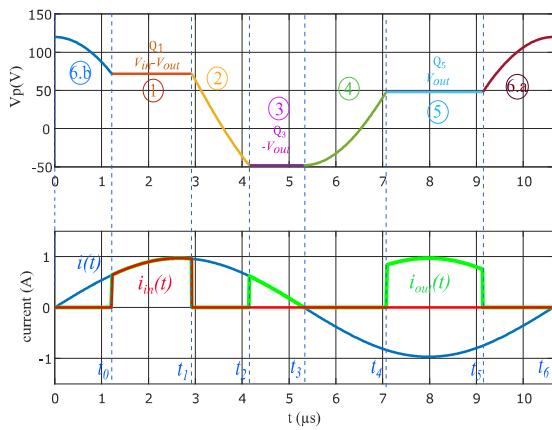


Fig. 3: Waveform of the PR's voltage and currents for 1-6b phases: $V_{in} = 120 V$, $V_{out} = 48 V$ and $P_{out} = 10 W$. (Red: i_{in} , Blue: i , Green: i_{out})

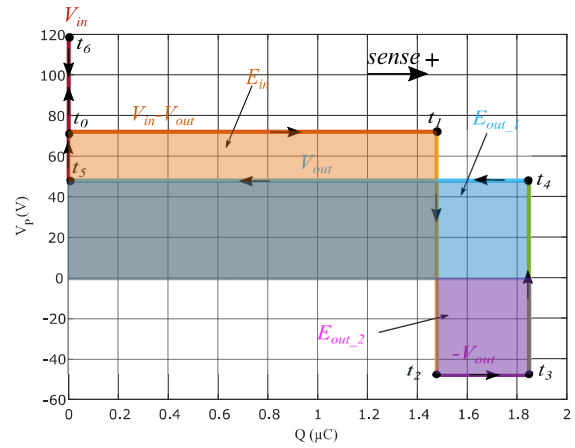


Fig.4: Voltage Vs Electrical charge of PR for 1-6b phases: $V_{in} = 120 V$, $V_{out} = 48 V$ and $P_{out} = 10 W$.

The conservation of electrical charge (CoC) during a cycle of conversion is given by Eq.5:

$$Q_1 + Q_3 + Q_5 = 0 \quad (5)$$

Q_1 , Q_3 and Q_5 are the algebraic electrical charges for stage 1, 3 and 5 respectively.

We can determine each transition time ($t_0, t_1 \dots t_6$) of the cycle by combining the above equations in steady state and considering PR's electrical model, assuming a constant output voltage and operating in soft switching. As shown in Fig. 3, we solved the previous equations for input voltage 120 V, output voltage 48 V and output power 10 W by using the electrical parameters of the PR that are listed in Table 1. Then, we have calculated each transition time for each phase. The electrical parameters of the PR are obtained experimentally by using an impedance analyzer.

Table I: Characteristics of the electrical model of PR. (Part NO: Z0.75T25D-W (C-213). Material is Lead Zirconate Titanate (PZT), the diameter is 25 mm, and thickness is 0.75 mm, the supplier is FUJITSU)

	L	C	R_p	C_p	f_r	Quality factor Q	Coupling factor k
Value	1.1 mH	2.9 nF	0.6 Ω	8.4 nF	89 kHz	1000	52 %

Control strategy of the DC-DC converter

In this section, we propose an analysis of the control strategy in order to regulate the output voltage. As demonstrated in the previous section, in steady state, we should achieve the CoE, CoC and the operating in ZVS conditions to reduce losses. Therefore, the objective of the control is also to regulate the output voltage with high efficiency.

Synchronization with the current i

Since, the PR resonates at variable frequency, which is highly depending on the output power and on the parasitic capacitances of switches [9-10]. The resonance frequency and the phase of the internal current i should be well known in order to synchronize the drive of switches S_1 and S_2 (as shown in Fig.3). In this purpose, we propose to use the state of diode D_3 to detect the 0 crossing of the internal current i and deduce the resonant period duration. Therefore, when current i is positive, diode D_3 is turned-off, and -on when negative. Hereunder, we will consider that the switches driving is synchronized with the internally current thanks to monitoring the state of D_3 .

Zero Voltage Switching

In order to operate in soft switching, we have to detect the zero voltage crossing of switches S_1 and S_2 . For switching-on S_2 , we simply turn it-on at the half period of the conversion cycle (as shown in Fig. 3), when the voltage of the PR equals $-V_{out}$. For switching-on S_1 , we have to regulate t_5 to let voltage V_P reaching the input voltage value V_{in} at the end of the period. Indeed, if t_5 is superior to the optimal value t_{5_opt} (the value to achieve ZVS for S_1 , see in Fig. 3), then voltage V_P will not have time enough to reach V_{in} . Alternatively, if t_5 is inferior to the optimal value t_{5_opt} , the voltage V_P will reach V_{in} before the end of the cycle and the voltage will be clamped by the body diode of S_1 , and a part of energy is restored to the input source that inducing unnecessary losses. Wherefore, a simple comparator can be used to regulate t_5 for the next conversion cycle by comparing the voltage V_{D_1} (left side of V_P) with input voltage V_{in} (see Fig. 5).

Output voltage regulation

As displayed in Fig. 3, the PR takes energy from the input source during step 1; in fact, the instant t_1 controls the amount of energy exchanged. By considering a resistor load R_{Load} in parallel with a capacitor C_{out} that filter the output voltage, we can deduce a relation between t_1 and V_{out} . Equation 6 gives the relation between t_1 and V_{out} .

$$\cos(\omega * t_1) = 1 - 4 \frac{V_{out}}{V_{in}} + V_{out} \frac{C_P \omega}{I} \left(1 + 2 \frac{V_{out}}{V_{in}} \right) - \pi \frac{R_P I}{V_{in}} \quad (6)$$

ω (rad/s) is the resonant pulsation of the PR, which is synchronized the switches driving. V_{in} is the input voltage and considered constant ($V_{in} = 120$ V), I is the amplitude of the internal current i that is also considered constant. So, only t_1 and V_{out} are variables. By using small signals modeling, we can deduce a gain expression between t_1 and V_{out} . Then, a proportional-integral (PI) controller can be designed to regulate the output voltage by adjusting the instant t_1 .

For ease of understanding, we have represented the control strategy in the block diagram depicted in Fig.5. Thus, to implement the control, we need a comparator for current sign detection to monitor the state of D_3 in order to synchronize the switching sequence with the current waveform. A second comparator compare V_{D_1} with V_{in} at the end of period to ensure ZVS operation on S_1 . For output voltage regulation, the difference between the measured V_{out} and the reference is multiplied by a PI controller to calculate t_1 . As shown Fig. 5, the switches S_1 is turned on at $t=t_0$ with ZVS. Then, V_P decrease from V_{in} to $V_{in} - V_{out}$. Ones $V_P = V_{in} - V_{out}$, the diode D_4 is turned on, and PR takes energy from input source until to turn off S_1 at $t=t_1$ in order to regulate V_{out} . During $[t_1, t_2]$, V_P decrease from $V_{in} - V_{out}$ to $-V_{out}$. When $V_P = -V_{out}$, the diodes D_1 and D_4 are turned on naturally, and part of the stored energy in PR is transferred the output load until the current i becomes negative. When $t=t_3$, the switches S_2 is turned on, and the voltage V_P goes from $-V_{out}$ to V_{out} . Ones $V_P = V_{out}$, the diode D_2 and D_3 are turned on, and the second part of the stored energy in PR is restored to output load. This phase ends by turning off S_2 at $t=t_5$ in order to let the voltage V_P evolve to reach V_{in} at the end of period.

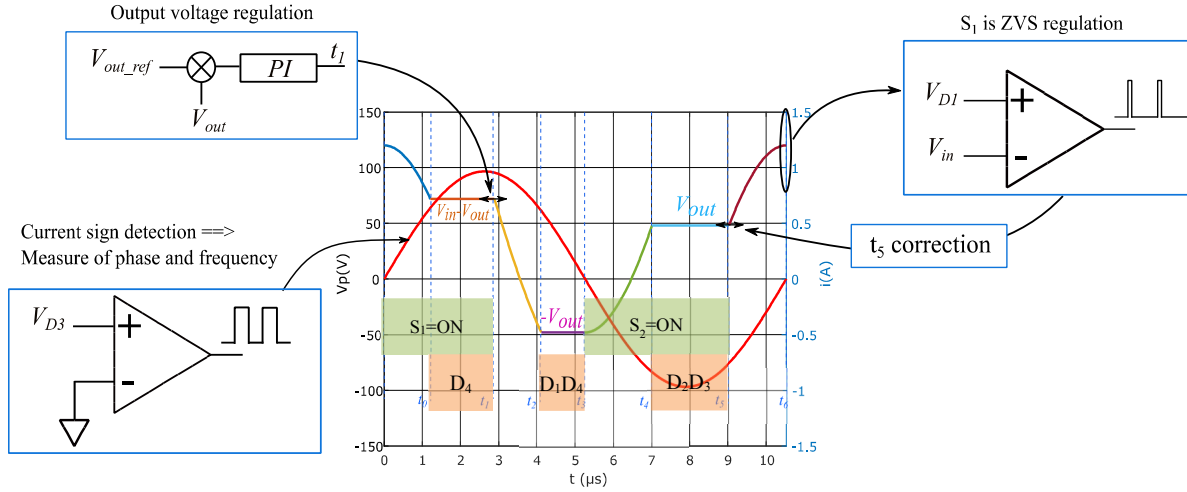


Fig. 5: Control diagram of the circuit.

Experimental Results

Setup

An actual power converter circuit is designed in the aim to test the proposed control strategy. Components references used in the prototype are listed in Table II. Figure 6 shows the prototype that is composed of two PCB circuits; power circuits and FPGA board. The control strategy is modeled in VHDL language and implemented in a FPGA SPARTAN 3 (XC3S200) design kit. The 230Ω load resistance is calculated for $48 \text{ V} / 10 \text{ W}$ output voltage and power. The output capacitor is chosen to reduce high frequency ripple of V_{out} , the value of C_{out} is $10 \mu\text{F}$. The output voltage is sensed by a voltage divider and then digitalized with an analog digital converter (ADC) AMC1204. The difference between the voltage reference and the measured output voltage enables to calculate the time duration t_1 by using a PI regulator, which is digitalized and implemented in the FPGA on state-machine. The FPGA receives measurements from the power circuit, and then calculates the variables t_1, t_5 and f . Once these variables are calculated the FPGA generates the width modulated pulse (PWM) synchronized with the internal PR current phase.

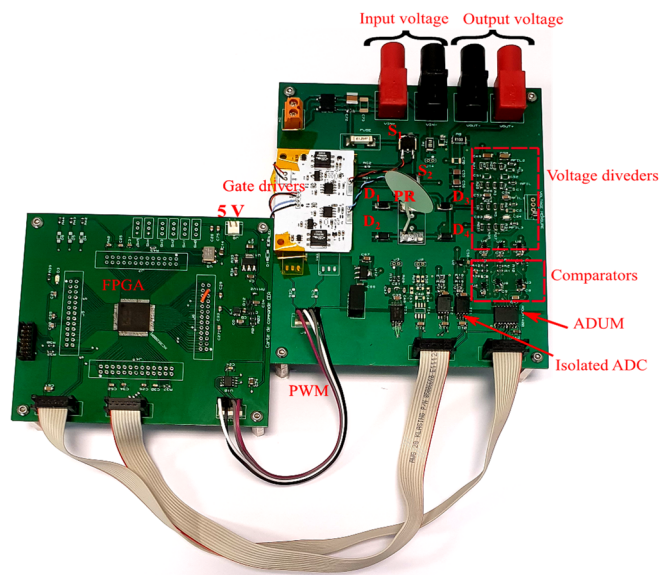


Fig. 6: Prototype circuit.

Table II: Reference of power components

	MOSFET Switch (S1, S2)	Diode (D1, D2)	Diode (D3, D4)
Reference	STD5NM50T4	US1G	VSSB310

Experimental waveforms

Dynamic response

Figure 7 shows the dynamic response for an input voltage of 120 V and an output voltage of 48 V, the output power is 10 W. As shown in Fig. 7, the converter operates firstly in open loop to increase the amplitude of oscillation, in order to detect the 0 current crosses and to measure the frequency of the PR. During this phase, the oscillation amplitude is not monitored because the switching sequences is not synchronized with the internal current. In a second step, the regulation is turned-on. As shown, the amplitude of oscillations decreases and the output voltage is regulated to the reference value. The settling time is 1.2 ms for the output voltage reach 90% of voltage reference. The conversion cycle is presented in steady state in the upper right part of Fig.7. The experimental waveform V_p is matching with the theoretical one (see Fig.3). The current i_p displayed in Fig.7 represents the internal current i measured during only the constant voltage, since no current flow during isolated phases. From the waveform of i_p , we can deduce the instantaneous current of i_{in} and i_{out} . Indeed, i_{in} equals current i_p during phase 1, and i_{out} is the current i_p during phase 1, phase 3 and $-i_p$ during phase 5. Moreover, the waveform of the internal current i can be approximated by a sinusoidal curve, as shown in Fig.7. We have measured 94.05% of efficiency at 10 W output power for 120/48 V input-output voltage considering only the power circuit. We have measured 1.1 W at 5 V power supply for the FPGA and the driving stage, which is quite high for our application, but no optimization was done for this circuit (out of the scope of this paper). However, the high efficiency and power densities of PRs-based converters could motivate the investigation in optimization of integrated digital controller (ASIC) with low cost and low power consumption.

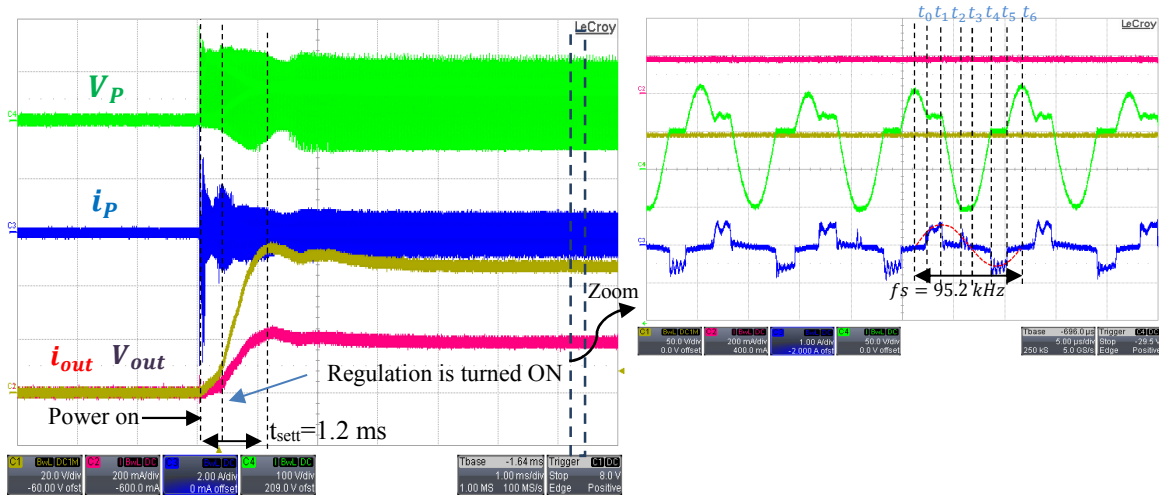


Fig. 7: Experimental dynamic response for input voltage 120 V and output voltage 48 V at 10 W.

Load variation

The load transient is examined for load variation. Fig. 8(a) shows a step change in load from 7 W to 13 W, and the output current goes from 0.145 A to 0.27 A. We can see that the output voltage V_{out} falls by 6 V before going back to the voltage reference when the load variation is applied. The output voltage is then regulated after 2.2 ms. Moreover, the resonance frequency decreases from 96.9 kHz to 94.3 kHz, as the amplitude of the oscillation increases on current i_p . It is noted that during the transient response, the switching driving still synchronized with the resonance period of the PR since no overshoot of

current i_p is observed. Fig. 8(b) shows a step change in load from 13 W to 7 W. In this case, the overshoot of the output voltage is less than 2 V and the output current i_p reaches the desired 0.145 A value after 2.5ms. We can also observe an overshoot on current i_p because no ZVS of S_1 is ensured since voltage V_p did not reach V_{in} at the end of the period. However, the regulation of t_s operates to ensure soft switching of S_1 , as shown in steady state.

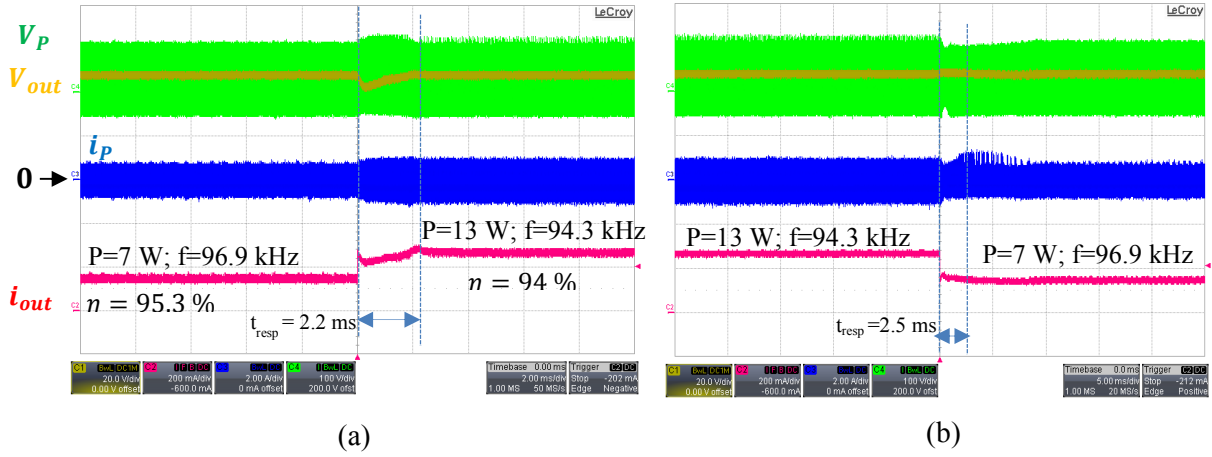


Fig. 8: Dynamic response for load variations.

Efficiency

Figure 9 shows the efficiency as a function of the output power for $V_{in} = 120\text{ V}$ and for different gain ratios up to $\frac{V_{out}}{V_{in}} = 0.4$. Experimentally, we have noted that the maximum output power for our PR is limited by the amplitude of the PR current I ($\approx 1\text{ A}$) due to the rise of temperature. So, increasing the output voltage will increase the maximum output power allowed, as shown in Fig.9. For a fixed input voltage, the efficiency increases when the output voltage increased as the amplitude of the current decreases, which decreases the power losses by I^2 . We have obtained an efficiency higher than 94% for large operating power range and a peak efficiency of 96% is obtained for $\frac{V_{out}}{V_{in}} = 0.4$ and $P_{out} = 8\text{ W}$.

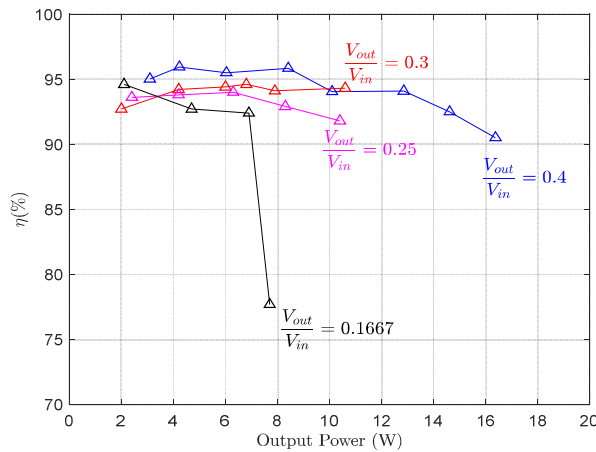


Fig. 9: Efficiency Vs Output Power for $V_{in} = 120\text{ V}$ and for different gain ratios up to $\frac{V_{out}}{V_{in}} = 0.4$.

Conclusion and future works

The concept to control a new DC-DC step-down converter based on a piezoelectric resonator is introduced in this paper. The conversion principle is explained in details. The control strategy is modeled and implemented in a FPGA. The operating with good performances is verified. Furthermore, our

specific control strategy enables to regulate efficiently the output at any voltage between $0 V$ to $\frac{V_{in}}{2}$ in less than 1.4 ms. Experimental results validated both the dynamic response and the steady state operations. Efficiency up to 94.05 % has been measured at 10 W and at input-output voltages of 120 - 48 V.

This paper demonstrate the feasibility of controlling dc-dc converter based on PR by using commercial components, however, we can reduce consumption and increase performances by integrating the control circuit into an ASIC, which is one of the scopes of our lab. The principle using PZT PR in DC-DC converters makes it an excellent solution for very compact, high input voltage, low output voltage applications at low power and high efficiency. Many opportunities still have to be explored such as serialization and/or parallelization of PRs to increase the power. As a conclusion, this new operating principle gives new opportunities in power electronics with the aims of miniaturizing and integration. It could be a serious challenger for magnetic and electrostatic based converters.

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