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FEC performance comparison for short frame sizes for NR

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1 Introduction

Simulation results for the different coding schemes have been presented during the last two RAN1 meetings. However, direct comparisons of obtained results by different proponents have not been performed yet. Indeed, due to the lack of agreement regarding strict constraints on simulation conditions and due the small differences obtained in most performance results, it is quite difficult to derive concrete conclusions. In fact, most of the performance differences result from the disparities in the simulation conditions such as the number of iterations and the choice of the decoding algorithm. Therefore, there was a common informal understanding that the different code proposals are all equivalent from the performance point of view.

In this contribution, we analyze some of the results obtained for the short frame sizes where large differences exist between the different code families. These differences are beyond the gaps that can be observed due to unfair simulation conditions.

2 Performance comparison

The performance comparison presented in this section focuses on comparing the results of the contributions for the LDPC codes [1] and for the improved Turbo code [2]. Please note that the simulation conditions seem “unequal”, favoring the LDPC code family since the best decoding algorithm based on the sum-product method is used with as high as 50 iterations.

Indeed in practice, a simplified version of the log-domain variant is commonly used known as “offset min-sum” which generally presents a slight degradation in performance of several tenths of a dB with respect to the sum-product version. In most cases, this penalty increases with decreasing coding rate calling for other more complex variants based on the λ -min algorithm [3]. In addition, 50 decoding iterations can be considered as excessive in practice and in comparison to the 8 iterations performed for the turbo decoder despite the unequal complexity of the iteration for each type of decoder family.

We recall the simulation conditions:

The simulations were performed over an Additive White Gaussian (AWGN) channel and a QPSK modulation.

For the LDPC decoder [1] denoted by Multi-Edge (ME) LDPC in Fig.1:

- Sum-product algorithm
- Floating point simulations
- 50 iterations

For the Turbo decoder [2] denoted by Enhanced TC in Fig.1:

- Max-Log MAP algorithm with a scaling factor (simplified log-domain algorithm)
- Floating point simulations
- 8 iterations

After analyzing the simulation results in the previously mentioned contributions, we can state that the conclusions indicating “similar” performance indeed holds for larger frame sizes since the observed performance differences are within the margins caused by the unequal simulation conditions. Of course, the compared codes do not achieve such results at the same hardware complexity. Comparisons regarding complexity are not addressed in this contribution.

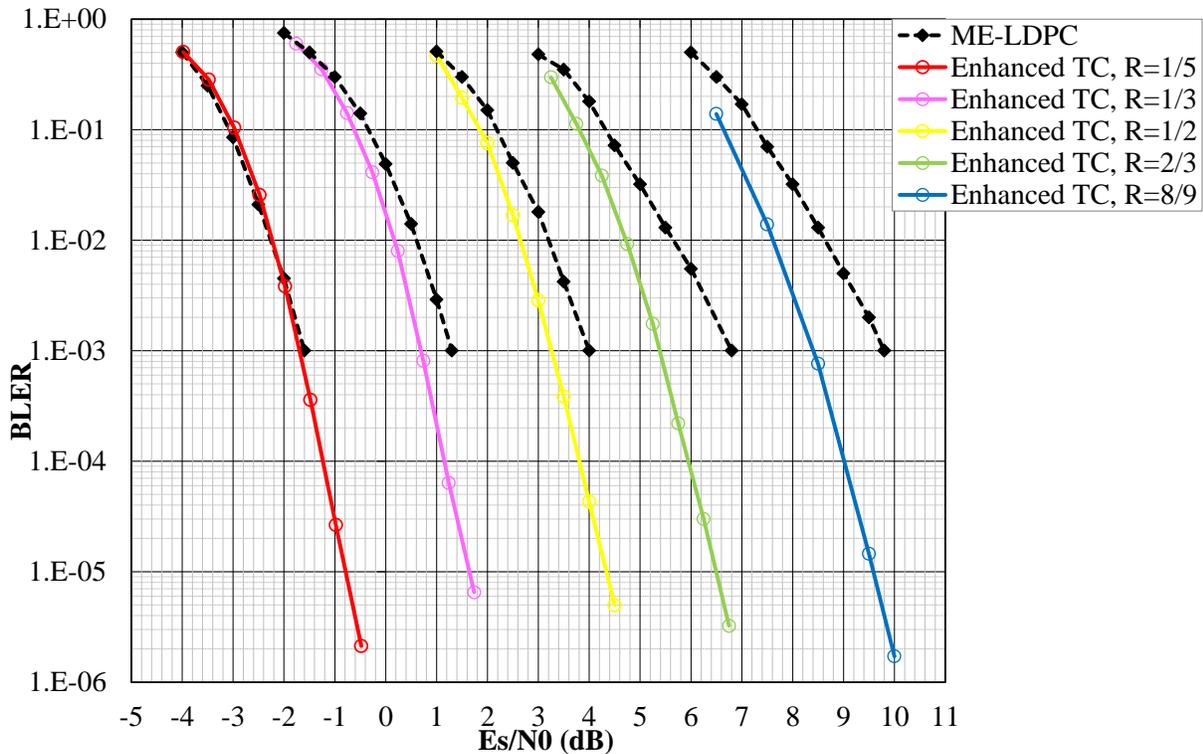


Figure 1. Performance comparison of the improved turbo code with the Multi-Edge LDPC code in AWGN channel for coding rates ranging from 1/5 to 8/9 in terms of BLock Error Rate vs E_s/N_0 . QPSK modulation, block size K around 100 bits.

Furthermore, some tendencies can be observed. Turbo codes tend to outperform LDPC codes when decreasing the frame size despite the simulation conditions favoring the LDPC code. Indeed, for short frame sizes of around 100 information bits, we can clearly see in Fig.1 that the proposed improved turbo code largely outperforms the proposed LDPC code by more than 1.5dB in some cases. It is important to note that the gap increases with increasing coding rate in favor of the turbo code while it is commonly assumed that such a code family presents a weakness for such high rates.

Another interesting aspect is the absence of the error floor down to 10^{-6} of BLER for the improved turbo code.

Observation 1: The improved Turbo code and the proposed LDPC code present similar performance at large frame sizes.

Observation 2: Improved Turbo code tends to outperform proposed LDPC code when decreasing frame sizes.

Observation 3: Performance gain of the improved Turbo code can exceed 1.5dB for 100-bit frame size.

Observation 4: The observed gain of the improved Turbo code increases with the coding rate.

Observation 5: No error floor was observed for error rates as low as 10^{-6} of BLER for the improved Turbo code.

3 References

- [1] R1-164698 “LDPC - Performance evaluation”, Qualcomm Incorporated, Nanjing, China, May 2016.
- [2] R1-167414, “Enhanced Turbo Codes for NR: Performance Evaluation”, IMT and Orange, Goteborg, Sweden, Aug. 2016.
- [3] F. Guilloud, E. Boutillon, J.L. Danger, “Lambda-Min decoding algorithm of regular and irregular LDPC codes”, 3rd International Symposium on Turbo Codes and related topics, 1-5 september, Brest, France, 2003.