



**HAL**  
open science

## Gate length dependent transport properties of in-plane core-shell nanowires with raised contacts

Alexandre Bucamp, Christophe Coinon, David Troadec, Sylvie Lepilliet, Gilles Patriarche, Xavier Wallart, L. Desplanque

► **To cite this version:**

Alexandre Bucamp, Christophe Coinon, David Troadec, Sylvie Lepilliet, Gilles Patriarche, et al.. Gate length dependent transport properties of in-plane core-shell nanowires with raised contacts. Nano Research, 2020, 13 (1), pp.61-66. 10.1007/s12274-019-2572-8 . hal-02974920

**HAL Id: hal-02974920**

**<https://hal.science/hal-02974920>**

Submitted on 15 Dec 2020

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

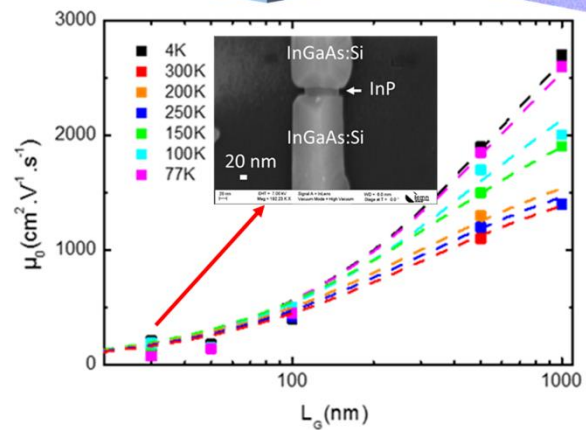
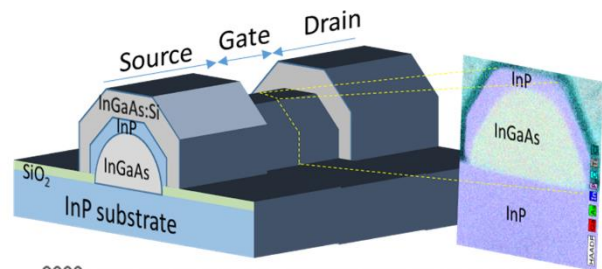
## TABLE OF CONTENTS (TOC)

### Gate length dependent transport properties of in-plane core-shell nanowires with raised contacts

Alexandre Bucamp<sup>1</sup>, Christophe Coinon<sup>1</sup>, David Troadec<sup>1</sup>, Sylvie Lepilliet<sup>1</sup>, Gilles Patriarche<sup>2</sup>, Xavier Wallart<sup>1</sup> and Ludovic Desplanque<sup>1,\*</sup>

<sup>1</sup>Univ. Lille, CNRS, Centrale Lille, Yncréa ISEN, Univ. Polytechnique Hauts-de-France, UMR 8520 - IEMN, F-59000 Lille, France

<sup>2</sup>C2N - UMR 9001 CNRS, Université Paris-Sud - Université Paris-Saclay, 91120 Palaiseau, France



The transport properties of in-plane InGaAs/InP core-shell nanowires with raised contacts grown by selective area molecular beam epitaxy are investigated through the characterization of MOSFET devices with gate length down to 30nm.



# Gate length dependent transport properties of in-plane core-shell nanowires with raised contacts

Alexandre Bucamp<sup>1</sup>, Christophe Coinon<sup>1</sup>, David Troadec<sup>1</sup>, Sylvie Lepilliet<sup>1</sup>, Gilles Patriarche<sup>2</sup>, Xavier Wallart<sup>1</sup> and Ludovic Desplanque<sup>1</sup> (✉)

<sup>1</sup>Univ. Lille, CNRS, Centrale Lille, Yncréa ISEN, Univ. Polytechnique Hauts-de-France, UMR 8520 - IEMN, F-59000 Lille, France

<sup>2</sup>C2N - UMR 9001 CNRS, Université Paris-Sud - Université Paris-Saclay, 91120 Palaiseau, France

© Tsinghua University Press and Springer-Verlag GmbH Germany, part of Springer Nature 2018

**Received:** day month year / **Revised:** day month year / **Accepted:** day month year (automatically inserted by the publisher)

## ABSTRACT

Three-dimensional nanoscale crystal shaping has become essential for the precise design of advanced electronic and quantum devices based on electrically gated transport. In this context, III-V semiconductor-based nanowires with low electron effective mass and strong spin-orbit coupling are particularly investigated because of their exceptional quantum transport properties and the good electrostatic control they provide. Among the main challenges involved in the processing of these nanodevices are (i) the management of the gate stack which requires ex-situ passivation treatment to reduce the density of traps at the oxide/semiconductor interface, (ii) the ability to get good ohmic contacts for source and drain electrodes and (iii) the scalability and reliability of the process for the fabrication of complex architectures based on nanowire networks. In this paper, we show that selective area molecular beam epitaxy of in-plane InGaAs/InP core-shell nanowires with raised heavily doped source and drain contacts can address these different issues. Electrical characterization of the devices down to 4K reveals the positive impact of the InP shell on the gate electrostatic control and effective electron mobility. Although comparable to the best reported values for In(Ga)As nanostructures grown on InP, this latter is severely reduced for sub-100 nm channel highlighting remaining issue to reach the ballistic regime.

## KEYWORDS

Molecular Beam Epitaxy, core-shell nanowire, selective area growth, effective electron mobility

## 1. Introduction

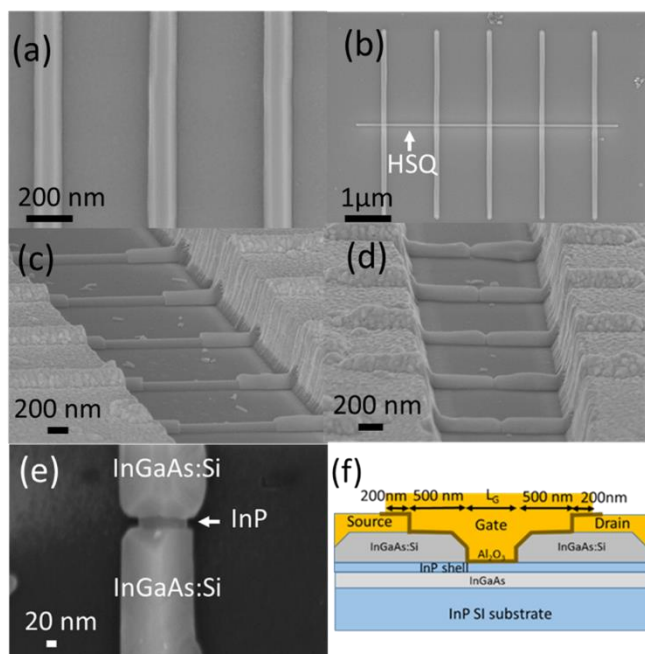
During the last fifteen years, many research efforts have targeted the fabrication of efficient MOSFETs based on low effective mass III-V materials that could reduce the power consumption of CMOS devices. Among these developments, metal-organic based nanoscale selective area epitaxy has demonstrated its efficiency for the integration of III-Vs on silicon [1-3], for the gate stack engineering [4], for self-aligned contact definition [5] or for the elaboration of quantum confined nanostructures [6-8]. More recently, molecular beam epitaxy (MBE) has also proven its usefulness for fabricating InAs or InSb in-plane nanowires (NW) [9-14] that combined with the in-situ deposition of an aluminum superconducting shell could produce hybrid mesoscopic devices for quantum bit manipulation [15]. Thus, even if silicon has remained the material of choice for CMOS, the technological breakthroughs that have been developed offer an interesting playground for the fabrication of nanoscale devices based on III-V materials with strong spin orbit coupling for quantum technologies. In this frame, MBE grown InGaAs presents an interesting trade-off between electron effective mass, spin orbit coupling and structural quality because it can be associated with lattice matched InP barrier and semi-insulating substrate and can be grown in the form of in-plane nanostructures with good electrical properties [16]. In this paper, we show that surrounding the InGaAs in-plane nanowire core by an InP shell results in a low

interface trap density at the oxide/semiconductor interface without any ex-situ passivation treatment. Together with raised source and drain Si doped InGaAs contacts the resulting nanostructure turns out to be an efficient MOSFET with a scalable gate length down to 30 nm. Electrical characterization of the transistors is performed down to 4K and we particularly investigate the impact of the gate length on the gate coupling efficiency and the effective electron mobility.

## 2. Experimental

The fabrication of the three-dimensional (3D) architectures of InGaAs/InP in-plane NWs requires a two-step selective area MBE growth. Semi-insulating InP (001) substrates are first patterned with a silicon dioxide mask following the process described in [17]. 3  $\mu\text{m}$  long and 1  $\mu\text{m}$  down to 50 nm wide openings in SiO<sub>2</sub> oriented both in [110] and [1-10] directions are defined for the first epitaxy. After in-situ III-V native oxides removal by annealing the sample at 500°C under atomic hydrogen and arsenic flux, in-plane InGaAs NWs are grown selectively with respect to the silicon dioxide mask using atomic hydrogen assisted MBE [16]. An InP shell with a 10 nm nominal thickness is then added after transfer of the sample under ultra-high vacuum in another MBE system equipped with a phosphine thermal cracker cell. Details about the selective area MBE growth conditions for the InGaAs and InP layers can be found in references [13] and [18] respectively. The nominal deposited

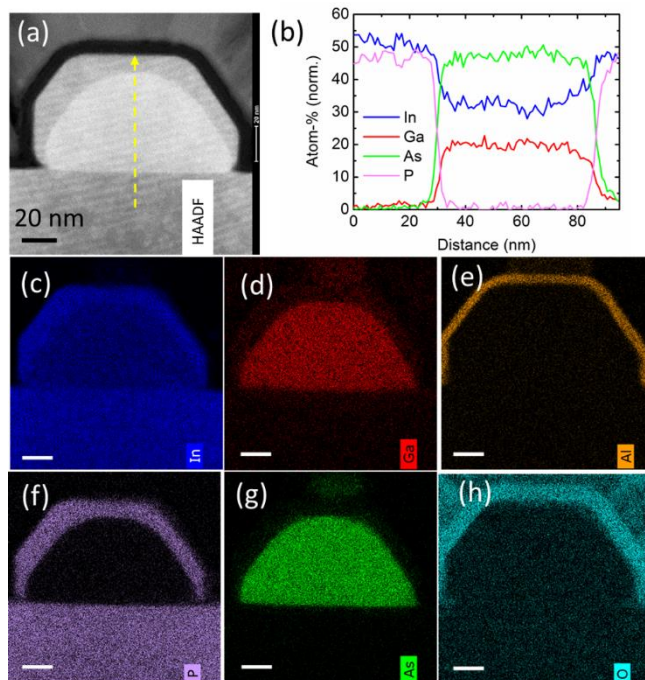
thickness of undoped InGaAs and InP are respectively 30 and 10 nm.



**Figure 1.** SEM images after different steps of the device fabrication: after selective area MBE of in-plane InGaAs/InP core-shell nanowires inside 100 nm wide openings in the SiO<sub>2</sub> layer (a), after the deposition of a HSQ ribbon on the array of in-plane InGaAs/InP nanowires (b), after regrowth of InGaAs:Si raised contacts, source and drain pads deposition and HSQ removal (c and d), zoom on the channel part after removing the 30 nm wide HSQ ribbon (e), and gate metal deposition on multi (f) or single NW (g) transistors. Scheme of the longitudinal cross-section of the devices (hf).

Scanning Electron Micrograph (SEM) of an array of in-plane core-shell nanowires grown inside 100 nm openings can be seen on figure 1a. After growth, a part of the nanostructures is masked using hydrogenosilsesquioxane resist (HSQ) ribbons (figure 1b). These 1 μm down to 30 nm wide ribbons are patterned with the spin-coating of an 80 nm thick layer of Dow Corning XR-1541 resist, e-beam exposure and tetramethylammonium hydroxide based development. A subsequent 200 °C annealing under N<sub>2</sub>/H<sub>2</sub> is performed before the introduction of the sample into the outgazing chamber where it is annealed under ultra-high vacuum for 90 minutes. After III-V native oxides removal as for the first epitaxy, the HSQ ribbons serve as a dummy gate for the subsequent selective area MBE growth of silicon doped InGaAs contacts with nominal thickness and doping of 30 nm and 2 × 10<sup>19</sup> cm<sup>-3</sup> respectively. After source and drain metal contact deposition using standard e-beam lithography, HSQ ribbons are removed using a buffered hydrofluoric acid solution (figures 1c-e). A 7 nm thick Al<sub>2</sub>O<sub>3</sub> layer is then deposited using Atomic Layer Deposition at 300 °C in a Benecq TFS200 system. Eventually a Ti/Au gate metallization is performed to obtain MOSFET devices (figures S1a and S1b). The longitudinal dimensions of the devices are schemed in figure 1f.

Transmission Electron Microscope cross sections are performed after the whole process by means of Focus Ion Beam (FIB) etching. The STEM studies are carried out on a Titan Themis 200 (FEI) microscope equipped with a spherical aberration corrector on the probe and the EDX analysis system super X (0.7 sr solid angle of collection). The accelerative voltage was 200 kV. The (half) convergence angle of the probe was 17.6 mrad and the probe current 85 pA.

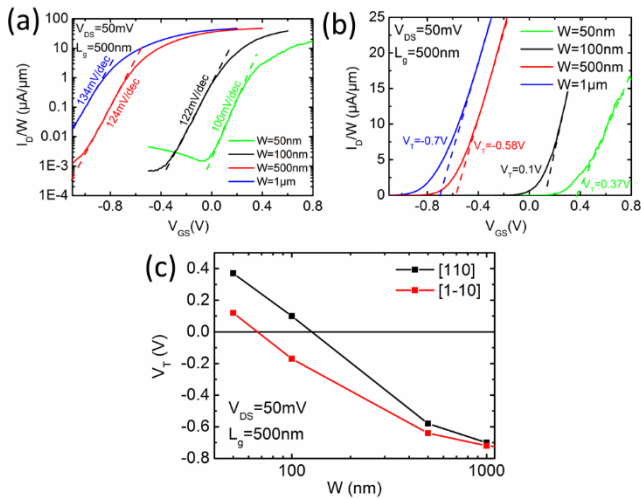


**Figure 2.** High Angle Annular Dark field (HAADF) image of the channel cross-section of an InGaAs/InP core-shell nanowire grown inside a 100 nm wide opening along [110] (a). The dash line indicates the position of the line scan of the composition profile given in graph (b). Detailed chemical composition of the NW: Indium (c), Gallium (d), Aluminum (e), Phosphorus (f), Arsenic (g) and Oxygen (h). The scale bar is 20 nm.

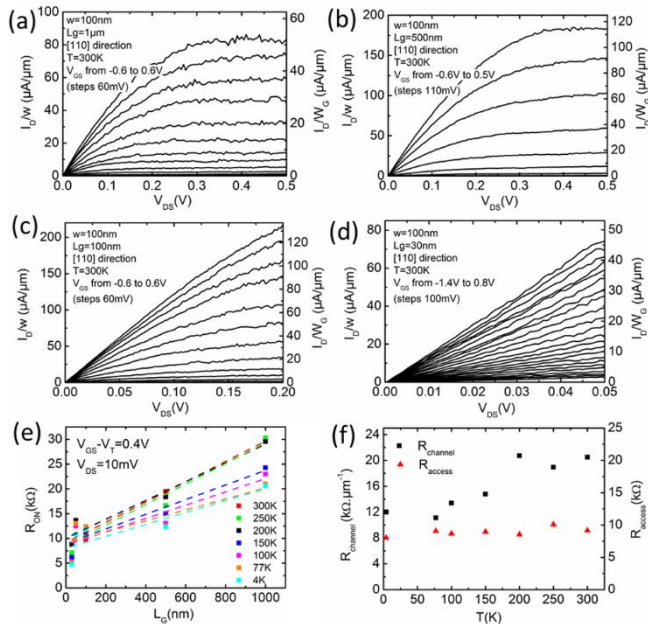
### 3. Results and discussion

The scanning transmission electron micrograph (STEM) and EDX chemical analysis of the cross sections taken off in the channel area of transistors grown inside 100 nm wide openings reveal that along [110] direction (figure 2), the InGaAs core exhibits a half cylinder shape with a radius of approximately 50 nm whereas the InP shell is roughly delimited by a semi-hexagonal contour formed by (1-10), (111) and (001) facets. The composition profile of III and V elements constituting the structure and deduced from EDX analysis indicates that the indium content in the InGaAs core is about 60% at the basis but evolves to 70-75% at the extreme top of the nanostructure (figure 2b). The rounded shape of the InGaAs core with the absence of a well-defined top (001) facets is quite different than the one observed for shell-free In<sub>0.53</sub>Ga<sub>0.47</sub>As in-plane nanowires grown with the same conditions [16]. This difference is probably resulting from strain induced indium migration from side facets to the top one.

In the [1-10] direction (supporting information SI-1, figure S1.1), the shape of the InGaAs core is quite similar but the composition grading is reversed since a slight decrease of the indium content is observed from the bottom to the top of the core (figure S1.1b). Concerning the InP shell, it forms mainly (111) facets with a preferential deposition of InP on the top leading to a triangular shape for the nanostructure. The prevalence of these facets can be attributed to the different InP surface energies between (111)<sub>A</sub>, (001) and (111)<sub>B</sub> facets [18]. For larger openings (w=500 nm and w=1 μm), we assume that InGaAs exhibits mainly a (001) surface (supporting information SI-1, figure S1.2).



**Figure 3.** Transfer characteristics at  $V_{DS}=50\text{mV}$  of single in-plane InGaAs/InP NW MOSFET grown inside mask openings oriented in the [110] crystal direction with different width  $w$  and a gate length of 500nm in logarithmic (a) and linear (b) scales. Evolution of the threshold voltage with respect to the width of the opening for both orientations (c).

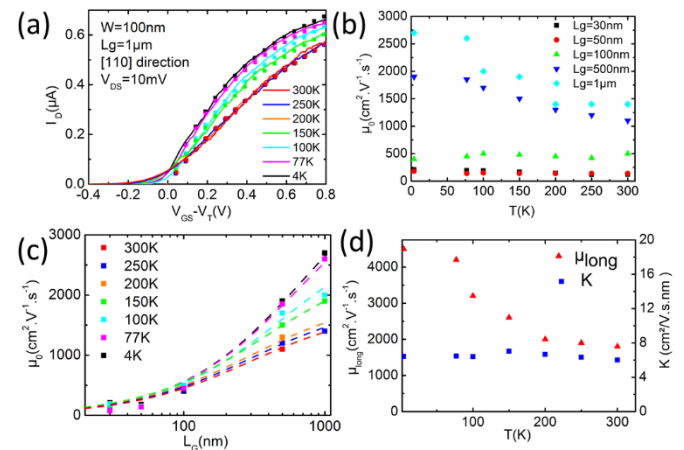


**Figure 4.** Drain current normalized either by the width  $w$  of the mask opening (left scale) or by the gate development  $W_G$  (corresponding to the length of the InGaAs/InP interface deduced from STEM; Right scale) versus drain to source voltage for  $L_G=1\ \mu\text{m}$  (a), 500nm (b), 100nm (c) and 30 nm (d). Resistance of the device for  $V_{GS}-V_T=0.4\text{V}$  and  $V_{DS}=10\text{mV}$  at different temperature versus gate length (e), squares correspond to experimental data and dash lines to linear interpolations. Evolution of the linear resistance of the channel and of the access resistance deduced from these interpolations with respect to the temperature (f).

The MOSFET transfer characteristics measured at 300K for a drain to source voltage of 50 mV are displayed on figure 3 for single NWs with a 500 nm gate length grown inside 1  $\mu\text{m}$  down to 50 nm wide openings and oriented in the [110] azimuth. The characteristics for the other azimuth can be found in supplementary information SI-2. As can be seen, the geometry of the opening and thus the shape of the nanostructure deeply impacts the threshold voltage of the transistor which is about -0.8V for large opening and shifted toward positive voltage when the size of the (001) surface of the nanowires is shrinking with respect to the lateral facets. This evolution is quite similar for both crystal directions although a little more pronounced for the [110] oriented devices which also exhibit an improvement of

the subthreshold slope when the width is reduced. However, for the 50 nm wide opening, a degradation of the conductance slope is observed above the threshold probably because of poor ohmic contacts. In the following, we focus on nanowires grown inside 100 nm wide openings in the [110] direction.

From these nanowires, transistors with different gate length (defined by the HSQ ribbon width) from 1  $\mu\text{m}$  down to 30 nm have been fabricated and their electrical properties above and below the threshold voltage are investigated. Figure 4a-d displays the  $I_D=f(V_{DS})$  characteristics of these devices. In the linear regime (at  $V_{DS}=10\text{mV}$ ), we extract the ON resistance for a fixed gate voltage 0.4 V above the threshold and different temperatures (figure 4e). The linear interpolations of these data enable the identification of the mean linear resistance of the channel and the mean access resistance with respect to the temperature (figure 4f). One can observe that for short channels, the ON state characteristics are mainly governed by the access resistances which exhibit some variations from one device to another. One can also notice that the mean channel resistance decreases when the temperature is reduced, probably related to an improvement of the electron mobility at low temperature.



**Figure 5.** Transfer characteristics measured at different temperature on a single in-plane NW transistor grown inside a 100 nm wide opening and with a gate length of 1  $\mu\text{m}$  (a): solid line corresponds to the measurement and squares to the corrected mobility model with  $\mu_0$  values of figure 5b. Evolution of the electron mobility  $\mu_0$  with the gate length (c): square corresponds to the data deduced from the fit of the transfer characteristics and dashed lines to the model based on Eq. (1) and (2) using the parameters  $\mu_{\text{long}}$  and  $K$  described on (d) with respect to the temperature.

In order to extract the effective electron mobility  $\mu_0$  for each device independently from the access resistance, we used the model proposed by Ghibaudo *et al* [19] involving a mobility correction factor  $\theta$  taking into account series resistance and gate voltage impact to fit our experimental transfer characteristics (figure 5a). This model is based on the following equations [19]:

$$I_D = \frac{W_G \cdot C_i \cdot \mu_0}{L_G(1+\theta(V_{GS}-V_T))} (V_{GS} - V_T) \cdot V_{DS} \quad \text{Eq. (1)}$$

$$\text{with } \theta = \theta_0 + R_S \cdot C_i \cdot \mu_0 \cdot \frac{W_G}{L_G} \quad \text{Eq. (2)}$$

where  $W_G$  is the gate development (length of the transverse core/shell interface),  $C_i$  is the gate capacitance per unit area formed by the 7 nm thick  $\text{Al}_2\text{O}_3$  layer (supporting information SI-3) and the InP shell. Assuming a mean thickness of about 15 nm for the shell, a value of 4.56  $\text{mF/m}^2$  is estimated for  $C_i$ .  $R_S$  is the series resistance

and  $\theta_0$  is the intrinsic mobility reduction factor. The values of  $\theta$  used for the fit as well as their evolution with the temperature are summarized in the supplementary materials SI-4.

Regarding the evolution of the electron mobility  $\mu_0$  with the gate length, a striking degradation can be noticed for short gate length. The highest mobility is indeed obtained for the device with a 1  $\mu\text{m}$  gate length increasing from about  $1500 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$  at room temperature to reach more than  $2700 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$  at 4K. Although reduced, the electron mobility for the device with a 500 nm gate length exhibits a similar behavior. However, for devices with a gate length of 100 nm and below, a much lower value is achieved and no more evolution with the temperature is observed. On figure 5c, this evolution is fitted using the Matthiessen rule involving two different mobility [19]: a diffusion limited classical one  $\mu_{\text{long}}$  independent of the gate length which prevails for long gate length, and a term  $\mu_{\text{short}}$  proportional to the gate length. The relationship between  $\mu_0$ ,  $\mu_{\text{long}}$  and  $\mu_{\text{short}}$  is given by:

$$\mu_0 = \left( \frac{1}{\mu_{\text{long}}} + \frac{1}{\mu_{\text{short}}} \right)^{-1} \quad \text{Eq. (3)}$$

$$\text{with } \mu_{\text{short}} = K \cdot L_G \quad \text{Eq. (4)}$$

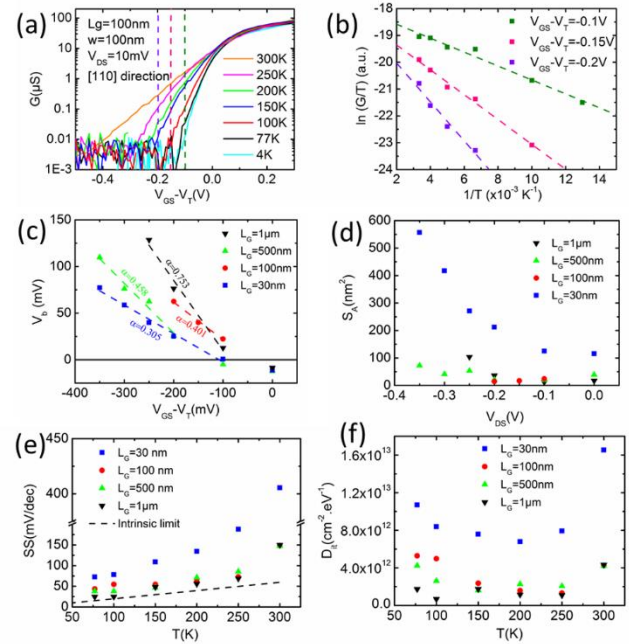
The values of  $\mu_{\text{long}}$  and  $K$  corresponding to the dashed lines of figure 5c are summarized in figure 5d. We can notice that the electron mobility is expected to reach  $4500 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$  at 4K for long NWs and that the  $K$  parameter is almost constant (about  $6.5 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1} \cdot \text{nm}^{-1}$ ) with the temperature. A quasi-linear dependency of the effective electron mobility with the gate length for nanoscale devices has already been observed in different field effect transistors with various interpretations [20-22]. Shur *et al* interpret this phenomenon as an expression of ballistic transport between source and drain in the case of AlGaAs/GaAs HEMTs with submicron gate length [20]. They introduce a term of effective “ballistic” mobility  $\mu_{\text{bal}}$  proportional to the gate length ( $\mu_{\text{bal}} = K_{\text{bal}} \cdot L_G$ ) by substituting the electron mean free path by the gate length in the expression of the mean scattering time. The value of the ballistic coefficient  $K_{\text{bal}}$  is thus only dependent of the injection velocity of electrons from the source, taken as the thermal velocity  $v_{\text{th}}$ .  $K_{\text{bal}}$  can then be expressed from the electron effective mass  $m^*$ , the temperature  $T$ , the Boltzmann constant  $k_B$  and the elementary charge  $q$  according to the following equations:

$$K_{\text{bal}} = \frac{2 \cdot q}{\pi \cdot m^* \cdot v_{\text{th}}} \quad \text{Eq. (5)}$$

$$\text{and } v_{\text{th}} = \sqrt{\frac{8 \cdot k_B \cdot T}{\pi \cdot m^*}} \quad \text{Eq. (6)}$$

However, considering an electron effective mass of InGaAs of about  $0.04 m_0$ , the calculated values of  $K_{\text{bal}}$  using these expressions are much higher than the one deduced experimentally from our  $K$  coefficient. The discrepancy is about one order of magnitude at 300K and even much higher at low temperature (Supporting information SI-5). Even if the electron mobility obtained for a gate length of 1  $\mu\text{m}$  is compatible with a ballistic transport over a length of 30 nm, it seems that another scattering phenomenon related to raised source and drain contacts affects the electron mean free path for short gate length. A similar interpretation was given by Karatsori *et al* in the case of strained or fully depleted SOI MOSFET and InGaAs on insulator FinFET with comparable electron mobility

values [22]. The diffusion of neutral defects from source and drain areas during the process was suspected. Such a mechanism is unlikely to happen in our case considering the quite low thermal budget of fabrication and the low diffusion of Si in InGaAs. More reasonably, elastic scattering from randomly distributed ionized impurities in the heavily doped source and drain extensions is probably the main mechanism inhibiting the ballistic transport [23]. ~~Adding some spacers separating the channel from heavily doped access should limit this phenomenon.~~



**Figure 6.** Conductance versus gate voltage of the transistor for  $V_{\text{DS}}=10\text{mV}$  and various temperatures (a). Arrhenius plot of  $G/T$  values extracted along the vertical dashed lines of figure 6a (b); squares correspond to the experimental data and the dashed lines correspond to the model described with equation 3. Potential barrier  $V_b$  (c) and active cross-sectional area  $S_A$  (d) deduced from the previous model. The dashed lines of figure 6c correspond to the linear regression of the experimental points obtained for different gate length and authorizing the deduction of the gate coupling efficiency  $\alpha$ . Subthreshold slope of the devices with different gate length measured at  $V_{\text{DS}}=10\text{mV}$  and different temperatures (e). The red dashed line represents the theoretical thermionic limit of the slope for a perfect gate coupling. Interface trap density versus temperature and gate length deduced from subthreshold slopes (f).

Let's now turn to the subthreshold regime. Figure 6a displays the evolution of the conductance  $G$  of the device with a 100 nm gate length with respect to the temperature. A clear improvement of the subthreshold slope can be noticed at low temperature. By plotting the evolution of  $G/T$  versus  $1000/T$ , one can extract the potential barrier height  $V_b$  at the source/channel interface for different gate voltage as well as the active cross-sectional area  $S_A$  of the channel following the expression [24]:

$$G = S_A A^* T \frac{q}{k_B} e^{-\frac{qV_b}{k_B T}} \quad \text{Eq. (7)}$$

Where  $A^*$  is the Richardson constant for  $\text{In}_{0.6}\text{Ga}_{0.4}\text{As}$  ( $A^*=4,582 \text{ A} \cdot \text{cm}^{-2} \cdot \text{K}^{-2}$  considering an electron effective mass of  $0.041 m_0$  [25]). The same extraction has been performed for the other devices with gate length of 30nm, 500nm and 1  $\mu\text{m}$  (Supporting information SI-6). These data are summarized in figure 6c and 6d. The slope  $\alpha$  of the  $V_b=f(V_{\text{GS}}-V_{\text{T}})$  curves of figure 6c indicates the gate coupling efficiency. A gate coupling efficiency of 1 corresponds to a complete

transfer of the gate voltage variation on the source/channel conduction band bending. The decrease of  $\alpha$  for small gate length is typically due to short channel effects (SCE), arising when the gate potential is not able to fully deplete the channel. This is confirmed by figure 6d where a larger active cross-sectional area is obtained for  $L_G=30\text{nm}$  meaning that the bulk current is mainly contributing to the OFF-state current. For larger gate length, the small active cross-sectional area indicates that the leakage current is probably located at the channel/gate interface. The density of traps at this interface can be estimated from the values of the subthreshold slope using the following expression [26]:

$$SS = \frac{C_i + C_{it} \frac{k_B T}{q}}{C_i} \ln 10 \quad \text{Eq. (8)}$$

Where  $C_{it}$  the capacitance related to the defects in the gate stack with the density  $D_{it}$  ( $C_{it}=q D_{it}$ ). We can thus deduce  $D_{it}$  from the data of figure 6e (figure 6f). Owing to SCE limiting the subthreshold slope,  $D_{it}$  is largely over-estimated for the device with a 30 nm gate length. For the other devices, a  $D_{it}$  rather independent of the gate length is obtained with a value of about  $4 \times 10^{12} \text{ cm}^{-2} \cdot \text{eV}^{-1}$  at room temperature and lower than  $2 \times 10^{12} \text{ cm}^{-2} \cdot \text{eV}^{-1}$  below 250K. These results are close to the best reported values for III-V MOSFET using a similar extraction method [26]. This is a clear indication of the positive impact of InP shell since no passivation of the surface has been required before the gate oxide deposition.

#### 4. Conclusion

Selective area molecular beam epitaxy is a useful technique to shape III-V semiconductors at the nanoscale. Field effect transistors based on in-plane InGaAs NWs surrounded with an InP shell exhibit a low density of interface traps in the gate stack and quite high effective electron mobility for long channel devices. The regrowth process based on a HSQ dummy gate is useful to contact the nanowire and define very short gate length down to 30 nm but it leads also to a severe effective mobility degradation preventing the ballistic regime to be attained at low temperature. This degradation may come from scattering from source and drain impurities, whose density should be carefully optimized to reduce their impact on electron transport in the channel while keeping low series resistances. With such improvement, we believe that this bottom-up process will be able to break through the barriers for the fabrication of nanoscale reliable quantum circuits.

#### Acknowledgements

The authors would like to acknowledge financial support from the French Technological Network Renatech, and the Région Hauts de France.

**Electronic Supplementary Material:** Supplementary material (additional information about STEM analysis of nanostructures, electrical characterization, effective electron mobility and ballistic model) is available in the online version of this article.

#### References

[1] N. Waldron, C. Merckling, W. Guo, P. Ong, L. Teugels, S. Ansar I, D. Tsvetanova, F. Sebaai, D.H. van Dorp, A. Milenin, D. Lin, L. Nyns, J. Mitard, A. Pourghaderi, B. Douhard, O. Richard, H. Bender, G. Boccardi, M. Caymax, M. Heyns, W. Vandervorst, K. Barla, N. Collaert and AV-Y. Thean, Digest of Technical Papers - Symposium on VLSI Technology 2015, 1–2 (IEEE, 2014).

[2] M.Borg, H.Schmid, K.E.Moselund, G.Signorello, L.Gignac, J.Bruley, C. Breslin, P. Das Kanungo, P.Werner, H.Riel, Nano Lett. 14, 1914–1920 (2014).

[3] H.Schmid, M.Borg, K.Moselund, L.Gignac, C. M.Breslin, J.Bruley, D.Cutaia and H.Riel, Appl. Phys. Lett. 106, 233101 (2015).

[4] K. Tomioka and T.Fukui, Device Research Conference - Conference Digest, DRC 488, 15–16 (IEEE, 2013).

[5] M.Egard, L.Ohlsson, M.Ärlelid, K.-M. Persson, M. Borg, F. Lenrick, R.Wallenberg, E.Lind, and L.-E. Wernersson, IEEE Electron Dev. Lett. 33, 369 (2012).

[6] C.B. Zota, D.Lindgren, L.-E.Wernersson and . Lind, ACS Nano 9, 9892–9897 (2015).

[7] J.Gooth, M.Borg, H.Schmid, V.Schaller, S.Wirths, K.Moselund, M.Luisier, S.Karg and H.Riel, Nano Lett. 17, 2596–2602 (2017).

[8] J.S.Lee, S.Choi, M.Pendharkar, D.J.Pennachio, B.Markman, M.Seas, S.Koelling, M.A.Verheijen, L.Casparis, K.D.Petersson, I.Petkovic, V.Schaller, M.J.W.Rodwell, C.M.Marcus, P.Krogstrup, L.P.Kouwenhoven, E.P.A.M. Bakkers, and C.J.Palmström, Phys. Rev. Mat. 3, 084606 (2019)

[9] M.Fahed, L.Desplanque, D.Troade, G.Patriarche and X.Wallart, Nanotechnology 27 (2016) 505301.

[10] M. Fahed, L. Desplanque, D. Troade, G. Patriarche, X. Wallart, J. Cryst. Growth 477, 45–49 (2017).

[11] M.Friedl, K.Cerveny, P.Weigele, G.Tütüncüoğlu, S.Marti-Sánchez, C.Huang, T.Patlaiuk, H.Potts, Z.Sun, M.O.Hill, L.Güniat, W.Kim, M.Zamani, V.G.Dubrovskii, J.Arbiol, L.J.Lauhon, D.M.Zumbühl and A. Fontcuberta i Morral, Nano Lett. 18, 2666–2671 (2018).

[12] M.Pastorek, A.Olivier, Y.Lechaux, N.Wichmann, T.Karatsori, M.Fahed, A.Bucamp, A.Addad, D.Troade, G.Ghibaud, L.Desplanque, X.Wallart and S.Bollaert, Nanotechnology 30 (2019) 035301.

[13] L.Desplanque, A.Bucamp, D.Troade, G.Patriarche and X.Wallart, Nanotechnology 29, 305705 (2018).

[14] P. Aseev, A. Fursina, F. Boekhout, F. Krizek, J. E. Sestoft, F. Borsoi, S. Heedt, G. Wang, L. Binci, S. Marti-Sánchez, T. Swoboda, R. Koops, E. Uccelli, J. Arbiol, P. Krogstrup, L. P. Kouwenhoven, and P. Caroff, Nano Lett. 2019, 19, 218–227.

[15] P. Krogstrup, N. L. B. Ziino, W. Chang, S. M. Albrecht, M. H. Madsen, E. Johnson, J.Nygård1, C.M. Marcus and T. S. Jespersen, Nature Mat 2015, 14, 400–406.

[16] A. Bucamp, C. Coinon, J.-L. Codron, D. Troade, X. Wallart, L. Desplanque, J. Crystal Growth 512 (2019) 11–15.

[17] L.Desplanque et al, Nanotechnology 25 (2014) 465302.

[18] M.Fahed, L.Desplanque, C.Coinon, D.Troade and X.Wallart, Nanotechnology 26 (2015) 295301.

[19] G. Ghibaud, Electron. Lett. 24, 543 (1988).

[20] M. S. Shur, IEEE Electron Device Lett. 23, 511–513 (2002).

[21] J. Luskowski et al, Appl. Phys. Lett. 87, 053507 (2005).

[22] Karatsori et al, IEEE Int. Electron. Dev. Meeting (IEDM) 166 (2018).

[23] Fiori et al, IEEE Int. Electron. Dev. Meeting (IEDM) 202 (2006).

[24] Tettamanzi et al, IEEE Electron Device Lett. 31, 150, (2010).

[25] Goldberg, Handbook Series on Semiconductor Parameters, vol. 2 62–88 (1996).

[26] S.Lee, C.-Y. Huang, D. Cohen-Elias, B. J. Thibeault, W. Mitchell, V. Chobpattana, S. Stemmer, A. C. Gossard, and M. J. W. Rodwell, IEEE Electron Device Lett. 35, 621–623 (2014)





## Electronic Supplementary Material

# Gate length dependent transport properties of in-plane core-shell nanowires with raised contacts

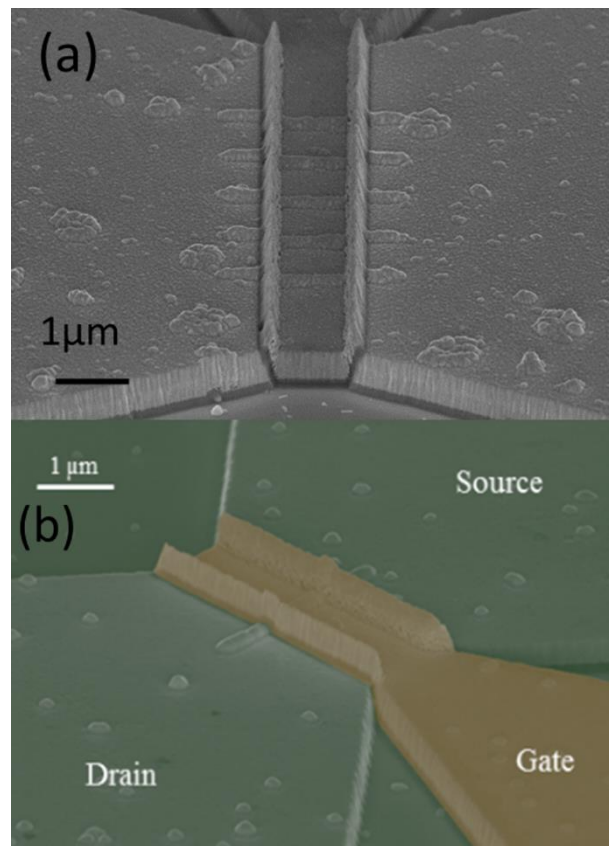
Alexandre Bucamp<sup>1</sup>, Christophe Coinon<sup>1</sup>, David Troadec<sup>1</sup>, Sylvie Lepilliet<sup>1</sup>, Gilles Patriarche<sup>2</sup>, Xavier Wallart<sup>1</sup> and Ludovic Desplanque<sup>1</sup> (✉)

<sup>1</sup>Univ. Lille, CNRS, Centrale Lille, Yncréa ISEN, Univ. Polytechnique Hauts-de-France, UMR 8520 - IEMN, F-59000 Lille, France

<sup>2</sup>C2N - UMR 9001 CNRS, Université Paris-Sud - Université Paris-Saclay, 91120 Palaiseau, France

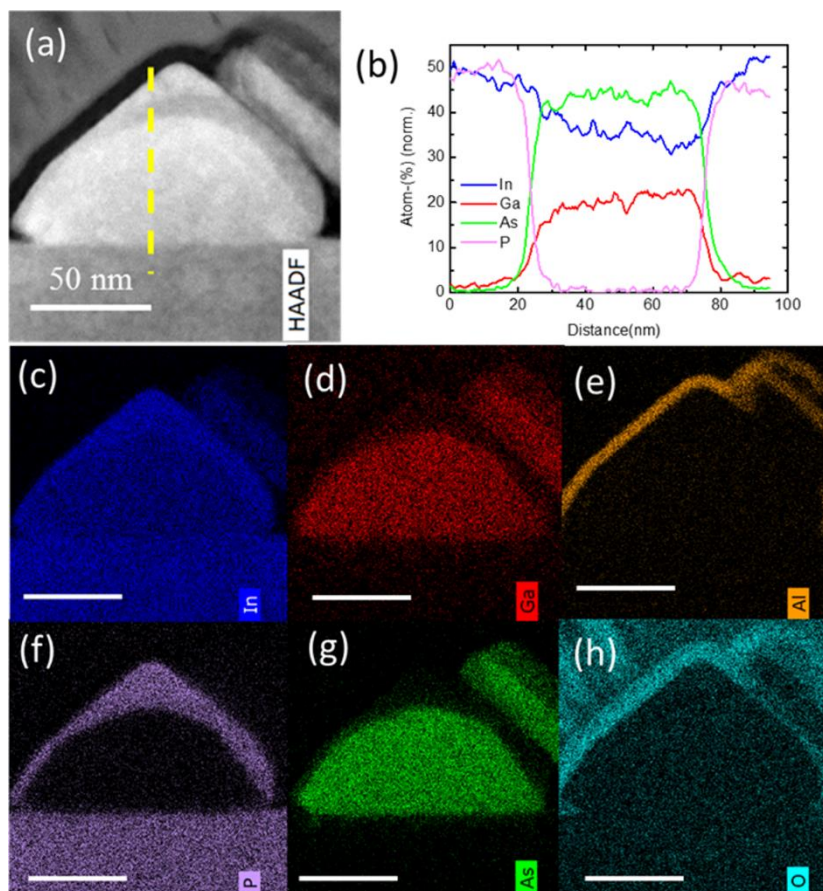
Supporting information to DOI 10.1007/s12274-\*\*\*\*-\*\*\*\*-\* (automatically inserted by the publisher)

### 1. SEM pictures of the fabricated transistors

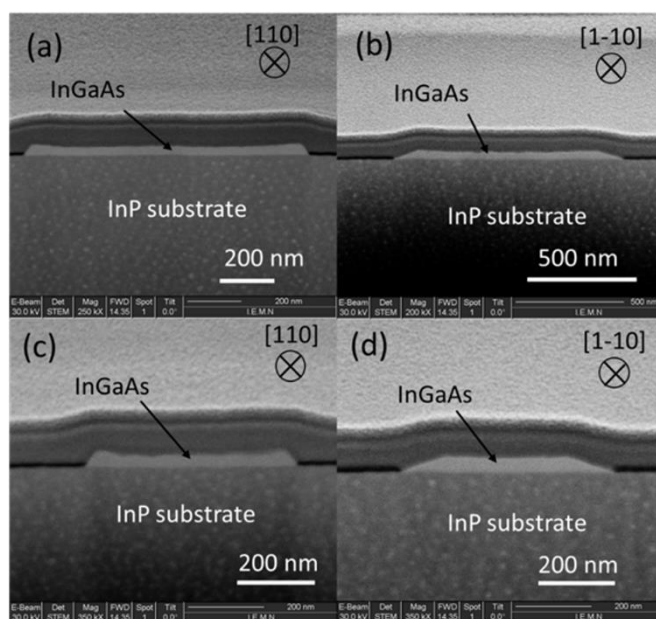


**Figure S1.** SEM image of the transistors fabricated from multiple (a) and single (b) in-plane InGaAs/InP core shell NWs.

## 2. STEM analysis of the channel cross section

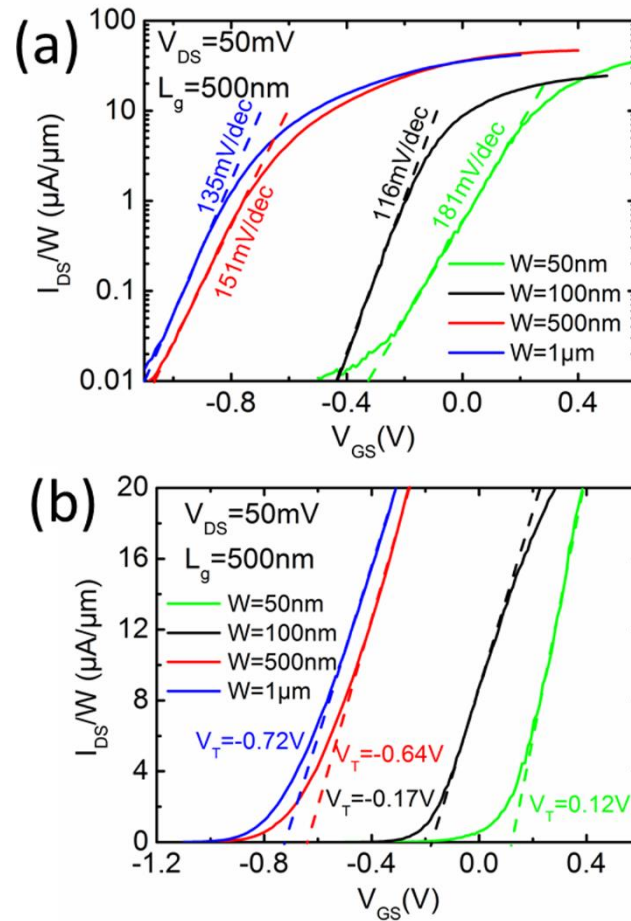


**Figure S2.1.** TEM analysis of the channel cross-section of an InGaAs/InP core-shell nanowire grown inside a 100 nm wide opening along [1-10] direction (a). The dashed line indicates the position of the line scan of the composition profile given in graph (b). High Angle Annular Dark field (HAADF) image (c) and detailed chemical composition of the NW: Gallium (d), Arsenic (e), Aluminum (f), Indium (g), oxygen (h), Phosphorus (i) and Titanium (j). The scale bar represents 20 nm.



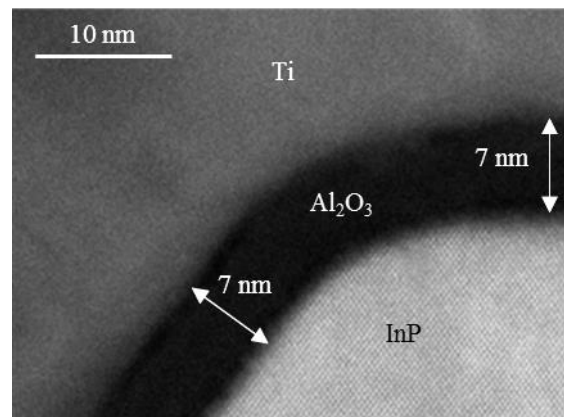
**Figure S2.2.** FIB-STEM cross-section images at 30 keV of 30 nm InGaAs deposited by selective area MBE on InP (001) substrate without InP shell inside SiO<sub>2</sub> openings with a width of 1  $\mu$ m and oriented along [110] (a) and along [1-10] (b) and with a width of 500nm and oriented along [110] (c) and [1-10] (d). InGaAs exhibits mainly a top (001) facet delimited by (111)<sub>B</sub> facets for openings along [110] and delimited by (113)<sub>A</sub> facets for openings along [1-10].

### 3. Transfer characteristics for [1-10] oriented devices with $L_g=500\text{nm}$ :



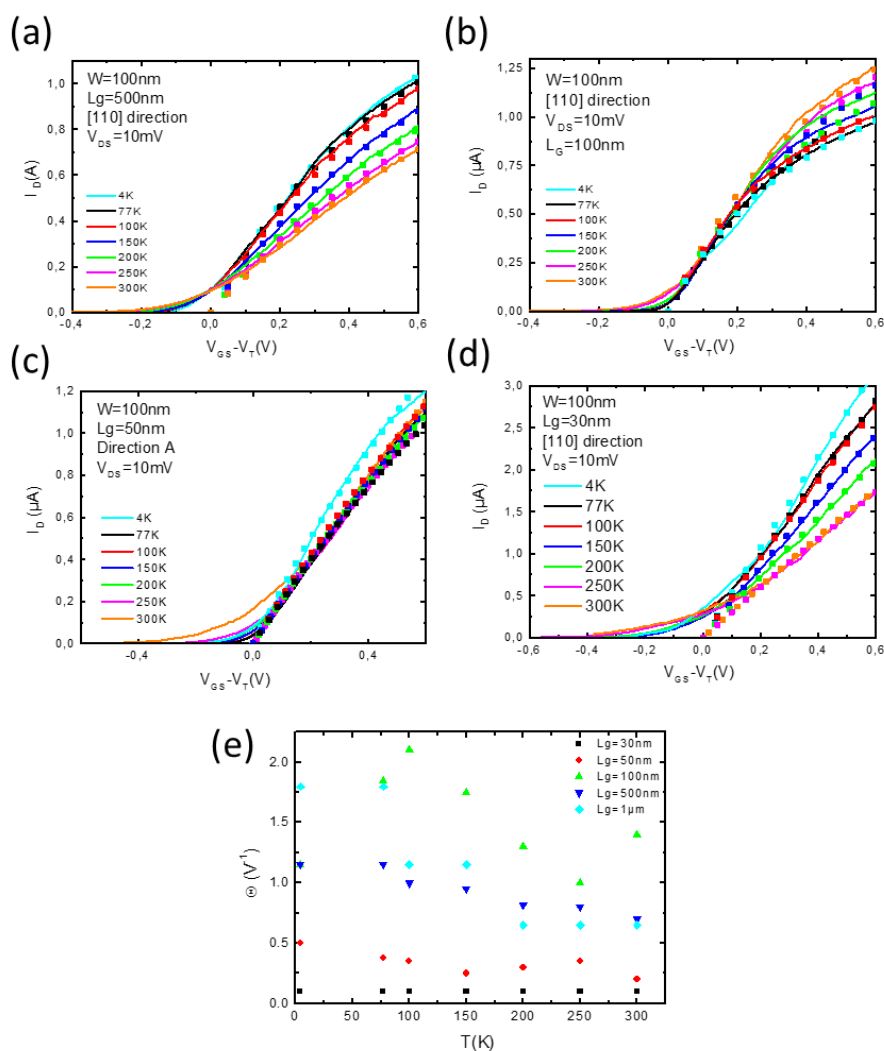
**Figure S3.** Transfer characteristics at  $V_{DS}=50\text{mV}$  of single in-plane InGaAs/InP NW MOSFET grown inside mask openings oriented in the [1-10] crystal direction with different width  $w$  and a gate length of  $500\text{nm}$  in logarithmic (a) and linear (b) scales.

### 4. STEM evaluation of the gate oxide thickness:



**Figure S4.** Cross section STEM image of InP/ $\text{Al}_2\text{O}_3$ /Ti interface

### 5. Effective electron mobility extraction:

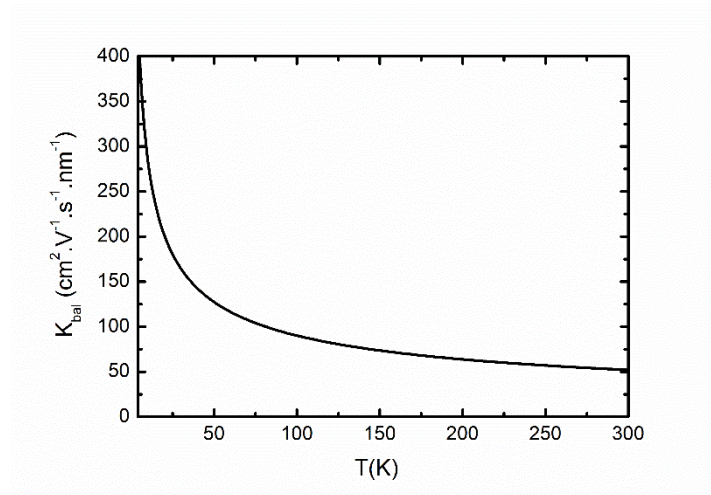


**Figure S5.** Transfer characteristics measured at different temperature on a single in-plane NW transistor grown inside a 100 nm wide opening and with a gate length of 500 nm (a), 100 nm (b), 50 nm (c) and 30 nm (d): solid line corresponds to the measurement and squares to the corrected mobility model with the  $\mu_0$  values of figure 5b. The correction factors  $\theta$  used for the fit are plotted with respect to the temperature (e).

## 6. Calculation of $K_{bal}$ coefficient versus temperature for InGaAs:

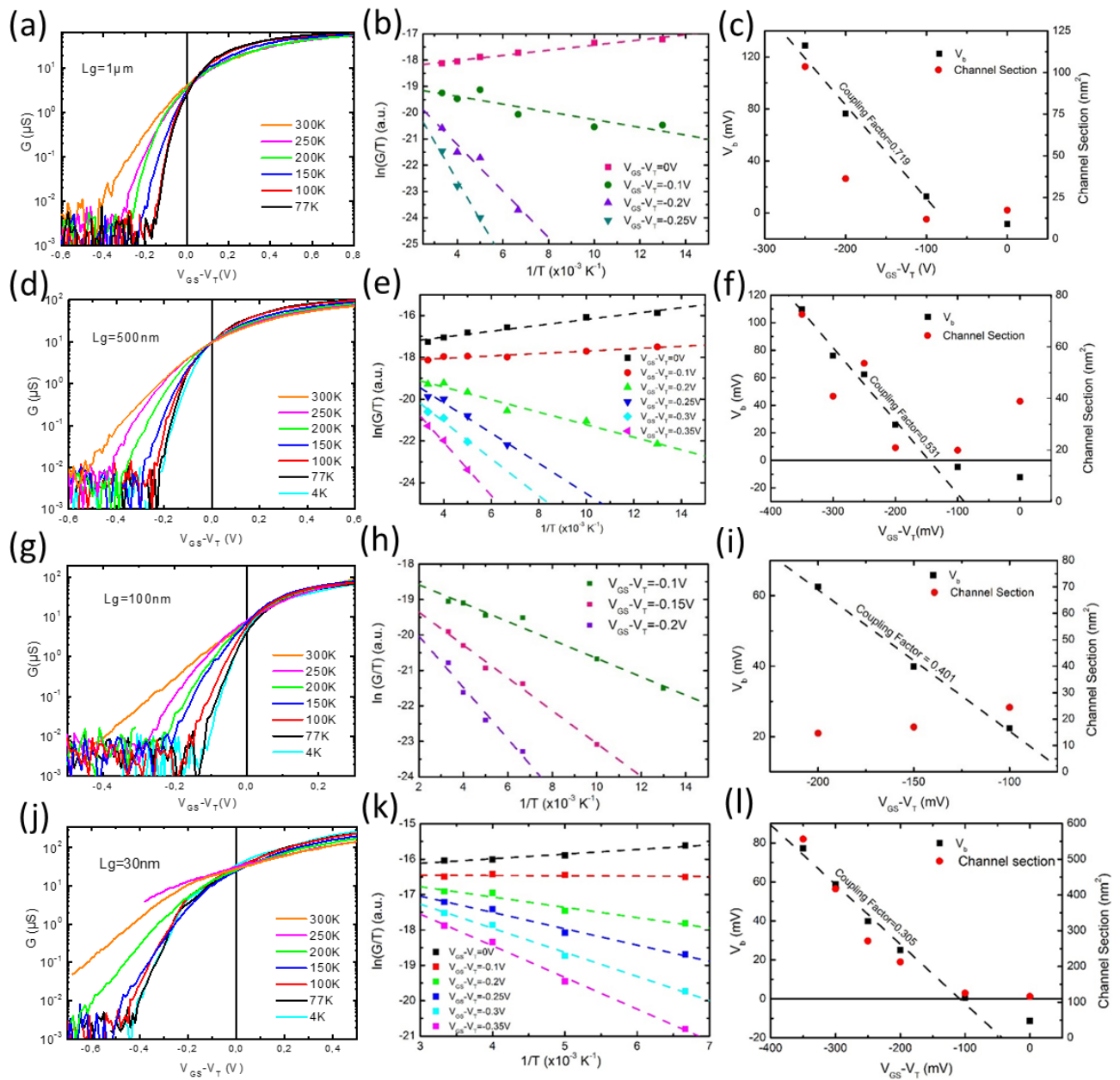
$$K_{bal} = \frac{2 \cdot q}{\pi \cdot m^* \cdot v_{th}} \quad \text{and} \quad v_{th} = \sqrt{\frac{8 \cdot k_B \cdot T}{\pi \cdot m^*}} \quad \text{Eq. (S1)}$$

Where  $v_{th}$  is the thermal velocity.  $m^*$  is the electron effective mass of InGaAs,  $T$  is the temperature,  $k_B$  the Boltzmann constant and  $q$  the elementary charge  $q$ .



**Figure S6.** Calculated values of  $K_{\text{bal}}$  versus temperature.

**7. Source to channel barrier voltage and active channel cross section area:**



**Figure S6.** Device conductance  $G$  versus gate voltage measured at different temperature, Arrhenius plot of  $G/T$  and extracted source to channel barrier voltage  $V_b$  and channel section for single in-plane NW transistor grown inside a 100 nm wide mask opening and with a gate length of 1  $\mu\text{m}$  (a, b, c), 500 nm (d, e, f), 100 nm (g, h, i) and 30 nm (j, k, l).