Comparison between i g integration and v gs derivation methods dedicated to fast short-circuit 2D diagnosis for wide bandgap power transistors

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Comparison Between i_g Integration and v_{gs} Derivation Methods Dedicated to Fast Short-Circuit 2D Diagnosis for Wide Bandgap Power Transistors

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Abstract This study presents and compares two original high-speed protection circuit methods, namely, i_g integration and v_{gs} derivation, against short-circuit types, referred to as, the hard switch fault and fault under load. Since the gate-drain capacitor C_{gd} of a power device depends on the drain to source voltage v_{ds}, it can become an original native sensor to monitor the switching operation and so detect the unwanted v_{ds} transition or the absence of the v_{ds} transition by monitoring only v_{gs}. The use of only low-voltage monitoring, such as v_{gs}, is an essential step to integrate fast and embedded new detection methods into a low-voltage application-specific integrated circuit gate driver, in particular for wide bandgap power transistors. The C_{gd} capacitor plays a major part in the two detection methods. The first method is based on dedicated two-dimensional monitoring of the gate charge transferred in a time interval combined with gate voltage monitoring. The second method consists of the reconstruction of the dv_{gs}/dt by means of a capacitive current sensing to provide the v_{gs} derivation combined with the v_{gs} monitoring. Comparison and simulation of the methods based on a *C2M0025120D* SiC MOSFET device under LTspice™ are made to verify the validity of the methods. In terms of detection speed of the short circuit, a detection time of 200 ns is obtained for both methods. Experimental waveforms based on *C3M0120090J* SiC MOSFET device were included into LTspice™ to push furthermore the methods to their limits and validate the approaches. Both methods are easy to design and to integrate. However, the robustness and the speed of detection trade-off of all these methods should be analysed and compared relative to the critical functionalities.

Keywords: Silicon carbide MOSFETs; normal turn on; short circuit; hard switch fault; fault under load; gate charge

1 Introduction

Wide bandgap semiconductor materials, such as silicon carbide (SiC), have undergone a tremendous evolution in recent years. Power semiconductor devices, such as insulted gate bipolar transistors (IGBTs) and super-junction (SJ-MOSFET) silicon devices, are limited in terms of maximum switching speeds. Consequently, silicon power devices have high switching losses and large and expensive thermal management systems. In contrast, SiC MOSFETs are promising power semiconductor devices for high density converters, with low conduction and switching losses and high temperature stability [[1]]. However, today, the short-circuit (SC) delay time capability for SiC MOSFETs is lower than for silicon devices [[2]]. Power converters designed with these components are therefore less robust.

Power semiconductors devices are used in various industrial applications, including motor drives, battery chargers, switch mode power supplies and converters. These devices are exposed to several types of SC. The hard switch fault (HSF, SC type I) and fault under load (FUL, SC type II) are the two main fault behaviours. Safety is necessary for these typical applications. Several ways of protecting circuits have been presented for either silicon IGBTs or MOSFETs [[3]]. Most of the previously proposed techniques rely on the drain-source voltage or current. This is clearly a limiting approach due to the high voltage detection diode or additional current sensor used, such as MOSFET-sense-current in non-standard dies [[4-5-6-7]].

In SiC MOSFETs, the drain current i_{ds} is controlled by the gate voltage v_{gs}. Since most wide bandgap (WBG) power FETs exhibit a low robustness and a typical fail-to-short behaviour [[8-9-10]], they must be turned-off softly within a few hundreds of nanoseconds after fault detection. Good management of the gate voltage results in the best compromise between losses in electromagnetic induction safety. The reverse transfer capacitance "C_{rss} = C_{gd}" of a SiC MOSFET, also known as the Miller capacitance, is one of the most important parameters in switching performances for unipolar devices. This capacitance is a nonlinear function of voltages v_{gs} and v_{ds} and it provides a feedback between the output voltage v_{ds} and the input v_{gs} of the device.

In this article, detailed analyses and comparisons between the SC detection methods are presented. LTspice™ simulated results are presented in view of verifying the SC detection methods to further protect SiC MOSFETs.

2 i_g integration detection method

2.1. Normal turn on

A useful parameter from the circuit design point of view is the gate charge Q_g, in which the gate charge Q_{gd} related to C_{gd} can be predominant. Figures 1(a) and (b) present the qualitative typical switching waveforms and the different contributions to the total gate charge during normal turn on (NTO). The first gate charge amount Q_1 is defined where $1/C_{issmin}$ is its slope (1), in the first time interval $[t_0 - t_2]$, region A in Fig. 1(d). Q_2 is the second gate charge amount, between $[t_2 - t_3]$ during the Miller plateau, where v_{ds} drops from (v_{bus} + v_{Body}) to approximately (v_{gs}-v_{th}), slightly higher than $R_{dson}.I_{load}$ while v_{gs} stays constant at v_{gsM} and C_{gd} or C_{Miller} starts to discharge, allowing the fast voltage to change across the drain-source terminals, region B in Fig. 1(d). In the presence of a SiC transistor, a short channel is generally used to reduce the losses in the on state. This property causes a greater dependence of v_{gsM} to variations in drain voltage than it can be in vertical silicon device (ex. SJ-VDMOS and IGBT), with a slight slope appearing instead of the plateau [11] (2). The third time interval begins at t_3 with v_{gs} increasing back, until it reaches v_{Drv+}, and gate charge amount Q_g reaches Q_{gTot} (4), with $1/C_{issmax}$ as a slope of the third amount of gate charge Q_3 (3), region C in Fig. 1(d). At the end of this time interval, the capacitance and C_{gs} is fully charged [12–13].

$$Q_1 = C_{issmin} \cdot (v_{gs} - v_{Drv-}) ; \qquad v_{gs} \in [v_{Drv-}; v_{gsM}[\tag{1}$$

$$Q_2 = \int_0^{v_{gsM}} C_{gdmax}.dv_{gd}{}^{(*)} + \int_{v_{gsM}}^{v_{bus}+v_{body}-v_{gsM}} C_{gd}(v_{gd}).dv_{gd} \tag{2}$$

$$Q_3 = C_{issmax}.(v_{gs} - v_{gsM}); \qquad v_{gs} \in]v_{gsM}; v_{Drv+}] \tag{3}$$

$$\begin{gathered} Q_{gTot} = \Delta Q_1 + \Delta Q_2 + \Delta Q_3 \\ \Delta Q_1 + \Delta Q_2 + \Delta Q_3 = C_{issmin} \cdot (v_{gsM} - v_{Drv-}) + C_{gdmax}.dv_{gd} + C_{issmax}.(v_{Drv+} - v_{gsM}) \end{gathered} \tag{4}$$

$$C_{iss} = C_{gs} + C_{gd} \quad ; \quad v_{gsM} = v_{gsplateau} \tag{5}$$

$C_{issMin} = C_{gs} + C_{gdMin}$; $C_{issMax} = C_{gs} + C_{gdMax}$; $C_{rss} = C_{gd}$

Equation (2) represents the region where v_{gs} is held at v_{gsM}. The (*) in Eq. (2) for the first integration is added to include the changes of C_{gd} from t_0 to t_2 Fig. 1(a); t_2 the beginning of the Miller plateau, the non-included integral when v_{ds} starts to fall, region C of the C_{rss} curve in Fig. 1(d). Figure 1(d) illustrates the curves of the three main capacitances of a power transistor [14].

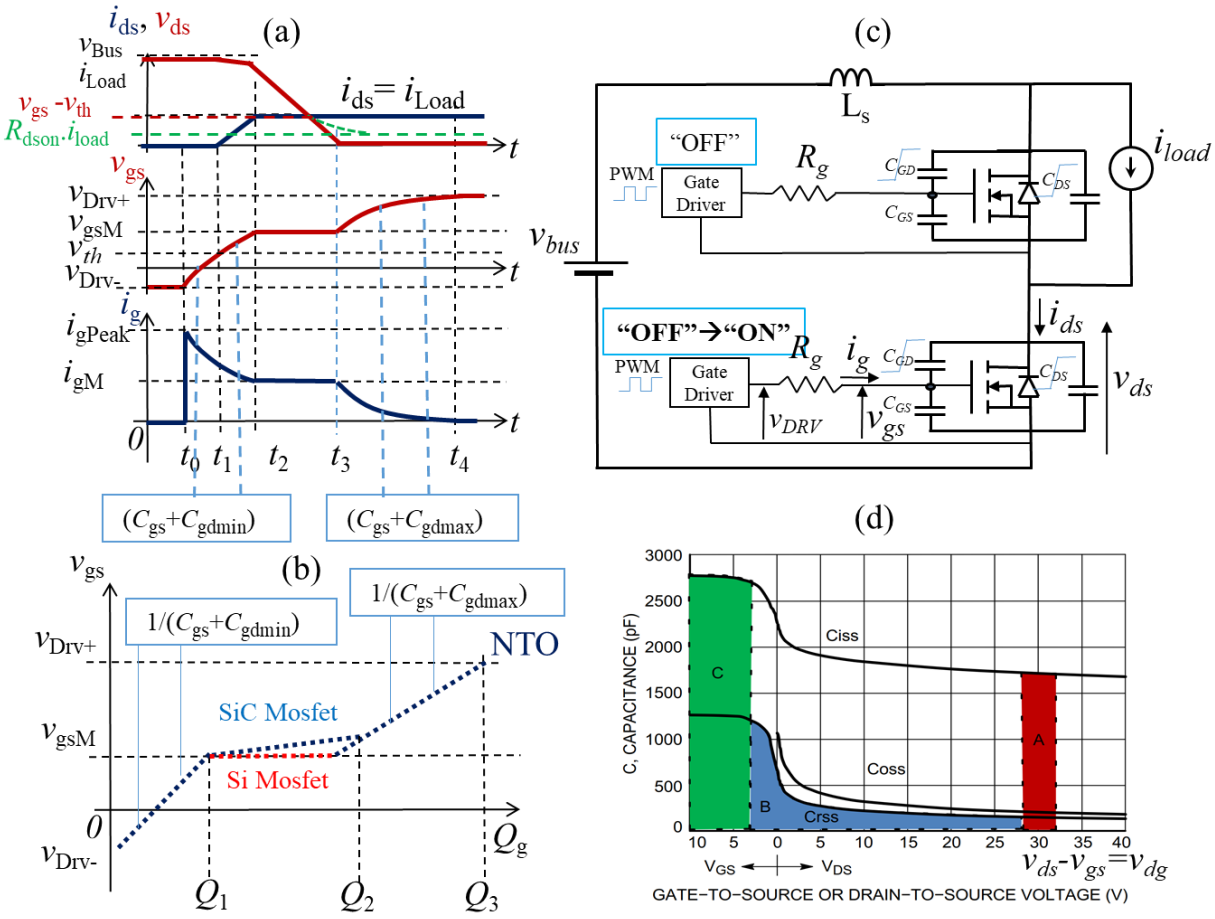

Fig. 1. (a) Turn-on switching characteristics of SiC MOSFET under NTO conditions. (b) Gate charge characteristics "NTO". (c) Equivalent circuit of the half bridge. (d) Capacitance variation.

*Note (Figs. 1–3): For the purposes of a simple graphical representation, C_{gs} and C_{gd} capacitors are taken here as constant values, except C_{gd}, which is modelled as its two asymptotic values C_{gdMin} and C_{gdMax} as illustrated in Fig.1 (d). The voltage drops in the on state of the components (diode and transistor) are also not taken into account for the switching study. A constant Miller plateau is also assumed in the figures. Neither the reverse recovery nor the parasitic inductances are taken into account, here, but will be discussed throughout this article in taken into consideration later on the chapters.

2.2. Hard switch fault

Contrary to fault condition type I, when $v_{gs} = v_{gsM}$ at t_2, v_{gs} and i_{ds} continue to increase until v_{gs} reaches v_{Drv+} and i_{ds} overcurrent, t_3, $i_{ds} = i_{sat\text{-}channel}$. v_{ds} stays at the v_{bus} value, which causes the transistor to operate in its saturation regime, as shown in Fig. 2(a). Such a regime can be sustainable only for a couple of µs, as presented in [10]. The amount of gate charge is $Q_{SC\text{-}HSF}$ with a $1/C_{issmin}$ slope, exhibiting no change in the charging rate of the input

capacitance. In this SC operation, there is no discharge of the Miller capacitance. As a consequence, a significant difference appears in the Q_g characteristic between NTO and HSF, as shown in Fig. 2(b).

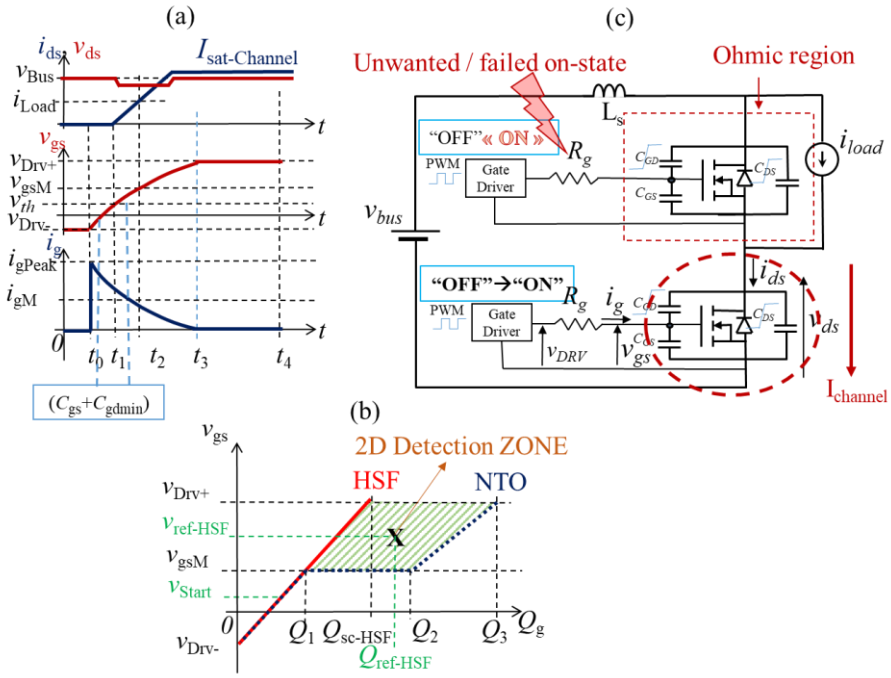

Fig. 2. (a) Turn-on switching characteristics of SiC MOSFET under HSF. **(b)** 2D representation of the gate charge characteristics "HSF" and detection zone with v_{gs}. **(c)** Equivalent circuit of the half bridge under HSF.

An HSF can be detected by monitoring v_{gs} and the amount of Q_g, whereas the assessment of the time variable is not directly required [15-16-19]. Then, a detection method based on the gate charge is proposed. As mentioned previously, a significant difference appears in the Q_g amount, as shown in Q_g characteristics, Fig. 2(b). A detection selectivity criterion can be introduced by the ratio $S = (Q_{SC\text{-}HSF})/(Q_{gTot})$. The ratio S is therefore a ratio between the quantity of gate charge under HSF and NTO. The smallest the ratio, the better the margin for the reference level Q_{ref} set. High ratios imply a difficulty in setting the Q_{ref} level, especially when adding the oscillation and circuit parasitic elements.

Table 1. Ratio of different technologies.

Technology	**Manufacturer**	**S**	$\mathbf{v_{rating}}$	$\mathbf{v_{bus}}$	$\mathbf{R_{dson}}$	$\mathbf{v_{gs}}$
Gan-GS6506	GanSystems	0.70	650 V	400 V	67 mΩ	0/6 V
SiC-C2M160120	WolfSpeed	0.47	1200 V	800 V	160 mΩ	-5/20 V
APT40SM120	MICROSEMI	0.34	1200 V	800 V	80 mΩ	0/20 V
Si-IKW40N120	Infineon	0.18	1200 V	960 V	-	0/15 V

For a better detection, the threshold level of v_{ref} and Q_{ref} need to be in the hatched trapezoid {(Q_1, v_{gsM}); (Q_2, v_{gsM}); (Q_{SC}, v_{Drv+}); (Q_3, v_{Drv+})} of Fig. 2(b). Hence, this detection method represents two-dimensional diagnosis.

Most of the time, this Q_g characteristic figure is given in the datasheet under NTO. The choice of the threshold detection levels v_{ref} and Q_{ref} can then be assessed from the datasheet. The method is naturally robust against variation in switching delay time due to variation in threshold voltage or current operating point of the load. With a constant threshold level, the detection will simply be a matter of integrated block design to obtain the gate charge Q_g [15-16].

2.3. Fault under load

In contrast, fault condition type II appears after the three normal time intervals are accomplished, namely, after t_4, where the MOSFET is in on-state ohmic mode $v_{gs} = v_{Drv+}$. In this fault condition, i_{ds} increases to $i_{ds\text{-}sat}$ (which can be calculated by the trans-conductance curve $i_{ds} = f(v_{gs})$ at v_{bus}), which in turn raises v_{ds} to the bus voltage v_{bus}, due to the MOSFET entering the saturation regime. Therefore, a positive value dv_{ds}/dt appears and a reverse current flows into the gate $i_g<0$ through C_{gd}, due to the Miller coupling and the capacitance C_{gd} decreases. All these phenomena lead to the increase of v_{gs} towards a larger value v_{gsov}, as shown in Fig. 3(a). The amount of gate charge is $Q_{SC\text{-}FUL}$, which also corresponds to a higher gate voltage v_{gsov}, observable in Fig. 3(b). A FUL can be detected by monitoring v_{gs} and the amount of Q_g, but for different threshold levels of v_{ref} and Q_{ref}, whose values need to be in the hatched triangle of Fig. 3(b).

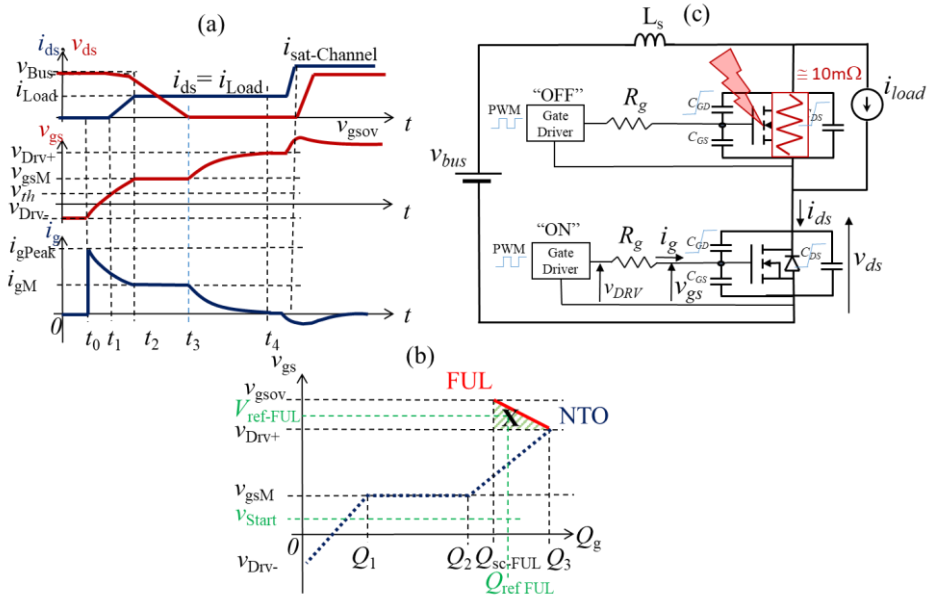

Fig. 3. (a) Turn-on switching characteristics of SiC MOSFET under FUL. **(b)** 2D representation of the gate charge characteristics "FUL" and detection zone with v_{gs} above v_{Drv+}. **(c)** Equivalent circuit of the half bridge under FUL.

2.4. Detection circuit based on gate charge monitoring

The proposed method is based on a gate charge characteristic as listed in this article as the integration method, also known as the gate charge method. In general, the charge transferred in the time interval is obtained by integrating the current (Eq. (6)). Since the charge needed in this work is the gate charge, the gate current i_g under NTO, HSF or FUL is integrated and the gate charge is then calculated for each condition. Using the reference levels v_{ref} and Q_{ref} presented in Eqs. (7)–(11), the detection of the SC is possible without setting a detection time window [17].

$$Q_g = \int i_g \, dt \tag{6}$$

$$v_{ref-Start} = p.v_{Drv+} \tag{7}$$

$$v_{ref-HSF} = k.v_{Drv+} \tag{8}$$

$$Q_{ref-HSF} = k'.Q_{Tot} \tag{9}$$

$$v_{\mathrm{ref-FUL}} = (1 + \mathrm{r}).v_{\mathrm{Drv+}} \tag{10}$$

$$Q_{ref-FUL} = r'.Q_{Tot} \tag{11}$$

With *p, k, k', r, r'* ponderation multipliers needed for the appropriate position of the reference levels.

Table 2. 2D diagnosis algorithm for HSF.

Comparator	**Output diagnosis**
If Q_g>$Q_{ref\text{-}HSF}$ **AND** v_{gs}>$v_{ref\text{-}HSF}$ then	NTO
If Q_g<$Q_{ref\text{-}HSF}$ **AND** v_{gs}>$v_{ref\text{-}HSF}$ then	HSF

Table 3. Diagnosis algorithm for FUL

Comparator	**Output diagnosis**
If Q_g>$Q_{ref\text{-}FUL}$ **AND** v_{gs}<$v_{ref\text{-}FUL}$ then	NTO
If Q_g<$Q_{ref\text{-}FUL}$ **AND** v_{gs}>$v_{ref\text{-}FUL}$ then	FUL

Tables 2 and 3 simplify the aforementioned figures regarding the gate charge characteristics and also provide guidance for the detection circuit below [6], gathering all the data to design the detection circuit. A comparator with $v_{ref\text{-}Start}$ (7) activates the detection circuit. A differential amplifier at the R_S terminals (sensing resistance integrated on the gate driver, R_s<<R_g+R_{int}) is needed, to create the image of the current i_g from the voltage across the sense resistor R_s and then to amplify it for better integration. With those two main blocks

(Diff. Amp. followed by Integrator), one obtains the gate charge Q_g, which is then further compared with the threshold $Q_{ref\text{-}HSF}$ and $Q_{ref\text{-}FUL}$ levels. Before that, to ensure that the detection is at the right moment, two additional comparators with $v_{ref\text{-}HSF}$ and $v_{ref\text{-}FUL}$ are used to activate the monitoring, as shown in Fig. 4.

For HSF in Table 2, when the output of the $v_{ref\text{-}HSF}$ comparator reaches a logic state '1' (non-priority value of the AND gate), this signal goes through the first input of the AND-HSF gate. The second input decides the state of the detection circuit: if the calculated Q_g is below the $Q_{ref\text{-}HSF}$, then the second input (the output of the $Q_{ref\text{-}HSF}$) of the AND-HSF gate goes to the high '1' logic state. The output of the AND-HSF gate goes high as well, which generates a flag for further SC protection. In contrast, if one of those two inputs; the two outputs of the $v_{ref\text{-}HSF}$ and $Q_{ref\text{-}HSF}$ comparators; is in a '0' logic state, there is no flag and no detected SC. For FUL, the same method is applied where both $v_{ref\text{-}FUL}$ and $Q_{ref\text{-}FUL}$ comparator outputs need to have a '1' logic state.

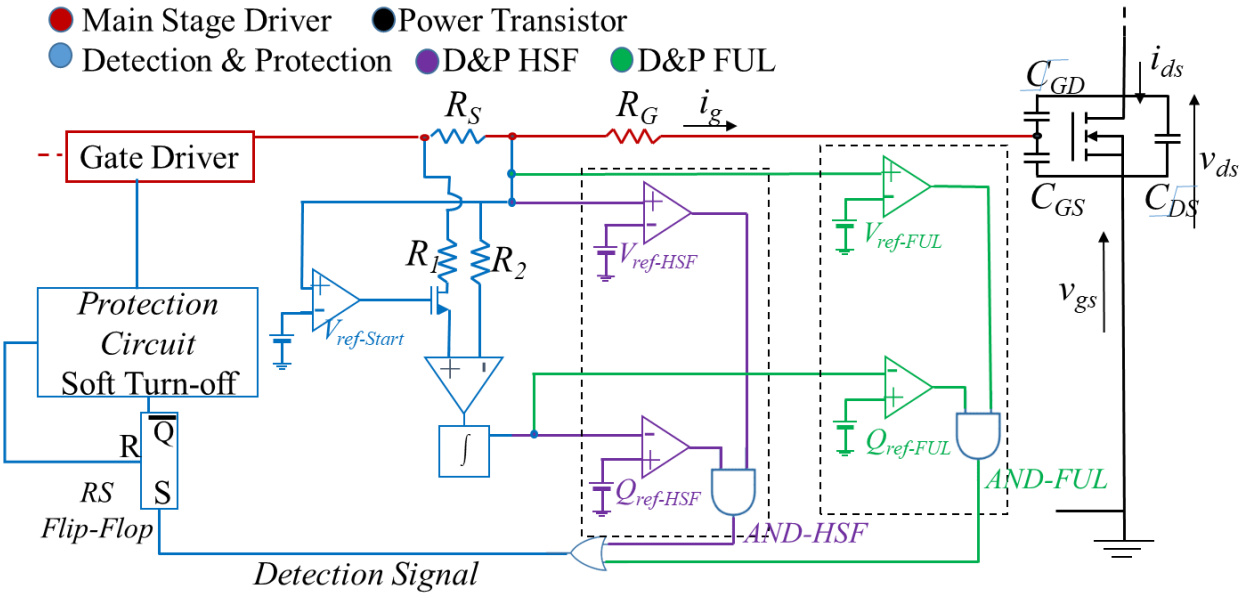

Fig. 4. Fast 2D diagnosis and protection circuit based on gate charge.
Note: Rs = 1 Ω, R1 = R2 = 20 kΩ and other blocks are considered ideals.

This principle will be more sensitive and robust for lower $Q_{SC\text{-}HSF}/Q_{gTot}$ ratios. This constraint is far from assured for WBG devices, where the C_{gd}/C_{gs} ratio is voluntarily minimised by designers to reduce the cross-talk phenomenon in inverter leg operation. As shown in Table 1, some commercially available SiC devices will be more suitable than others. Commercially available high-voltage GaN power transistors seem poorly adapted to this technique, while other protection techniques are adapted for GaN [18]. Higher $v_{ref\text{-}HSF}$ values lead to a more robust diagnosis, albeit with longer delay times. Nevertheless, it remains a general principle, also named "2D adaptive detection", only combining two low-voltage waveforms or signals without resorting directly to time measurements. Another 2D SC detection method is based on the source sensing [19]. One can note that our

proposed method can be easily integrated in a low voltage ASIC, which would not be allowed with classical high-voltage detection V_{dssat} (saturation voltage) or would require high-voltage ASIC technology. Moreover, the Q_g method is an integral technique that will introduce less signal-to-noise ratio (SNR).

3 Derivation detection method

3.1. Behaviour and characteristics

Even with optimised detection thresholds, the previous method based on the gate-current integration over the gate-voltage range may not be fast enough for SC protection. The following methods provide more direct quasi-instantaneous detection without the need for the gate charge method. The impact of the capacitance C_{gd} on the switching behaviour is also demonstrated for a new detection method based on monitoring the quasi-derivation of v_{gs}. There are three important time intervals on the behaviour of v_{gs}, as explained above. The first one has a slope of $1/C_{issmin}$, followed by the Miller plateau, where C_{gd} is involved, and the last one has a slope of $1/C_{issmax}$. Using this alteration of slopes, a significant impact appears on their time derivatives. Figure 5 shows the dv_{gs}/dt signal behaviour under NTO and SC conditions, where two distinctive changes of slope can be observed. The time interval $[t_0, t_2]$ in Fig. 5 dv_{gs}/dt signal presents a high peak "$1/C_{issmin}>1/C_{issmax}$", followed by a decrease until reaching a dip presenting the plateau period $[t_2, t_3]$. A smaller peak occurs at t_3 to present $1/C_{issmax}$. The dv_{gs}/dt signal under SC is reasonably straight forward, where there is only $1/C_{issmin}$ as a slope for v_{gs} signal, from t_0 to t_4 dv_{gs}/dt is the derivation of the slope $1/C_{issmin}$, the dip or the smaller peak is not present. Figures 5(a) and (b) introduce two different ways to analyse the derivation signal. Other approaches are studied on the detection of the plateau [20].

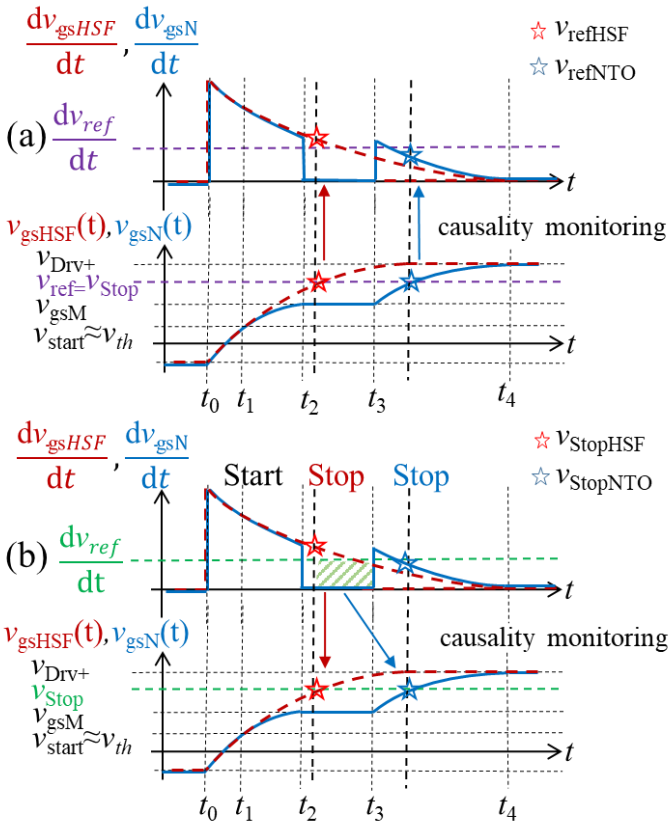

Fig. 5. dv_{gs}/dt characteristics under "NTO" and "HSF": **(a)** Slope detection approach; **(b)** dip detection approach. Stars represent the levels obtained for the same gate voltage, $v_{gs} = v_{ref} = v_{stop}$, with $v_{ref} > v_{gsM}$ for the slope approach and for the dip approach $v_{gs}=v_{stop}$ is not a reference level for comparison.

From this analysis, two detection approaches can be concluded. The first one is based on the changes of the dv_{gs}/dt waveforms, where a threshold level dv_{ref}/dt is needed to be fixed for the dv/dt signal to distinguish between $1/C_{issmax}$ for NTO and $1/C_{issmin}$ for HSF at the threshold level $v_{gs} = v_{ref}$. This threshold level v_{ref} is used to activate the readout of the comparison, as well as the SC detection, seen in Table 4. Figure 5(a) shows the importance of the v_{ref} level (represented by stars), while removing any direct dependence with time. Indeed, the v_{ref} detection is indirectly reflected in different times for NTO and HSF. Therefore, the difference between the slopes define the NTO or HSF detections. The second detection approach is based on the detection of the dip in the derivation signal, the presence of Miller plateau. A threshold level dv_{ref}/dt is also needed. Under SC conditions, the two approaches do not have any difference detecting at v_{ref} the presence of $1/C_{issmin}$ or a non-presence of a dip. The approach is to detect the signal above dv_{ref}/dt before reaching $v_{ref,}$, as illustrated in Tables 4 and 5. In contrast, under NTO conditions, the two approaches are almost similar, both of them being based on the detection of the signal below dv_{ref}/dt. The only difference is to detect before $v_{gs}>v_{ref}$ when the dip is quickly detected or at $v_{gs} = v_{ref}$ detecting $1/C_{issmax}$ slope changes.

Table 4. 2D diagnosis for HSF with v_{gs} slope approach.

Comparator	Output diagnosis
If $v_{gs} = v_{ref}$ **AND** $dv_{gs}/dt<dv_{ref}/dt$ then	NTO
If $v_{gs} = v_{ref}$ **AND** $dv_{gs}/dt>dv_{ref}/dt$ then	HSF

Table 5. 2D diagnosis for HSF with dip approach.

Comparator	Output diagnosis
If $dv_{gs}/dt<dv_{ref}/dt$ **AND** $v_{gs}<v_{ref}$ then	NTO
If $dv_{gs}/dt>dv_{ref}/dt$ **AND** $v_{gs}<v_{ref}$ then	HSF

Both approaches can be accurate and robust because they are based on 2D detection $dv_{gs}/dt \sim i_{Ciss}$ combined with v_{gs}. The second approach may be faster in NTO operation, where dip detection is before reaching v_{ref}.

More importantly, the second approach (dip approach) should present a higher SNR than the slope method thanks to the high signal amplitude detection.

This one, dip approach, may help the robustness of the detection by allowing a lower dv_{ref}/dt; consequently, a wider discrimination range for a SC detection is offered, avoiding the small critical zone whenever v_{gsNTO} and v_{gsSC} have similar values. The different threshold voltages must be defined from key parameters extracted from the datasheet, operating conditions and experimental results.

3.2. Detection circuit based on derivation monitoring and simulation behaviour

The proposed method is based on the derivation method. As known, the current that runs through a capacitor is given by the voltage/current relationship (12), where C_s is the sensing capacitor in parallel with the gate of the power device. Using this voltage/current relationship gives the derivative of v_{gs}:

$$\frac{dv_{gs}}{dt} = \frac{i_{Cs}}{c_s} \tag{12}$$

Figure 6 presents the detection circuit for a fixed R_g. The capacitor C_s connected in parallel with the gate is a sense capacitor, sensing the derivation of the voltage v_{gs}. This sense capacitor must be much smaller than the minimum input capacitor of the power transistor ($C_s << C_{issmin}$). The i_{cs} current passing through C_s is further

amplified and converted in a voltage, which is then compared with dv_{ref}/dt. Two other comparators with v_{gs} signal are used to create a monitoring window for the readout and detection. Flip-flops are added for both approaches, with the purple parts being the dip detection circuit and the green ones being the slope detection circuits.

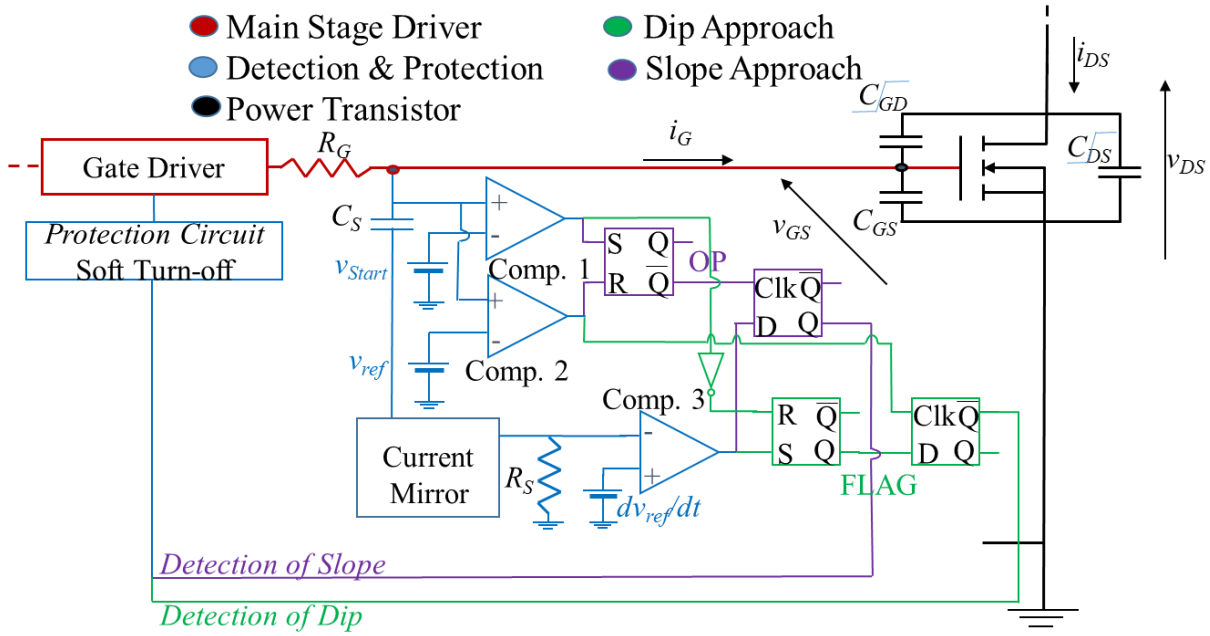

Fig. 6. Detection and protection circuit based on slope and dip approaches. Note: C_s = 100 pF, R_s = 100 Ω and other blocks are considered ideals.

4 Simulation results

Simulations using LTspice™ are performed to verify the validity of the proposed detection circuits. The parameters used in the simulations are on the low side a power device C2M0025120D, v_{bus} = 600 V, i_{load} = 50 A, v_{Drv} = -5/+20 V and R_g = 50 Ω and on the high side a Schottky diode C4D20120A, 20-A, 1200-V. In the switching cell, the Schottky diode is only used during the dead time and can therefore be current-undersized.

Gate loop and power loop parasitic inductances were included to better reproduce experimental waveforms, L_d = 25 nH L_s = 25 nH, L_g = 5 nH. The value of R_g is deliberately chosen high for representation purposes. For lower values of R_g, the detection must be faster. The LTspice™ model proposed by Wolfspeed does not take into consideration the thermal self-heating during accidental short circuit operations, which is fast and at high temperature levels. Modifications need to be added on the power transistor structure. [21] presents a transient electro thermal circuit model, which allows for analysis of the SC operation.

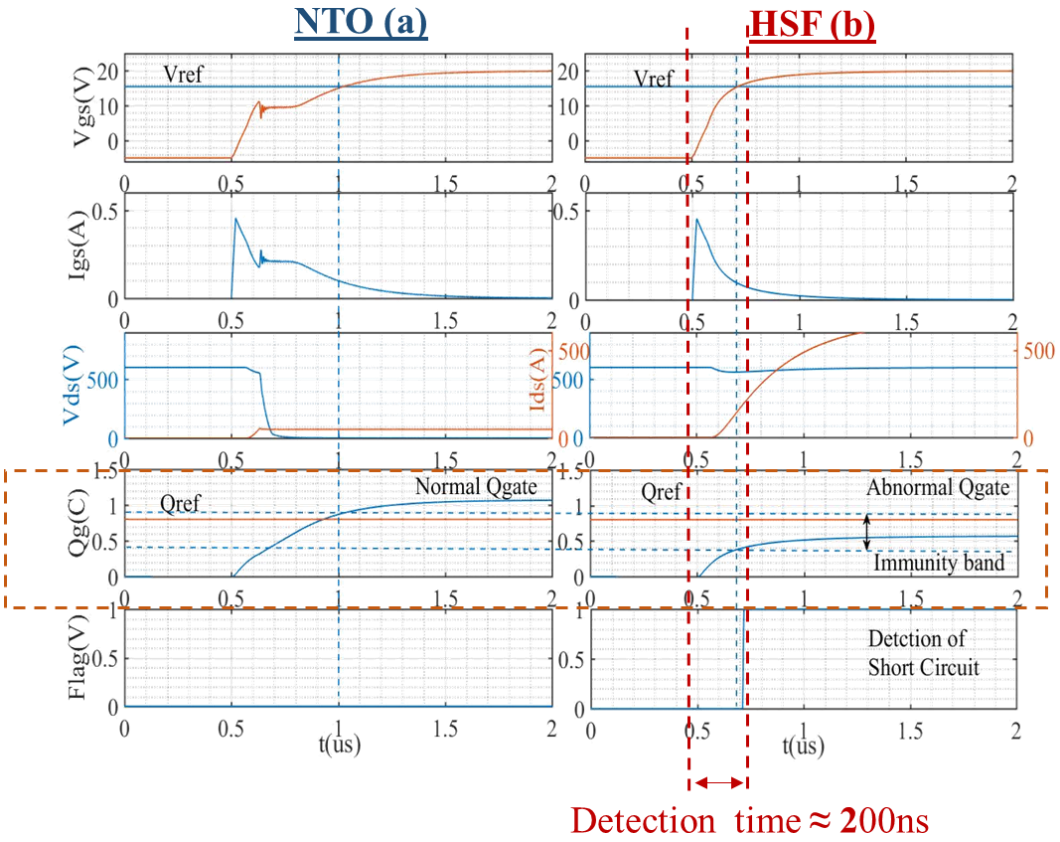

Fig. 7. Waveform characteristics using LTspice™ at V_{bus} = 600 V and I_{load} = 50 A under (a) NTO and (b) HSF.

*NB: Protection is not taken into consideration.

4.1. Detection and protection circuit simulation based on 2D gate charge monitoring

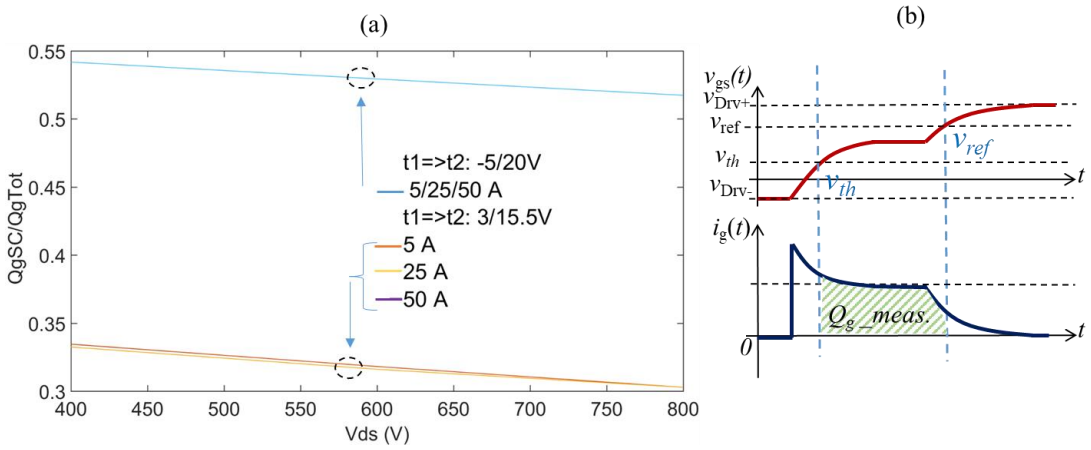

Fig. 8. (a) Variation of the amount of charge for different v_{ds}, i_{ds} and v_{gs}. **(b)** v_{gs} and i_g characteristic to present integration period.

Figure 8 introduces the robustness [10-22-23-24], highlighting the effect of different integration windows. Figure 8(a) presents the ratio of $Q_{SC\text{-}HSF}/Q_{gTot}$ for different v_{ds} and i_{ds}. The integration window can be calculated between

v_{gs} = -5/+20 V or +3/+15.5 V. This latter setting offers a smaller $Q_{SC\text{-}HSF}/Q_{gTot}$ ratio, which reduces the stress on the Q_g detection threshold (i.e. the lower the ratio, the easier the detection).

4.2. Detection and protection circuit simulation based on 2D derivation monitoring

Figure 9 presents the simulation voltage signal v_{gs} and its derivative under NTO and HSF conditions. Figure 10 takes the NTO condition further into different i_{ds} and v_{ds} values. The simulations show the slope differences and the dip presence in the gate voltage derivative. Parasitic inductors (L_d = 25 nH, L_s = 25 nH and L_g= 5 nH) were added to bring the approaches to their limits and as close as possible to a realistic circuit. The slope approach shows it limits in Fig. 10, where the dip approach assures the proper functionality, as shown in Fig. 11. The dip approach overcomes the overvoltage caused in the beginning of the Miller plateau, where this overvoltage makes the presence of the dip more remarkable and apparent in the derivative signal. Figure 11 supports the dip approach as well, where the dip is detected before the stop signal appearance and the flag remains 0, even when oscillations are present.

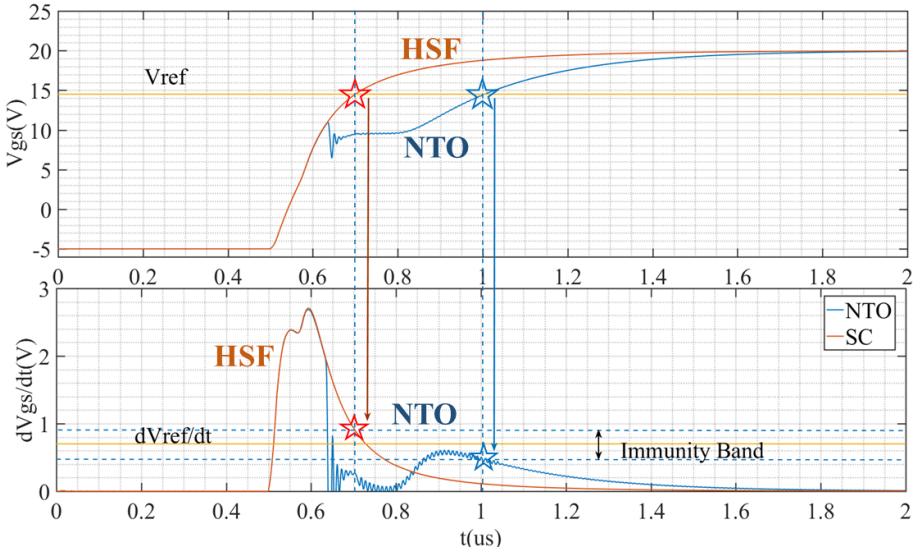

Fig. 9. Simulation waveforms of the derivation method, using the slope detection, under NTO and HSF conditions without the protection circuit, Rg = 10 Ω.

The detection flag is assured under both methods (integration and derivation). Figure 12 illustrates the circuit under protection for both methods. The detection time for both methods is below 200 ns due to the same reference gate voltage of v_{ref} 15.5 V. Section 5 explains the impact of this reference level. Figure 12 proves that both methods are independent of time. Figure 10 illustrates how important v_{ref} should be early for the detection of SC. With an early v_{ref}, an early detection will take place and probably v_{ref} interfering with the second peak in NTO mode, causing a false detection. To overcome this interference, the dip method will not take into

consideration the second peak, even if there are interferences. Figure 10 represents a variation of i_{load} and v_{bus} in the circuit under HSF, where we can see the oscillation reaches dv_{ref}/dt, for low i_{ds} and v_{ds}. Under SC, dv_{gs}/dt does not show any oscillation.

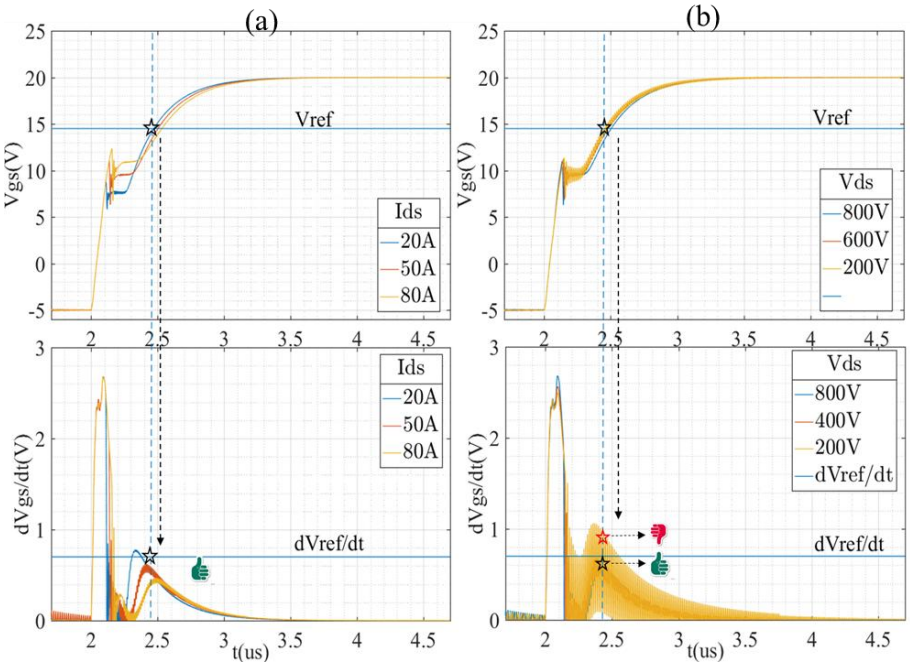

Fig. 10. Simulation waveforms of derivation method using the slope approach under NTO conditions for different i_{ds} and v_{ds} without the protection circuit (detection only).

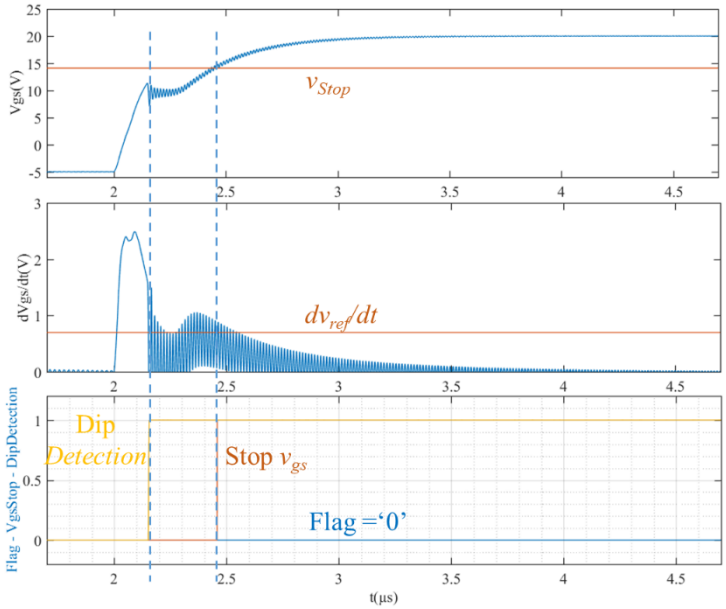

Fig. 11. Simulation waveforms of derivation method using the dip approach under NTO condition at V_{bus} = 200 V and I_{load} = 50 A. Parasitic induction is added.

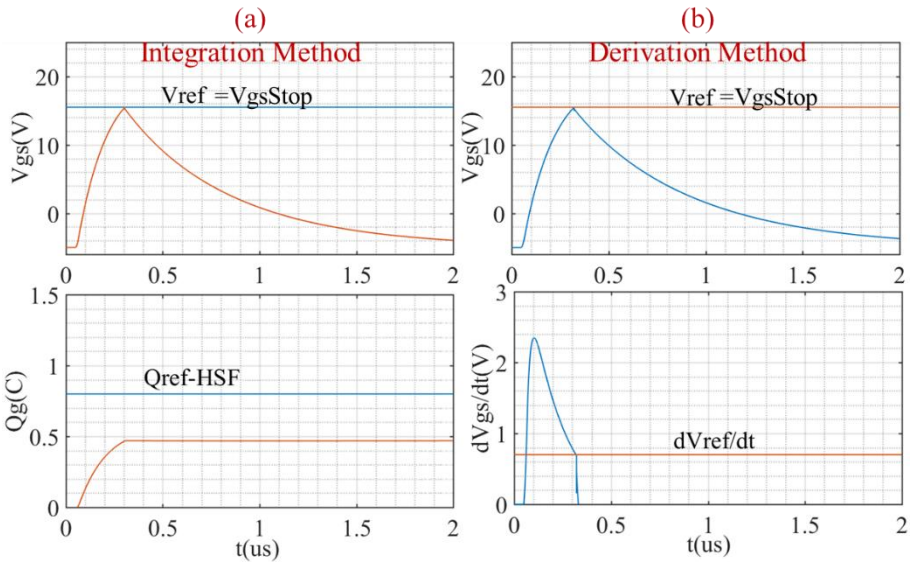

Fig. 12. Simulation waveforms under HSF conditions with the protection circuit: **(a)** gate charge method; **(b)** derivation method.

4.3. Experimental waveforms included in the simulation circuit

The simulation data presented hereinbefore show promising results. Hence, to further validate the concept of those detection methods, v_{gs} and v_{ds} experimental waveforms were extracted and included in the LTspice™ as simulation signals. The 2nd generation C2M0025120D including the high external gate resistance were used above in the simulation, for the unique purpose, to have clear waveforms of the proposed detection methods. The experimental waveforms were extracted using the Cree Demo board which includes Wolfspeed C3M0120090J (1 kV 90 mΩ) under half bridge configuration, fig.13. This 3rd generation (G3) model adds more challenges to the detection circuit, smaller gate resistor and input capacitor. The input capacitor is $C_{iss\text{-}G3}$ = 350 pF @600V ($C_{iss\text{-}G3}$ = 2.7 nF @1kV) with a external gate resistor $R_{G\text{-}G3}$ = 8 Ω ($R_{G\text{-}G2}$ = 50 Ω) and v_{Drv} = -4/+15 V (v_{Drv} = -5/+20 V).

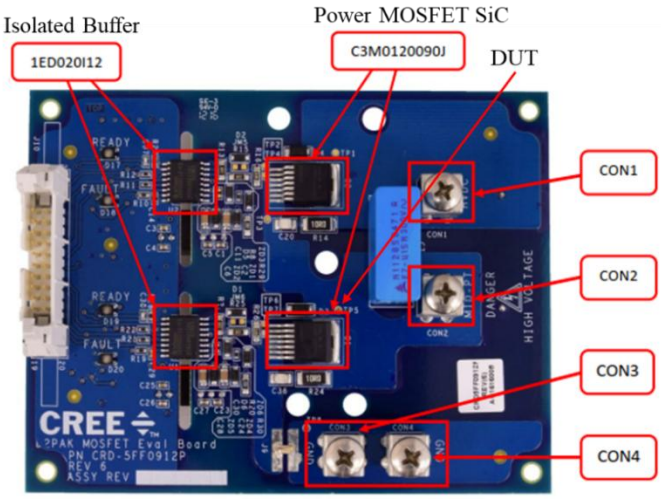

Fig. 13. Cree Demo Board used for v_{gs}(t), v_{ds}(t) extraction

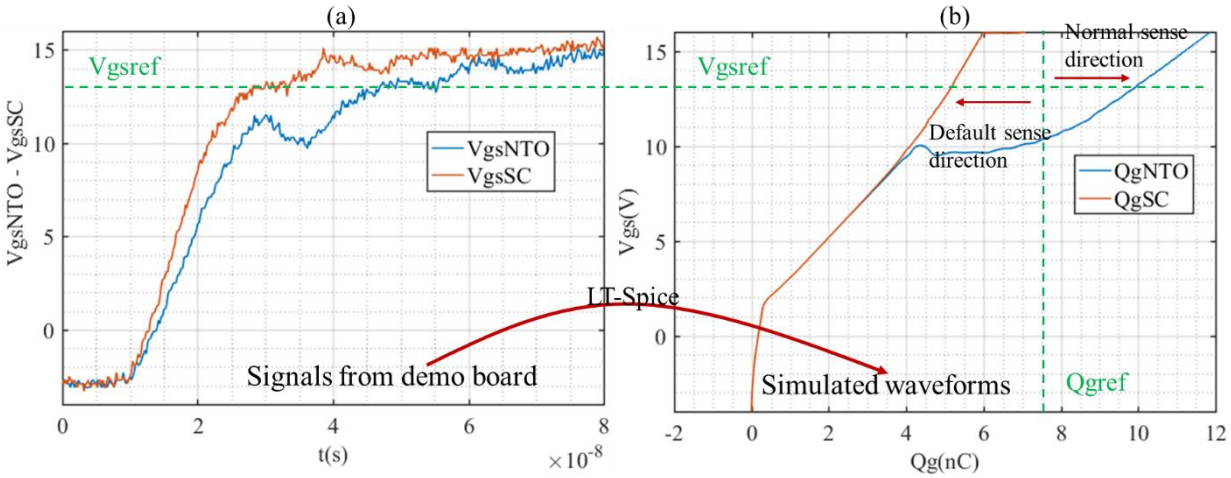

Fig. 14. (a). Real v_{gs} waveforms **(b).** Gate charge including (a); under NTO and HSF conditions,

Fig.14 (a). presents the real v_{gs} waveforms using the Cree demo board, fig. 13. Those real waveforms were imported into LTSpice platform; for the sole purpose to get closer to the real model. The waveforms have been used in the integration circuit proposed, validating the 2D gate charge plot, fig. 14 (b).

Fig. 15 validates the second method approach, using real v_{gs} waveforms. The waveform shows clear dip that ca be easily detectable with integrated circuit. In contrast to the integration method which has a higher SNR, the derivation method does not have a high noise tolerance, and for better robustness, chapter 5 below "Method discussion" discuss these issues.

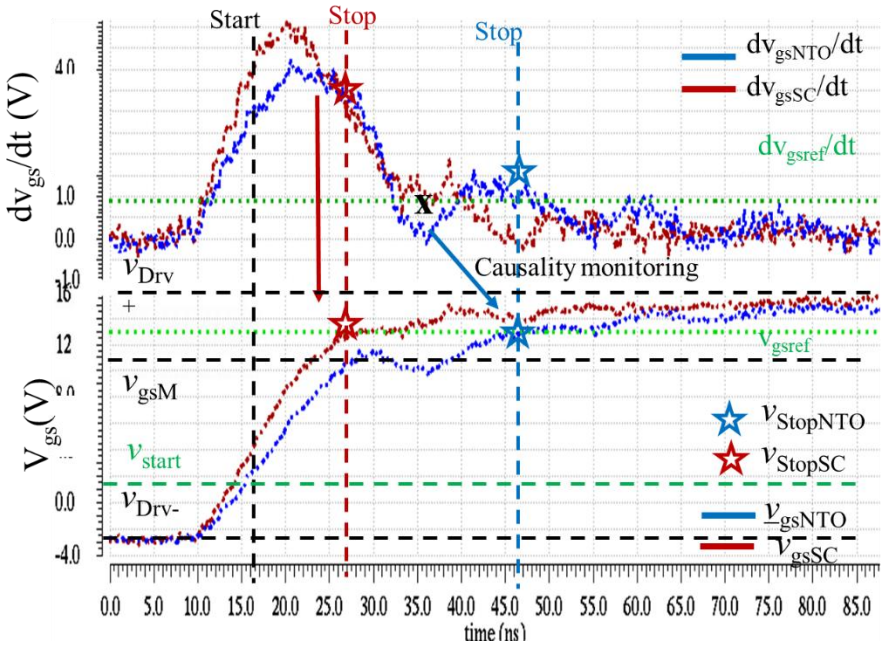

Fig. 15. Derivation method including real v_{gs} waveforms from CREE demo board to simulation.

5 Method discussion

Different detection methods proposed in the literature showed their pros and cons. Table 6. highlights diverse aspects for the most known methods and those proposed in this article. The table shows the high integration capability and how fast the detection comparing to the other detection methods.

Table 6. Comparison of the basic and proposed approaches related detection fault

Methods	**Pin**	**Approaches**	**Speed**	**Cost**	**Integration Capability in Gate Driver**
Desaturation	Drain	Very Indirect	- (Blanking time)	High Voltage sensing Diode	--
Shunt Resistor	Source	Straight forward	+	High precision Sensing resistor	-
ShuntFET current sensing	Additional Pin	Most Straight forward	++	Non-Standard Chip	+
Integration (Proposed)	Gate	Indirect	+	Low-Voltage Circuits	++
Derivation (Proposed)	Gate	Indirect	+	Low-Voltage Circuits	++

To discuss further more the proposed method, Figures 16 and 17 show a timing chart for both approaches (dip and slope) under NTO and HSF. One can see that v_{gs} is still rising to its saturation value. As shown in Fig. 16, the detection starts at t_{start} where $v_{gs} \approx v_{th}$ and stops at $t_{detection}$ where $v_{gs} = v_{ref} = v_{stop}$, at this time the detection signal depends on the output of the third comparator, as shown in Fig. 6. The output of the third comparator signal is neglected before and after v_{ref}. Figure 17 shows the same detection start signal, the stop signal is where $v_{gs} = v_{ref}$ but it different at reading the flag. The flag is activated at $t_{detection}$ the first crossing dv_{gs}/dt and the reference signal, where it is saved until $t_{activation}$.

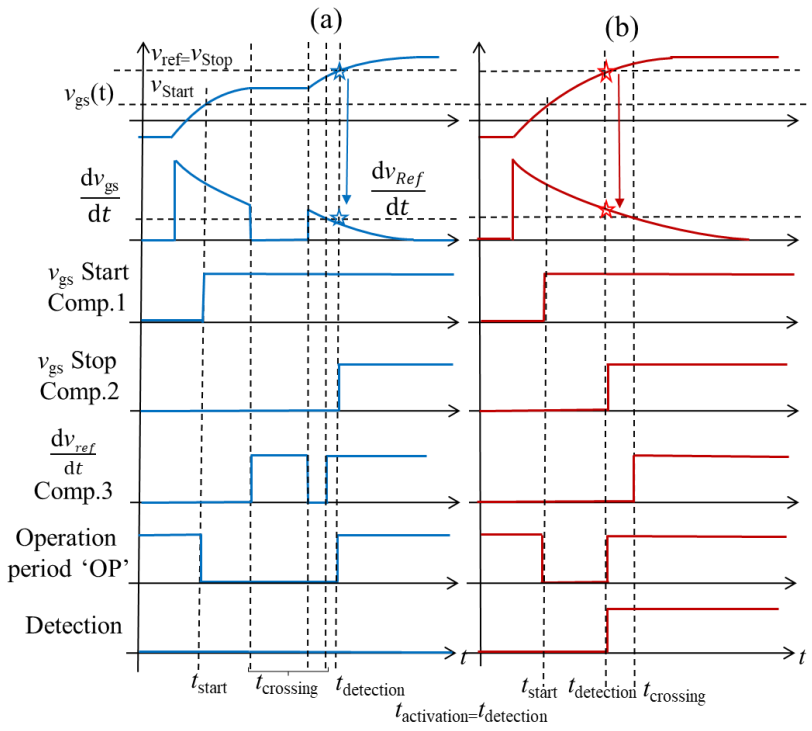

Fig. 16. Timing chart for slope detection approach under **(a)** NTO and **(b)** HSF.

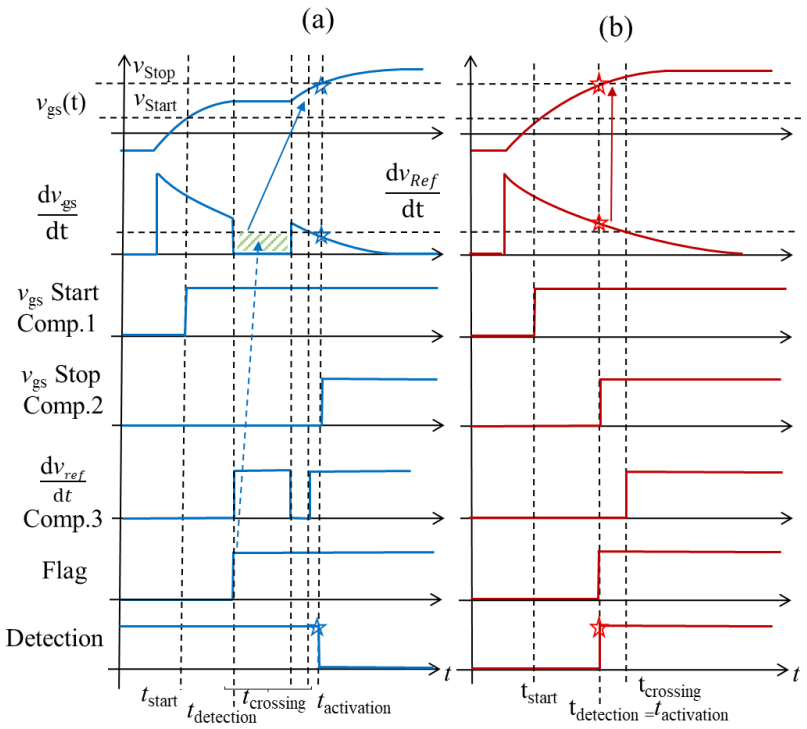

Fig. 17. Timing chart for dip detection approach under **(a)** NTO and **(b)** HSF.

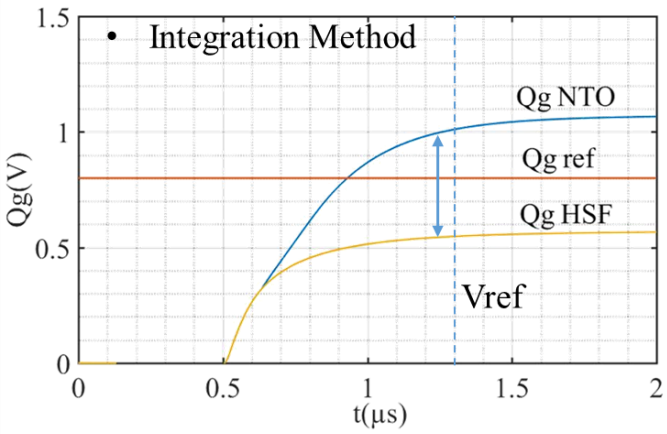

Fig. 18. Simulation waveforms of the gate charge under NTO and HSF conditions without the protection circuit.

Figure 18 shows the impact of the v_{gs} reference level and the critical zone. Its shows the gate charge amount in voltage (output of the integrator) under NTO and HSF, with the waveforms based on the same simulation criteria of Fig. 7 using LTspice™.

The discussed methods and approaches have no time dependency; however, they depend on when the gate voltage rises above the reference level v_{ref}, so the lower this reference, the earliest the detection, with the only condition of the $v_{gs} > v_{gsM}$. So which of these approaches is the fastest? For the gate method, Fig. 18 shows that reducing v_{ref} is difficult due to the limitation of the Q_g curve. For the derivation method, Fig. 11 shows that the dip approach is more robust than the slope approach. Using the dip approach, we have more flexibility with the reference level dv_{ref}/dt to cover more area for the v_{ref} reduction. With the dip approach, it can be the most robust method allowing v_{gs_Ref} to go lower.

6 Conclusions

This study introduces two two-dimensional detection method circuits, both of which are time independent. Both methods protect the power circuit in the event of a SC. The gate charge method exhibits a fast detection and protection capability and introduces less SNR under NTO and HSF. The reference levels are the critical values for both methods. The derivation method is presented with two approaches. With the slope approach, oscillation can slightly distort the detection, if the detection is at a critical v_{ref} (dv_{ref}/dt interfering with dv_{gs}/dt). In contrast, the dip approach is better due to the dip transition, under NTO conditions, even with dv_{ref}/dt interfering with dv_{gs}/dt, the detection of a dip occurs before the interference of the second peak. Under HSF, no oscillations are present for both approaches.

For robustness and fast detection, the higher the dv_{ref}/dt and the lower the v_{ref}, the better. In other words, setting dv_{ref}/dt higher, will prevent interference. Defining a low v_{ref}, allows for early detection.

In future works, the authors will implement experimentally and compare with the simulations. Several limitations must be particularly addressed, such as the precise assessment of the threshold voltages with the dip method, the effects of parasitic elements and non-ideal circuits.

Acknowledgements

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