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***Abstract*— This work presents a novel field for solid state power devices : a 4H-SiC specific device is examined as a current limiting device for serial protection application. The device structure is a vertical power MOSFET like with a existing N channel. Its performances is simulated with ISE TCAD tools. A study of its electrothermal behavior is presented, demonstrating the SiC superiority over silicon with regards to this field.**

***Index terms*-- SiC, current limiting device, serial protection, temperature, simulation.**

I. INTRODUCTION

Silicon carbide is well adapted for the power electronic needs. Already, many prototypes have been built and most of them show interesting abilities. It would be possible to translate in SiC technology most of the commercial silicon device and, therefore, to push away the limits of the semiconductor power device. The silicon carbide properties (Eg≈3 eV, Ec≈2 MV.cm^{-1}, λ_{300K}≈4.5 W.K^{-1}.cm^{-1}) allow to study specific device design for new application fields. This paper presents a silicon carbide high voltage current limiting device for 20 A/(300V to 600V) applications. Typically, this kind of device has to work under high temperature conditions without failure. A simulation study of the static I-V characteristics is proposed. Electrothermal simulations have been performed to take into account self-heating during a current surge wave. The parameters of the models used for the simulations [1] are:

Electron mobility model:

$$\mu_{dop} = \mu_{min1} e^{-\frac{P_c}{N_r}} + \frac{\mu_L \left(\frac{T}{300}\right)^{-\chi} - \mu_{min2}}{1+\left(\frac{N_r}{C_r}\right)^{a}} - \frac{\mu_1}{1+\left(\frac{C_s}{N_r}\right)^{b}}$$

$$\mu(E) = \frac{\mu_{low}}{\sqrt{1+\left(\frac{\mu_{low} E}{v_{sat}}\right)^2}} \qquad v_{sat} = v_{sat,0}\left(\frac{T}{T_0}\right)^{-v_{sat,e}}$$

Parameter	4H-SiC
μ_{min1} [cm^2/V.s]	20
μ_{min2} [cm^2/V.s]	0
μ_L [cm^2/V.s]	700
ξ	3
μ_1 [cm^2/V.s]	0
C_r [cm^{-3}]	4.5×10^{17}
α	0.45
C_s [cm^{-3}]	3.43×10^{20}
β	2
P_c [cm^{-3}]	0
Parameter	**4H-SiC**
v_{sat} [cm/s]	2×10^7
$v_{sat,exp}$	0.5

Impact ionization model:

$$a = g a_{n,p} \exp\left(\frac{-g b_{n,p}}{E}\right) \qquad \text{with} \quad g = \frac{\tanh\left(\frac{\hbar w}{600k}\right)}{\tanh\left(\frac{\hbar w}{2kT}\right)}$$

Parameter	4H-SiC
$a_{n,p}$	3.09×10^6 cm^{-1}
$b_{n,p}$	1.8×10^7 V/cm
E_o	4×10^5 V/cm
$\hbar w$	0.09 eV

Thermal conductivity:

$$l(T) = \frac{1}{a + bT + cT^2}$$

Parameter		4H-SiC
λ	a	0.01 K.cm/W
	b	6×10^{-4} cm/W
	c	6×10^{-7} cm/W.K
C		3 J/K.cm^3

II. DEVICE STRUCTURE.

Figure II-1 shows the device structure. The design looks like a vertical power MOSFET with a gate-source short-circuit and a preformed N channel. The epitaxial layer is optimized to withstand 600V. The channel is defined by the region between the P buried layer [2] and the SiC/oxide interface. The peripheral protection is realized by guard rings. They are integrated in the process flow of the active

region. The device is normally on. The current conduction is unidirectional and the current limiting behavior is available for positive drain to source bias voltage.

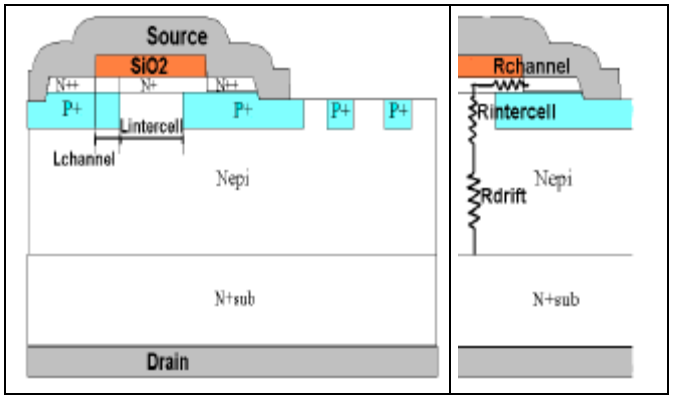

Figure II-1: Vertical cut of the device and its guard rings peripheral protection (the channel length 'Lchannel' and the intercell length 'Lintercell' are noted).

III. I – V STATIC CHARACTERISTICS.

A. *Static characteristic*

A typical I-V curve of a current limiter is shown on the Figure III-1. The channel design controls the limitation current $I_{SATURATION}$ and the on-resistance R_{ON}. The breakdown voltage (V_{br}) is withstood by the adjusted N epilayer for 600V capability (6 µm/10^{16}cm^{-3}). Therefore, the R_{ON} value is the addition of $R_{channel}$, R_{drift} and $R_{intercell}$ (Figure II-1).

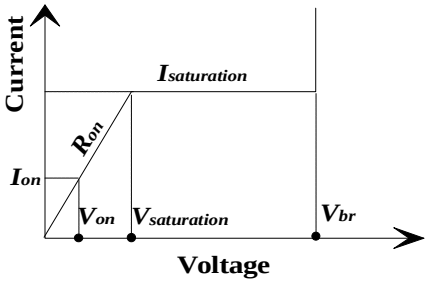

Figure III-1: typical I-V characteristic of a current limiting device.

For $0<V_{DS}<V_{SATURATION}$, the current increases linearly with V_{DS}. When V_{DS} is over $V_{SATURATION}$, the reverse space charge region due to the P+/$N_{channel}$ junction is wide enough to pinch off the channel. Then, the current can not increase more, and, remains equal to $I_{SATURATION}$. 2D process simulation and 2D electrical simulations with the tools package ISE TCAD [3] allow to study the electrical behavior the device. The figure III-2 shows a simulated characteristic with a current saturation of 1500 A/cm² and a specific on-resistance equals to 10 mΩ.cm² (compared to a silicon 600V structure 45 µm/10^{14} cm^{-3}, only $R_{drift}=w_{epi}/(qn\mu_n)\approx 250$ mΩ.cm²).

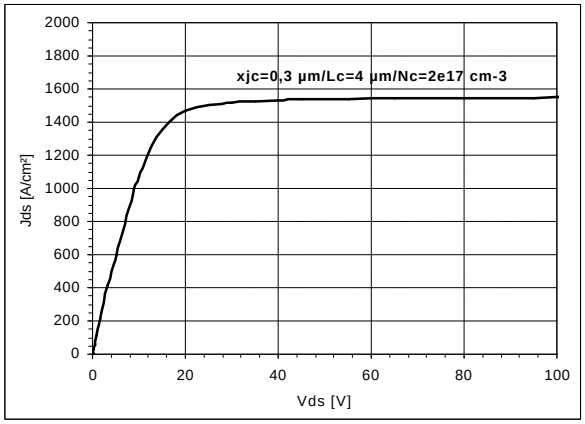

Figure III-2: I-V curve at T=300K (channel depth=0,3 µm; channel length=4 µm; channel doping level=2 10^{17} cm^{-3}, Lintercell=10 µm)

B. *Simple analytical model*

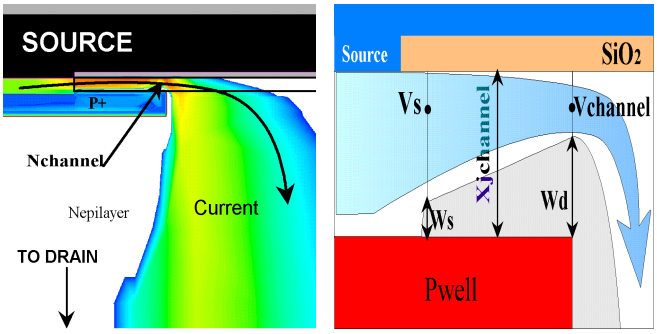

Figure III-3: Left picture: 2D mapping of the current inside the device near the channel region. Right picture: simplified current path in the channel.

As is shown on figure III-3 (left picture), the current flow crosses the channel horizontally, and then goes down through the intercell region and the epilayer. 2D simulations are needed to evaluate the parasitic effects of the intercell JFET and SiC/oxide interface charge. However an simple analytical model can be extracted from 2D simulations. The saturation effect can be described by the JFET equation [4] with V_{GS}=0V (figure III-3, right picture).
The built-in voltage and pinch-off voltage expressions are given by:

$$V_{bi}=\frac{kT}{q}\ln\left(\frac{N_A N_{channel}}{n_i^2}\right) \quad \text{and} \quad V_P=\frac{X_{jchannel}^2 q N_{channel}}{2e}$$

The space charge width expressions for both edges of the channel as defined on figure III-3 are as follows:

$$W_D=\sqrt{\frac{2e(V_{Channel}+V_{bi})}{qN_{Channel}}} \quad \text{and} \quad W_S=\sqrt{\frac{2eV_{bi}}{qN_{Channel}}}$$

The current versus voltage expression is:

$$I_{Channel}(V_{Channel})=\frac{W}{L_{Channel}}\frac{\mu_{Nchannel} q^2 N_{Channel}^2}{e} gg(V_{Channel})$$

where W is the third dimension of the channel and with

$$gg(V_{Channel}) = X_{jchannel}\frac{W_D^2 - W_S^2}{2} - \frac{W_D^3 - W_S^3}{3}$$

The saturation current is given when $W_D=X_{jchannel}$. This model is used to roughly evaluate the range of each channel parameter, before running the necessary 2D numerical simulations for the device optimization.

IV. ELECTROTHERMAL SIMULATION.

In case of current surge, the current limiting device has to operate under current and high voltage simultaneously. Therefore, the self-heating of the device generates high temperature spot and could start up a thermal run away failure. Electrothermal 2D simulations have been performed to take into account the effects of the temperature on carrier mobility [5,6], carrier concentration, thermal conductivity [7,8] and ionization coefficient [9]. The carrier mobility model [10,11] used is also a doping and electric field dependent model.

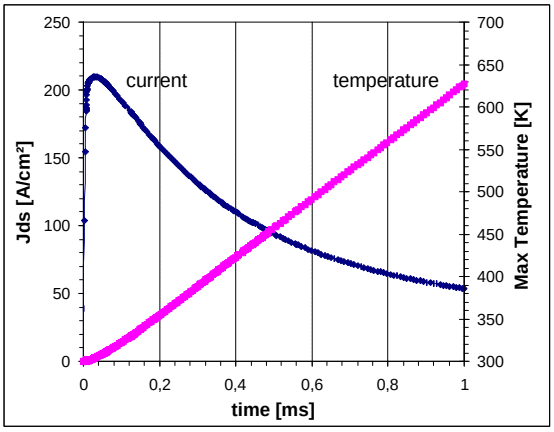

Figure IV-1: Current density and the maximum temperature inside the device versus time during a 500V/1ms V_{DS}-ramp. (channel depth=0,2 µm; channel length=4 µm; doping level=2 10^{17} cm^{-3}, T_A=300K, R_{TH}=0.5 K.cm²/W at the backside, R_{TH}=∞ at the topside).

Figure IV-1 shows an example of the average current density versus time and the corresponding maximal temperature inside the device during a 500V/1ms V_{DS}-ramp. When the temperature increases, the carrier mobility starts to decrease and leads the current to do the same. The hot spot is located at the end of the channel, close to SiC/oxide interface. Then, the stress of the oxide layer is quite important: high electric field (≈5 MV/cm) and high temperature (600 K). Figure IV-2 shows the average power losses in the device versus time under the same conditions as figure IV-1. The power reached after 1ms is up to 25 kW/cm² and seems to saturate as the current decreases. The device keeps a good behavior even under such high temperature conditions. The current level through the device essentially depends on the channel parameters and the electron mobility. The device structure allows to consider a good mobility value in the channel contrary to the classical SiC-MOSFET in which the inversion layer mobility is reduced by the SiC/oxide interface quality [12].

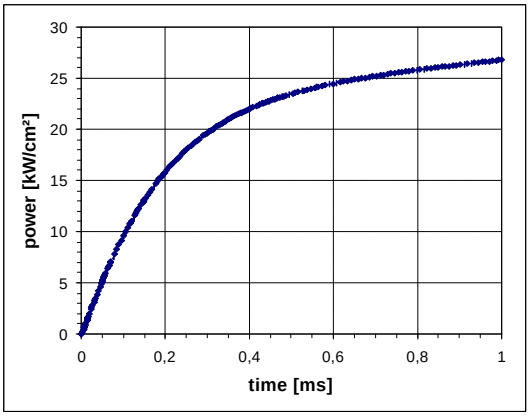

Figure IV-2: Average power versus time (Same conditions as figure IV-1).

For comparison with the silicon case, we studied a similar structure, as there is no commercial silicon current limiting device acting in the range of 20A/600V. The silicon device is a power MOSFET with an implanted channel [13], the low doped region is optimized for 600V (45 µm/10^{14} cm^{-3}). The same thermal boundary condition as for the SiC device is used for the silicon device: R_{TH}=0.5 K.cm²/W. The resulting saturation current is 60 A/cm² and the on-resistance is 600 mΩ.cm² (figure IV-3). Contrary to the SiC structure, after 0.9ms, the temperature inside is so high (intrinsic carrier level is enough) that a thermal run-away occurs and fails the silicon device (figure IV-3).

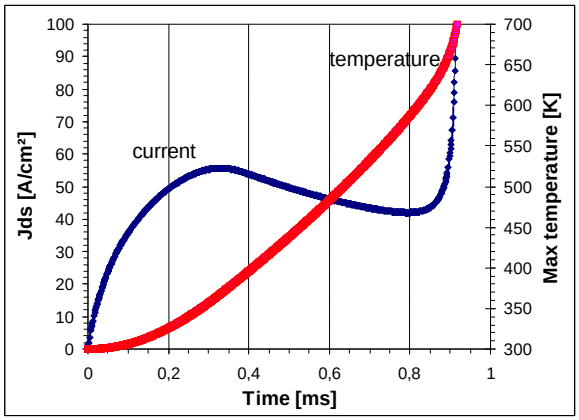

Figure IV-3: Thermal run-away of a silicon current limiting device (same VDS-ramp condition and thermal boundary conditions as for the SiC device figure IV-1).

In case of a current surge during at least 10ms:

To verify the current limiting ability during a current surge, some electrothermal simulations have been performed with a copper layer (1mm) added to the backside. In this case, the thermal conductivity and the thermal capacitance of the heat-sink are considered. Figures IV-4 and IV-5 show the

simulation results. The V_{DS} waveform is a 500V/1ms ramp during the first 1ms and then a constant (500V). The maximal temperature stabilizes close to 900 K and the device keeps working. The considered structure is designed for a 1000 A/cm² saturation current density (figure IV-5).

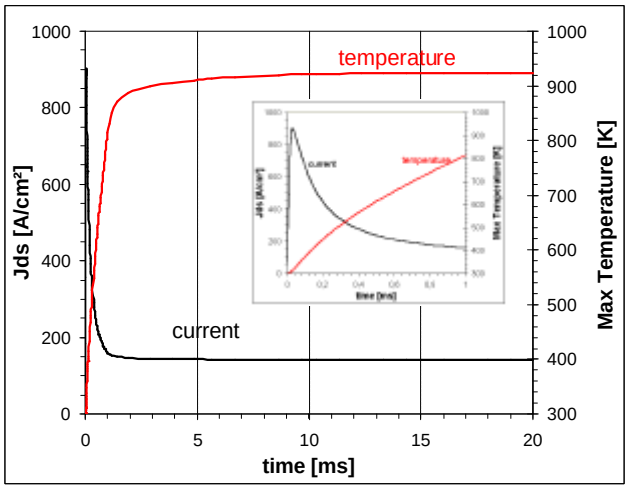

Figure IV-4: Electrothermal behavior in case of >10ms current surge.

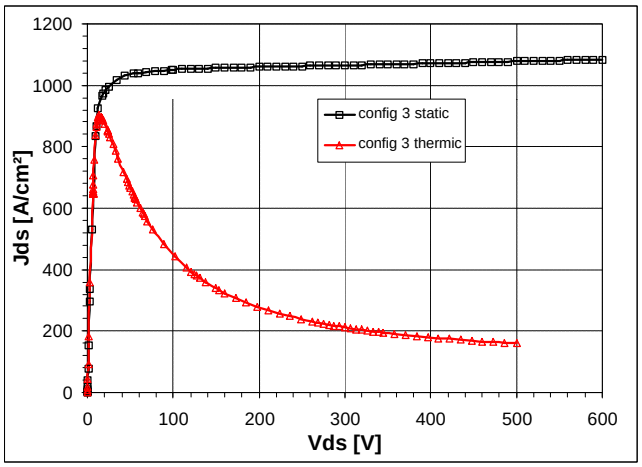

Figure IV-5: Comparison of the static I-V characteristic and electrothermal transient behavior (same structure as figure IV-4).

	SiC	Silicon
$J_{SATURATION}$	1000 A/cm²	60 A/cm²
R_{ON}	8 mΩ.cm²	600 mΩ.cm²
$V_{SATURATION}$	8V	36V
Max temperature reached	900K	650K (before run-away)
Time without run-away	At least 20ms	0.9 ms

Table 1: Ratings of both SiC and silicon device.

The silicon device is not adapted for this kind of application; the current density range and the specific on-state resistance lead to build device with surface of 1 cm² almost for a saturation current of 60A (R_{ON}≈0.6 Ω). To avoid the thermal run-away of the silicon device during at least 10ms, the saturation current density should be reduced and then the surface should be increased. Silicon carbide is well adapted (Table 1), can work with low surface (6 mm² for I_{SAT}=60A and R_{ON}≈0.1 Ω) and with a thermal boundary of 1 mm copper layer.

V. Conclusion

According to our simulation study, silicon carbide seems very attractive for current limiting application. The concept presented here can be applied to a large range of currents and voltages. The breakdown voltage could be improved without dramatically increases the on-resistance value (1500V – 10µm/5 10^{15} cm^{-3}). The device could even be controlled with a gate electrode for the switching off. It could be useful not only for serial protection but also for other applications, as for example, the motor starting phase.

Acknowledgment

We acknowledge SCHNEIDER ELECTRIC S.A for their support.

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